

Contents

Preface to the Second Adapted Edition
Preface

xiii
xvii

1. INTRODUCTION

1.1 – 1.33

- 1.1 Objectives 1.1
- 1.2 Evolution of Computers and Computer Generations 1.1
- 1.3 Technological Trends 1.10
- 1.4 Measuring Performance 1.10
- 1.5 Speedup 1.13
- 1.6 Amdahl's Law 1.13
- 1.7 Summary 1.15
- Solved Problems* 1.15
- Unsolved Problems* 1.27
- Objective Type Questions* 1.30
- Solutions of Unsolved Problems* 1.31

2. COMPUTER ORGANIZATION

2.1 – 2.28

- 2.1 Objectives 2.1
- 2.2 Introduction 2.1
- 2.3 Von Neumann Machine Architecture 2.1
- 2.4 Functional Units and Components in Computer Organization 2.4
- 2.5 Program Development Tools 2.12
- 2.6 Operating Systems 2.14
- 2.7 Summary 2.16
- Solved Problems* 2.16
- Unsolved Problems* 2.24
- Objective Type Questions* 2.26
- Solutions of Unsolved Problems* 2.27

3. COMPUTER ARITHMETIC

3.1 – 3.60

- 3.1 Objectives 3.1
- 3.2 From Electrons to Bits 3.1
- 3.3 Binary Representation of Positive Integers 3.2
- 3.4 Negative Integers 3.3
- 3.5 Fixed Point Arithmetic Operations on Positive and Signed (Negative) Integers 3.7
- 3.6 Floating-Point Numbers (IEEE754 Standard) and Operations 3.26
- 3.7 BCD Arithmetic Operations 3.32

3.8	Design of ALU	3.34	
3.9	Bit Slice Processors	3.37	
3.10	Summary	3.37	
	<i>Solved Problems</i>	3.38	
	<i>Unsolved Problems</i>	3.52	
	<i>Objective Type Questions</i>	3.54	
	<i>Solutions of Unsolved Problems</i>	3.56	
4.	INSTRUCTION SETS AND THE PROCESSOR ORGANIZATIONS		4.1 – 4.85
4.1	Objectives	4.1	
4.2	Introduction	4.1	
4.3	Register Transfers	4.4	
4.4	Register Transfer Language	4.5	
4.5	Concept of Instruction Formats and Instruction Set	4.5	
4.6	Instruction Set Types	4.9	
4.7	Types of Operands and Operations	4.12	
4.8	Generation of Memory Addresses and Addressing Modes	4.26	
4.9	Subroutine Nesting Using Stacks to Implement Subroutine Calls and Calling Conventions	4.41	
4.10	Processor Organizations	4.44	
4.11	Instructions in a General-Purpose Register Organization	4.45	
4.12	Instructions in a Stack-Based Organization	4.48	
4.13	Encoding of Machine Instructions	4.52	
4.14	General Features of RISC and CISC Instruction Sets	4.56	
4.15	Modern Processors Convergence of RISC with CISC	4.58	
4.16	Summary	4.58	
	<i>Solved Problems</i>	4.59	
	<i>Unsolved Problems</i>	4.77	
	<i>Objective Type Questions</i>	4.80	
	<i>Solutions of Unsolved Problems</i>	4.82	
5.	BASIC PROCESSING UNIT— REGISTER TRANSFER LANGUAGE, MICROOPERATIONS, HARDWIRED AND MICROPROGRAMMED CONTROL UNIT ORGANIZATIONS		5.1 – 5.50
5.1	Objectives	5.1	
5.2	Introduction	5.1	
5.3	Fundamental Concepts—Register Transfers	5.2	
5.4	Bus and Memory Transfer During Data Path Implementation	5.3	
5.5	Performing an Arithmetic or Logical Operation	5.6	
5.6	Shift Microoperations	5.10	
5.7	Fetch a Word from Memory and Transfer to IR or GPR or Other Word Storing Unit	5.11	
5.8	Storing a Word in Memory	5.12	
5.9	Execution of a Complete Instruction by Data Path Implementation—Processor Microarchitecture	5.14	
5.10	Branching Instruction	5.17	

5.11	Multiple Bus Organization	5.18
5.12	Hardwired Control Unit	5.20
5.13	A Complete Processor	5.23
5.14	Microprogrammed Control Execution	5.23
5.15	Concept of Separate Register Files for Floating-Point and Integer Data	5.31
5.16	Central Processing Unit: Coprocessor	5.32
5.17	Recent Innovations in Execution Unit Design	5.33
5.18	Summary	5.35
	<i>Solved Problems</i>	5.35
	<i>Unsolved Problems</i>	5.44
	<i>Objective Type Questions</i>	5.46
	<i>Solutions of Unsolved Problems</i>	5.47

6. INSTRUCTION PIPELINING AND PARALLEL PROCESSING **6.1 – 6.53**

6.1	Objectives	6.1
6.2	Introduction	6.1
6.3	Instruction Pipeline	6.3
6.4	Instruction Pipeline Hazards	6.6
6.5	Overcoming Hazards Using a Pipeline with Forwarding Paths	6.16
6.6	Instruction Set Design Influence on Pipelining	6.17
6.7	Parallel Processing and Pipelining	6.19
6.8	Example of a Pipelined CISC Processor	6.27
6.9	Example of Pipelined RISC Processors	6.28
6.10	Summary	6.30
	<i>Solved Problems</i>	6.30
	<i>Unsolved Problems</i>	6.48
	<i>Objective Type Questions</i>	6.50
	<i>Solutions of Unsolved Problems</i>	6.51

7. INSTRUCTION-LEVEL PARALLELISM—VLIW, VECTOR, ARRAY AND MULTITHREADED PROCESSORS AND USING PARALLEL OPTIMIZING COMPILER **7.1 – 7.33**

7.1	Objectives	7.1
7.2	Introduction	7.1
7.3	CISC and RISC Pipelines Instruction-Level Parallelism	7.4
7.4	VLIW (Very Long Instruction Word) Processors	7.7
7.5	Vector Processors	7.9
7.6	Array Processors	7.12
7.7	Multithreaded Processors	7.15
7.8	Compilation Techniques Support to Instruction-Level Parallelism	7.17
7.9	Summary	7.21
	<i>Solved Problems</i>	7.21
	<i>Unsolved Problems</i>	7.28
	<i>Objective Type Questions</i>	7.30
	<i>Solutions of Unsolved Problems</i>	7.31

8. THE MEMORY SYSTEM	8.1 – 8.50
8.1 Objectives 8.1	
8.2 Introduction 8.1	
8.3 Memory Hierarchy 8.3	
8.4 Replacement or Eviction, and Replacement Policy (Algorithms) 8.5	
8.5 Internal Organization of Semiconductor Main Memory Chips—RAM and ROM 8.6	
8.6 Semiconductor Main Memories—RAM 8.8	
8.7 Semiconductor Read-Only Memories—ROMs 8.24	
8.8 Speed, Size and Cost 8.27	
8.9 Auxiliary Memory Peripheral Devices—Secondary Storage Magnetic Ferrite Core Memories 8.28	
8.10 Peripheral Devices for Memory—Optical Disks CDROM Memories 8.32	
8.11 Secondary Storage—RAID 8.33	
8.12 Summary 8.35	
<i>Solved Problems</i> 8.36	
<i>Unsolved Problems</i> 8.45	
<i>Objective Type Questions</i> 8.48	
<i>Solutions of Unsolved Problems</i> 8.49	
9. CACHES	9.1 – 9.29
9.1 Objectives 9.1	
9.2 Introduction 9.1	
9.3 Data Caches, Instruction Caches, and Unified Cache 9.2	
9.4 Features Describing a Cache 9.3	
9.5 Direct-Mapped Caches 9.6	
9.6 Set Associative Cache 9.7	
9.7 Replacement Policy 9.9	
9.8 Cache Implementations 9.9	
9.9 Multilevel Caches 9.16	
9.10 Summary 9.17	
<i>Solved Problems</i> 9.18	
<i>Unsolved Problems</i> 9.25	
<i>Objective Type Questions</i> 9.26	
<i>Solutions of Unsolved Problems</i> 9.28	
10. VIRTUAL MEMORY	10.1 – 10.34
10.1 Objectives 10.1	
10.2 Introduction 10.1	
10.3 Virtual-Memory Organization 10.2	
10.4 Address Mapping Functions for Translating the Program Pages in Virtual to Physical Addresses Space 10.3	
10.5 Page Tables 10.4	
10.6 Associative Memory [Content Addressable Memory (CAM)] 10.7	
10.7 Page Replacement Algorithms (Policies) 10.8	
10.8 Translation Lookaside Buffer 10.9	

10.9	Partitioning	10.12	
10.10	Segmentation (Superpages or Page Blocks)—Partitioning of Virtual Address Space into Segment and Page Address	10.13	
10.11	Demand Paging and Swapping	10.19	
10.12	Caches and Virtual Memory	10.20	
10.13	Inverted Page Tables Concept	10.21	
10.14	Protection between Programs Running on the Same System	10.21	
10.15	Summary	10.23	
	<i>Solved Problems</i>	10.24	
	<i>Unsolved Problems</i>	10.29	
	<i>Objective Type Questions</i>	10.31	
	<i>Solutions of Unsolved Problems</i>	10.33	
11.	INPUT/OUTPUT ORGANIZATION		11.1 – 11.58
11.1	Objectives	11.1	
11.2	Introduction	11.1	
11.3	Peripheral Devices	11.2	
11.4	Input-Output Interface—Accessing I/O devices	11.2	
11.5	Synchronous Data Transfer Using Synchronous Bus	11.7	
11.6	Asynchronous Data Transfer Using Asynchronous Bus	11.8	
11.7	Modes of Transfer of Data, Command and Status	11.10	
11.8	Interrupts Driven I/O	11.12	
11.9	Priority Interrupts Organization	11.17	
11.10	Controlling Device Requests	11.19	
11.11	Exceptions	11.20	
11.12	Device Polling as Alternative to Interrupts	11.21	
11.13	DMA Based Transfer—Direct Memory Access (DMA)	11.22	
11.14	Bus Arbitration	11.24	
11.15	Interface Circuits	11.27	
11.16	Parallel Port Strobe Control and Handshaking	11.29	
11.17	Serial Port	11.31	
11.18	Communication Interfaces—I/O Interfaces	11.32	
11.19	I/O Processor	11.36	
11.20	Peripheral Devices Examples—External I/O Devices	11.38	
11.21	Summary	11.43	
	<i>Solved Problems</i>	11.44	
	<i>Unsolved Problems</i>	11.54	
	<i>Objective Type Questions</i>	11.56	
	<i>Solutions of Unsolved Problems</i>	11.57	
12.	MULTIPROCESSOR ARCHITECTURES		12.1 – 12.51
12.1	Objectives	12.1	
12.2	Introduction	12.1	
12.3	Multiprocessor Architectures	12.2	
12.4	Performance Characteristics of Multiprocessors	12.2	

- 12.5 Multicore Architectures—Single Chip Multiprocessors 12.5
- 12.6 Flynn Classification 12.5
- 12.7 Interconnection Structures 12.6
- 12.8 Interconnection Networks—Dynamic and Static Multiprocessor System Interconnects 12.9
- 12.9 Banyan and Delta Networks (Banyan Multistage Networks) 12.12
- 12.10 Interprocessor Arbitration 12.14
- 12.11 Interprocessor Communication 12.15
- 12.12 Memory Organization in Multiprocessors 12.16
- 12.13 Shared-memory Multiprocessor Systems 12.20
- 12.14 Synchronization—Memory Organization, Contention and Arbitration, and Cache Coherence and Synchronization Mechanisms 12.21
- 12.15 Cache Coherence 12.21
- 12.16 Message Passing Systems 12.27
- 12.17 Issues in Cluster Computing 12.30
- 12.18 Summary 12.31
- Solved Problems* 12.31
- Unsolved Problems* 12.45
- Objective Type Questions* 12.46
- Solutions of Unsolved Problems* 12.47

Index**I.1 – I.27**