Preface to the Second Adapted Edition

Since the publication of the original work of Nicholas Carter, this Schaum's Outlines has become an indispensable study guide for students of computer architecture for the following reasons:

- ✓ It covers the core concepts of hardware and software design for computer systems.
- ✓ It explains using a step-by-step approach the real world design choices for a computer system, and hardware interfaces with software.
- ✓ It emphasizes in detail how to make efficient use of system resources.
- ✓ It enables students to master fundamentals of computer architecture.
- ✓ Tutorial based treatment—important concepts are explained through solved examples and problems—helps students hone their problem-solving skills

RATIONALE BEHIND THE ADAPTATION

The earlier adaptation was inspired by the two classics—Computer Architecture by John P Hayes and Computer Organization by Carl Hamacher, Zvonko Vranesic and Safwat Zaky—both published by McGraw-Hill. The response to this adaptation within the last three years was significant—approximately 15000 engineering and professional training students became first-time readers of this book. Collated feedback from young lecturers in engineering colleges reinforced the finding that the chapters were valuable in honing problem solving skills, leading to ready adaptation in their lessons. The treatment and presentation of chapters on Computer Organization, Instruction Pipelining and Parallel Processing, Caches and Multiprocessor Architecture were highly appreciated.

The author has received several suggestions from academicians for inclusion of/separate emphasis on certain topics, which are in the syllabi of Computer Organization and Architecture course at Bachelor of Technology level in multiple engineering disciplines such as Computer Science and Engineering, Information Technology, Electronics and Communication, and Instrumentation and Control Engineering. The topics suggested by Professors in several Universities for inclusion were: array multiplier, register transfer language, arithmetic pipelining, delayed load and delayed branch, array processing, secondary storage: RAID, DRAM organization, Flynn's classification of parallel processing systems and inter-processor arbitration. The topics suggested for separate emphasis were: horizontal and vertical formats and address sequencer, data dependency, branch instruction, memory interleaving, direct mapping and set associativity in caches, read and write operation of associative memory and page replacement algorithm, mode of transfer, asynchronous data transfer, strobe control, handshaking asynchronous serial transfer, communication interface, and DMA based transfer.

Based on these suggestions, the first adaptation has been revised extensively and restructured to include/emphasize new and important topics.

THE USERS

This book will be particularly well-suited for students of undergraduate BE Computer Science and Engineering, BTech in Information Technology, and MCA. It will also prove to be a valuable reference for the students of BTech ECE, BCA, DOEACC 'A' Level, and BSc/MSc (Computer Science/IT) and for preparation of All India GATE competitive examinations.

CHAPTER ORGANIZATION WITH SPECIFIC CHANGES

The chapters have been restructured with inclusion of new topics keeping in mind the requirements of the syllabi of universities.

Chapter 1 covers the evolution of computers and first to fourth generations of computers. Students will learn how the new VVLSI technology has reduced space as well as power requirements in a computer system on the one hand and has improved a computer's performance greatly on the other. Babbage in 1832 conceptualized difference engine and repeated use of the registers to generate a table and terms in a series. A refreshing coverage of this concept, which is still a *must learn* concept for programming a computer, is one of the highlights of this chapter.

Chapter 2 discusses the computer organization. The coverage of the operating system as an interface between a user software and an organization of a computer system is the highlight of the original work. Other topics like von Neumann machine architecture, memory and I/O systems are explained with examples.

Chapter 3 describes the concepts of computer arithmetic. Topics of arithmetic circuits for addition, subtraction, multiplication and division are elucidated with examples. Key concepts used in the arithmetic circuit hardware design like- fast addition, fast multiplication, Booth's algorithm and bit pairing concept, BCD arithmetic and bit slice ***ALU*** are explained. The new addition in this chapter is a section on array multiplier.

Chapter 4 explains the core concepts such as instruction formats, operands and operations in the instruction-sets, regularity orthogonality, completeness and efficiency of the sets, encoding of machine instructions, memory operations, instruction execution, straight line, branching and subroutine call sequences, addressing modes, and the addressing of stacks and queues. These topics will help a student in learning the key concepts, which are used in the instruction sets of a computer system and further understanding the differences between GPR-based and stack-based architecture, between CISC and RISC computers and also the convergence of CISC instruction set architecture in the modern RISCs. Concepts of register transfer and register transfer language are the new additions in this chapter.

Chapter 5 covers the core concepts in processing unit designs and data path implementation. The path-implementation techniques are (1) use of the multiple bus-organization and (2) use of one of the two key technologies for execution of a program—one is single-cycle execution by a hardwired control unit, and the other is multicycle execution of a microprogram for an instruction and the microprogram for each instruction stored at a control ROM. Recent innovations in processor execution unit design are also covered in this chapter. The important areas that have been included under the purview of this chapter are—introduction to microoperation (including arithmetic microoperation), shift microoperation, logic microoperations and the central processing unit: co-processors.

Chapter 6 covers the core concepts of instruction pipelining and parallel processing in superscalar processors. Also, concepts of dynamic scheduling, and dynamic branch prediction are given due coverage. Examples of the pipelined CISC processors—Pentium and pipelined RISC processors—PowerPC and ARM will be highly useful to students. Among the enhancements to this chapter, is an important section on Arithmetic Pipeline.

Chapter 7 discusses instruction level parallelism and VLIW execution in the parallel processors. A novel concept of multithreaded processing used for achieving a higher performance in the parallel processors is provided in this chapter. A multithreaded multicore processor gives greatly improved performance at the reduced energy dissipation. Multithreading and multicore processor concepts are also explained.

Chapter 8 covers memory systems with due emphasis on DDRSDRAM, RDRAM, Rambus memory, ROM, EEPROM, flash and optical disks (CDROMs). The new topics that have been covered in this chapter are auxiliary memory, peripheral devices, error correction, replacement algorithms and secondary storage: RAID and DRAM organization.

Chapter 9 describes the cache memory concepts. In Chapter 10, the coverage of virtual memory organization, hit-miss logic, associativity in the caches and write-back and write through cache memories in a given computer organization is the highlight of the original work. Important topics such as mapping function for translation, content addressable memory, partitioning segmentation and exemplary segmentation and address translation mechanism in a Pentium are also covered in this chapter.

Chapter 11 deals with input-output organization in a computer system—programmed IO, parallel and serial ports and their interfaces, interrupts and the handling of masking and priorities, data transactions using direct memory accesses and the input-output processor and bus arbitration using daisy chaining, polling and independent requesting and granting mechanisms. The important concept of synchronous and asynchronous data transfer and bus transactions is also featured in this chapter. It also provides an understanding of USB, FireWire, and many external I/O devices used in a computer system. PCI and SCSI buses are also addressed.

Chapter 12 covers the multiprocessor system–synchronization, memory organization and arbitration; cache coherence problem; snoopy bus protocols and message passing systems. It also explains the concepts in multiprocessor organization—interconnection networks, multiprocessor system interconnects, and use in the interconnects concepts of crossbar switches, hypercube, multiport memories, combining requests, multistage and banyan-delta networks, directory based protocols to solve cache coherence problem in a multistage network, message routing schemes, deadlock and virtual channels, flow control strategies and a recent concept of cluster computing. The additional feature in this chapter is the coverage of Flynn's classification of parallel processing systems and interprocessor arbitration.

PEDAGOGY

Each chapter begins with objectives that offer concise information about expected learning outcomes. This is followed by an introductory paragraph that provides basic background and introduces the topics that students will learn. Important concepts are explained using solved examples and figures. Each chapter culminates with a summary, and a carefully selected assortment of solved problems. The objective type questions will help students further test their understanding of the concepts and also in the

preparation of competitive examinations. The new pedagogical enhancement in the revised adaptation is the inclusion of unsolved problems for practice. The rich pedagogy of the book includes:

- Solved Examples: 251
- Solved Problems: 316
- Objective Type Questions: 195
- New Unsolved Problems: 164

WEB SUPPLEMENT

The accompanying exhaustive online learning centre has solutions to the unsolved questions and problems given in the book.

For Instructors:
- Solution Manual
- Chapter wise PowerPoint slides with diagrams and notes for effective lecture presentations

For Students:
- A Sample Chapter
- Objective Questions with Answers
- Link to Reference Material

ACKNOWLEDGEMENTS

The author acknowledges his co-professors and lecturers for their suggestions and feedback to improve the previous adaptation. The author acknowledges his family members—Ms Sushil Mittal (wife), Dr Atul Kondaskar, Dr Shilpi Kondaskar (daughter), Arushi Kondaskar, Shalin Mittal (son), Ms Needhi Mittal (daughter-in-law) and Atharv Raj Mittal (grandson) for their affection. A note of acknowledgement is due to the following reviewers for their feedback.

Manoj Chaube
GLA Institute of Technology and Management (GLAITM), Mathura

Basudev Halder
Institute of Technology & Marine Engineering College, South 24 Parganas

Suchita Sharma
Inderprastha Engineering College (UPTU), Ghaziabad

Hiranmoy Roy
RCC Institute of Technology, College of Leather Technology, Kolkata

V S Shankar Sriram
Birla Institute of Technology, Ranchi

Finally, we would like to thank the Tata McGraw Hill Education team specially Vibha Mahajan, Shalini Jha, Nilanjan Chakravarty, Surbhi Suman, Dipika Dey, Anjali Razdan and Baldev Raj for their enthusiastic support and guidance during the preparation of the book. We would be grateful if readers send their valuable suggestions for further improvement of the book at the following email id—tmh.csefeedback@gmail.com (*kindly mention the title and author name in the subject line*).The readers can also refer the website http://www.rajkamal.org for further information on Computer Architecture and Computer and Electronic Engineering.