Field-Effect Transistors

The field-effect transistor[1] is a semiconductor device which depends for its operation on the control of current by an electric field. There are two types of field-effect transistors, the *junction field-effect transistor* (abbreviated JFET, or simply FET) and the *insulated-gate field-effect transistor* (IGFET), more commonly called the *metal-oxide-semiconductor* (*MOS*) *transistor* (MOST, or MOSFET).

The principles on which these devices operate, as well as the differences in their characteristics, are examined in this chapter. Representative circuits making use of FET transistors are also presented.

The field-effect transistor differs from the bipolar junction transistor in the following important characteristics:

1. Its operation depends upon the flow of majority carriers only. It is therefore a *unipolar* (one type of carrier) device.
2. It is simpler to fabricate and occupies less space in integrated form.
3. It exhibits a high input resistance, typically many megohms.
4. It is less noisy than a bipolar transistor.
5. It exhibits no offset voltage at zero drain current, and hence makes an excellent signal chopper.[2]

Almost all integrated circuits are now made with MOSFETs.

10.1 The Junction Field-effect Transistor

The structure of an *n-channel* field-effect transistor is shown in Fig. 10.1. Ohmic contacts are made to the two ends of a semiconductor bar of *n*-type material (if *p*-type silicon is used, the device is referred to as a *p-channel* FET). Current is caused to flow along the length of the bar because of the voltage supply connected between the ends. This current consists of majority carriers, which in this case are electrons. A simple side view of a JFET is indicated in Fig. 10.1*a* and a more detailed sketch is shown in Fig. 10.1*b*. The circuit symbol with current and voltage polarities marked is given in Fig. 10.2. The following FET notation is standard.

Source The *source S* is the terminal through which the majority carriers enter the bar. Conventional current entering the bar at *S* is designated by I_S.

Drain The *drain D* is the terminal through which the majority carriers leave the bar. Conventional current entering the bar at *D* is designated by I_D. The drain-to-source voltage is called V_{DS}, and is positive if *D* is more positive than *S*. In Fig. 10.1, $V_{DS} = V_{DD}$ = drain supply voltage.

Gate On both sides of the *n*-type bar of Fig. 10.1, heavily doped (p^+) regions of acceptor impurities have been formed by alloying, by diffusion, or by any other procedure available for creating *p-n* junctions. These impurity regions are called the *gate G*. Between the gate and source a voltage $V_{GS} = -V_{GG}$ is applied in the direction to reverse-bias the *p-n* junction. Conventional current entering the bar at *G* is designated I_G.

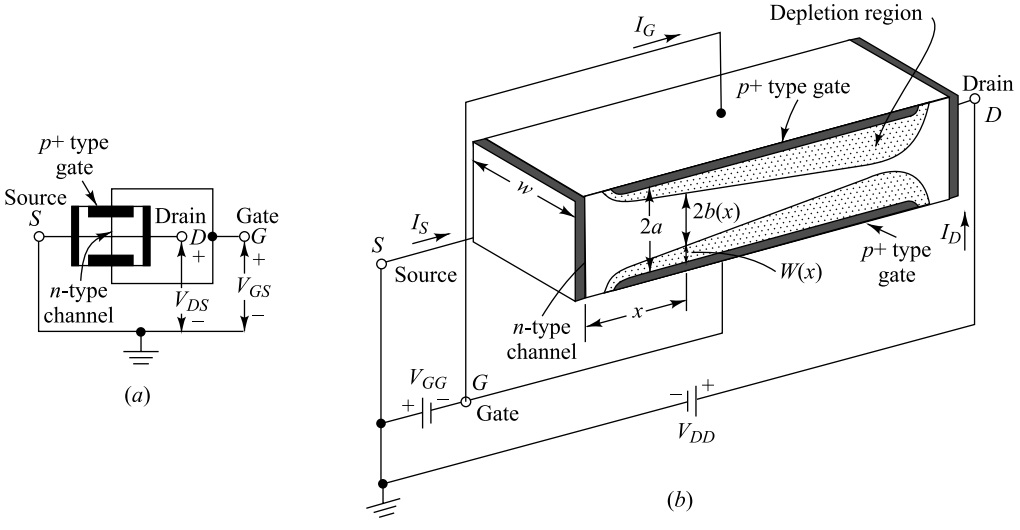


Fig. 10.1 *The basic structure of an n-channel field-effect transistor. (a) Simplified view. (b) More detailed drawing. The normal polarities of the drain-to-source (V_{DD}) and gate-to-source (V_{GG}) supply voltages are shown. In a p-channel FET the voltages would be reversed.*

Channel The region in Fig. 10.1 of *n*-type material between the two gate regions is the *channel* through which the majority carriers move from source to drain.

FET Operation It is necessary to recall that on the two sides of the reverse-biased *p-n* junction (the transition region) there are space-charge regions (Sec. 3.7). The current carriers have diffused across the junction, leaving only uncovered positive ions on the *n* side and negative ions on the *p* side. The electric lines of field intensity which now originate on the positive ions and terminate on the negative ions are precisely the source of the voltage drop across the junction. As the reverse bias across the junction increases, so also does the thickness of the region of immobile uncovered charges. The conductivity of this region is nominally zero because of the unavailability of current carriers. Hence we see that the effective width of the *channel* in Fig. 10.1 will become progressively decreased with increasing reverse bias. Accordingly, for a fixed drain-to-source voltage, the drain current will be a function of the reverse-biasing voltage across the gate junction. The term *field effect* is used to describe this device because the mechanism of current control is the *effect* of the extension, with increasing reverse bias, of the *field* associated with the region of uncovered charges.

FET Static Characteristics The circuit, symbol, and polarity conventions for an FET are indicated in Fig. 10.2, The direction of the arrow at the gate of the junction FET in Fig. 10.2 indicates the

direction in which gate current would flow if the gate junction were forward-biased. The common-source drain characteristics for a typical *n*-channel FET shown in Fig. 10.3 give I_D against V_{DS}, with V_{GS} as a parameter. To see qualitatively why the characteristics have the form shown, consider, say, the case for which $V_{GS} = 0$. For $I_D = 0$, the channel between the gate junctions is entirely open. In response to a small applied voltage V_{DS}, the *n*-type bar acts as a simple semiconductor resistor, and the current I_D increases linearly with V_{DS}. With increasing current, the ohmic voltage drop between the source and the channel region reverse-biases the junction, and the conducting portion of the channel begins to constrict. Because of the ohmic drop along the length of the channel itself, the constriction is not uniform, but is more pronounced at distances farther from the source, as indicated in Fig. 10.1. Eventually, a voltage V_{DS} is reached at which the channel is "pinched off." This is the voltage, not too sharply defined in Fig. 10.3, where the current I_D begins to level off and approach a constant value. It is, of course, in principle not possible for the channel to close completely and thereby reduce the current I_D to zero. For if such, indeed, could be the case, the ohmic drop required to provide the necessary back bias would itself be lacking. Note that each characteristic curve has an ohmic region for small values of V_{DS}, where I_D is proportional to V_{DS}. Each also has a constant-current region for large values of V_{DS}, where I_D responds very slightly to V_{DS}.

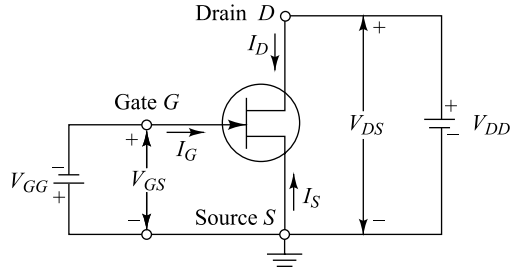


Fig. 10.2 *Circuit symbol for an n-channel FET. (For a p-channel FET the arrow at the gate junction points in the opposite direction.) For an n-channel FET, I_D and V_{DS} are positive and V_{GS} is negative. For a p-channel FET, I_D and V_{DS} are negative and V_{GS} is positive.*

If now a gate voltage V_{GS} is applied in the direction to provide additional reverse bias, pinch-off will occur for smaller values of $|V_{DS}|$, and the maximum drain current will be smaller. This feature is brought out in Fig. 10.3. Note that a plot for a silicon FET is given even for V_{GS} = +0.5 V, which is in the direction of forward bias. We note from Table 5.1 that, actually, the gate current will be very small, because at this gate voltage the Si junction is barely at the cutin voltage V_γ.

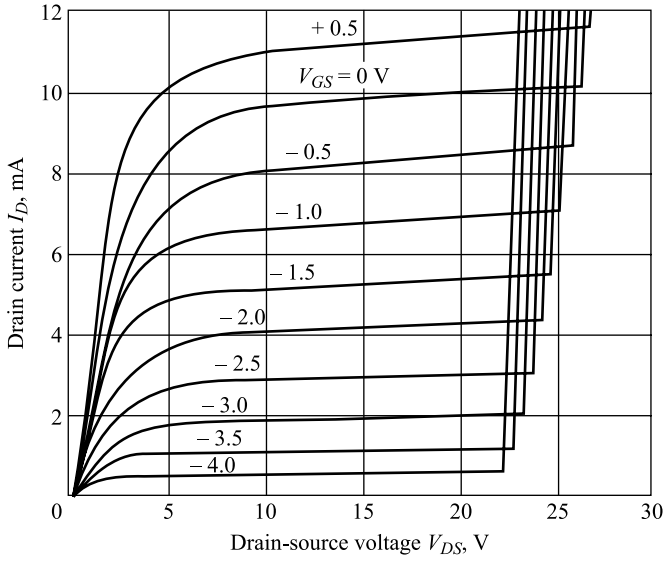


Fig. 10.3 *Common-source drain characteristics of an n-channel field-effect transistor.*

The maximum voltage that can be applied between any two terminals of the FET is the lowest voltage that will cause avalanche breakdown (Sec. 3.11) across the gate junction. From Fig. 10.3 it is seen that avalanche occurs at a lower value of $|V_{DS}|$ when the gate is reverse-biased than for $V_{GS} = 0$. This is caused by the fact that the reverse-bias gate voltage

adds to the drain voltage and hence increases the effective voltage across the gate junction.

We note from Fig. 10.2 that the *n*-channel FET requires zero or negative gate bias and positive drain voltage. The *p*-channel FET requires opposite voltage polarities. Either end of the channel may be used as a source. We can remember supply polarities by using the channel type, *p* or *n*, to designate the polarity of the *source* side of the drain supply.

A Practical FET Structure The structure shown in Fig. 10.1 is not practical because of the difficulties involved in diffusing impurities into both sides of a semiconductor wafer. Figure 10.4 shows a single-ended-geometry junction FET where diffusion is from one side only. The substrate is of *p*-type material onto which an *n*-type channel is epitaxially grown (Sec. 7.3). A *p*-type gate is then diffused into the *n*-type channel. The substrate which may function as a second gate is of relatively low resistivity material. The diffused gate is also of very low resistivity material, allowing the depletion region to spread mostly into the *n*-type channel.

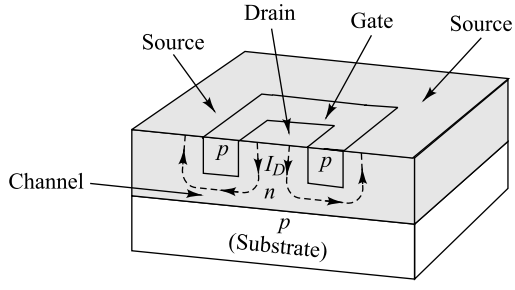


Fig. 10.4 *Single-ended-geometry junction FET.*

Example The JFET in Fig. 10.5 has the characteristics shown in Fig. 10.3. (*a*) If $V_{DD} = 20$ V, $V_{GG} = -2.5$ V, and $I_D = 3$ mA, determine the value of R_d. (*b*) If the drain current is to be reduced to 2 mA by changing R_d, determine the new value of R_d.

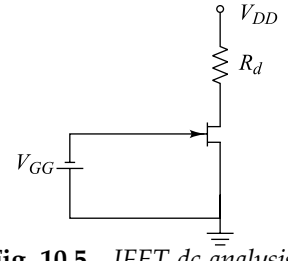


Fig. 10.5 *JFET dc analysis.*

Solution (*a*) From Fig. 10.3, we can read that for $V_{GG} = -2.5$ V and $I_D = 3$ mA, $V_{DS} = 10$ V. Therefore, the drop across R_d is 10 V, so that

$$R_d = \frac{10V}{3\,\text{mA}} = 3.33\,\text{k}\Omega$$

(*b*) For $I_D = 2$ mA, $V_{DS} = 2.5$ V (from Fig. 10.3). Therefore,

$$R_d = \frac{20 - 2.5}{2\,\text{mA}} = 8.75\,\text{k}\Omega$$

10.2 The Pinch-off Voltage V_P

We derive an expression for the gate reverse voltage V_P that removes all the free charge from the channel using the physical model described in the preceding section. This analysis was first made by Shockley,[1] using the structure of Fig. 10.1. In this device a slab of *n*-type semiconductor is sandwiched between two layers of *p*-type material, forming two *p*-*n* junctions.

Assume that the *p*-type region is doped with N_A acceptors per cubic meter, that the *n*-type region is doped with N_D donors per cubic meter, and that the junction formed is abrupt. The assumption of an abrupt junction is the same as that made in Sec. 3.7 and Fig. 3.10, and is chosen for simplicity. Moreover, if $N_A >> N_D$, we see from Eq. (3.17) that $W_p << W_n$, and using Eq. (3.21), we have, for the space-charge width, $W_n(x) = W(x)$ at a distance x along the channel in Fig. 10.1:

$$W(x) = a - b(x) = \left\{ \frac{2\epsilon}{qN_D} [V_o - V(x)] \right\}^{\frac{1}{2}} \tag{10.1}$$

where ϵ = dielectric constant of channel material
q = magnitude of electronic charge
V_o = junction contact potential at x (Fig. 3.1*d*)
$V(x)$ = applied potential across space-charge region at x and is a negative number for an applied reverse bias
$a - b(x)$ = penetration $W(x)$ of depletion region into channel at a point x along channel (Fig. 10.1)

If the drain current is zero, $b(x)$ and $V(x)$ are independent of x and $b(x) = b$. If in Eq. (10.1) we substitute $b(x) = b = 0$ and solve for V, on the assumption that $|V_o| << |V|$, we obtain the pinch-off voltage V_P, the diode reverse voltage that removes all the free charge from the channel. Hence

$$|V_P| = \frac{qN_D}{2\epsilon} a^2 \tag{10.2}$$

If we substitute V_{GS} for $V_o - V(x)$ in Eq. (10.1), we obtain, using Eq. (10.2),

$$V_{GS} = \left(1 - \frac{b}{a}\right)^2 V_P \tag{10.3}$$

The voltage V_{GS} in Eq. (10.3) represents the reverse bias across the gate junction and is independent of distance along the channel if $I_D = 0$.

Example For an *n*-channel silicon FET with $a = 3 \times 10^{-4}$ cm and $N_D = 10^{15}$ electrons/cm^3, find (*a*) the pinch-off voltage and (*b*) the channel half-width for $V_{GS} = \frac{1}{2} V_P$ and $I_D = 0$.

Solution (*a*) The relative dielectric constant of silicon is given in Table 2.1 as 12, and hence $\epsilon = 12\,\epsilon_o$. Using the values of q and ϵ_o from Appendix A, we have, from Eq. (10.2), expressed in mks units,

$$|V_P| = \frac{1.60 \times 10^{-19} \times 10^{21} \times (3 \times 10^{-6})^2}{2 \times 12 \times (36\pi \times 10^9)^{-1}} = 6.8 \text{ V}$$

(*b*) Solving Eq. (10.3) for b, we obtain for $V_{GS} = \frac{1}{2} V_P$

$$b = a\left[1 - \left(\frac{V_{GS}}{V_P}\right)^{\frac{1}{2}}\right] = (3 \times 10^{-4})\left[1 - \left(\frac{1}{2}\right)^{\frac{1}{2}}\right] = 0.87 \times 10^{-4} \text{ cm}$$

Hence the channel width has been reduced to about one-third its value for $V_{GS} = 0$.

10.3 The JFET Volt-ampere Characteristics

Assume, first, that a small voltage V_{DS} is applied between drain and source. The resulting small drain current I_D will then have no appreciable effect on the channel profile. Under these conditions we may consider the effective channel cross section A to be constant throughout its length. Hence $A = 2bw$, where $2b$ is the channel width corresponding to zero drain current as given by Eq. (10.3) for a specified V_{GS}, and w is the channel dimension perpendicular to the b direction, as indicated in Fig. 10.1.

Since no current flows in the depletion region, then, using Ohm's law [Eq. (2.7)], we obtain for the drain current

$$I_D = AqN_D\mu_n\varepsilon = 2bwqN_D\mu_n \frac{V_{DS}}{L} \tag{10.4}$$

where L is the length of the channel.

Substituting b from Eq. (10.3) in Eq. (10.4), we have, for small I_D,

$$I_D = \frac{2awqN_D\mu_n}{L}\left[1 - \left(\frac{V_{GS}}{V_P}\right)^{\frac{1}{2}}\right]V_{DS} \tag{10.5}$$

The ON Resistance $r_{d,\mathrm{ON}}$ Equation (10.5) describes the volt-ampere characteristics of Fig. 10.3 for very small V_{DS}, and it suggests that under these conditions the FET behaves like an ohmic resistance whose value is determined by V_{GS}. The ratio V_{DS}/I_D at the origin is called the ON *drain resistance* $r_{d,\mathrm{ON}}$. For a JFET we obtain from Eq. (10.5), with $V_{GS} = 0$,

$$r_{d,\mathrm{ON}} = \frac{L}{2awqN_D\mu_n} \tag{10.6}$$

For the device values given in the illustrative example in this section and with $L/w = 1$, we find that $r_{d,\mathrm{ON}} = 3.3$ K. For the dimensions and concentration used in commercially available FETs and MOSFETs (Sec. 10.5), values of $r_{d,\mathrm{ON}}$ ranging from about 100 Ω to 100 K are measured. This parameter is important in switching applications where the FET is driven heavily ON. The bipolar transistor has the advantage over the field-effect device in that R_{CS} is usually only a few ohms, and hence is much smaller than $r_{d,\mathrm{ON}}$. However, a bipolar transistor has the disadvantage for chopper applications[2] of possessing an offset voltage (Sec. 5.12), whereas the FET characteristics pass through the origin, $I_D = 0$ and $V_{DS} = 0$.

The Pinch-off Region We now consider the situation where an electric field ε_x appears along the x axis. If a substantial drain current I_D flows, the drain end of the gate is more reverse-biased than the source end, and hence the boundaries of the depletion region are not parallel to the longitudinal axis of the channel, but converge as shown in Fig. 10.1. If the convergence of the depletion region is gradual, the previous one-dimensional analysis is valid[1] in a thin slice of the channel of thickness Δx and at a distance x from the source. Subject to this condition of the "gradual" channel, the current may be written by inspection of Fig. 10.1 as

$$I_D = 2b(x)wqN_D\mu_n\varepsilon_x \tag{10.7}$$

As V_{DS} increases, ε_x and I_D increase, whereas $b(x)$ decreases because the channel narrows, and hence the current density $J = I_D/2b(x)w$ increases. We now see that complete pinch-off ($b = 0$) cannot take place because, if it did, J would become infinite, which is a physically impossible condition. If J were to increase without limit, then, from Eq. (10.7), so also would ε_x provided that μ_n remains constant. It is found experimentally,[3, 4] however, that the mobility is a function of electric field intensity and remains constant only for $\varepsilon_x < 10^3$ V/cm in n-type silicon. For moderate fields, 10^3 to 10^4 V/cm, the mobility is approximately inversely proportional to the square root of the applied field. For still higher fields, such as are encountered at pinch-off, μ_n is inversely proportional to ε_x. In this region the drift velocity of the electrons ($v_x = \mu_n\varepsilon_x$) remains constant, and Ohm's law is no longer valid. From Eq. (10.7) we now see that, both I_D and b remain constant, thus explaining the constant-current portion of the V-I characteristic of Fig. 10.3.

What happens[4] if V_{DS} is increased beyond pinch-off, with V_{GS} held constant? As explained above, the minimum channel width $b_{\min} = \delta$ has a small nonzero constant value. This minimum width occurs at the drain end of the bar. As V_{DS} is increased, this increment in potential causes an increase in $\mathcal{E}_x$ in an adjacent channel section toward the source. Referring to Fig. 10.6, the velocity-limited region L' increases with V_{DS}, whereas δ remains at a fixed value.

The Region before Pinch-off We have verified that the FET behaves as an ohmic resistance for small V_{DS} and as a constant-current device for large V_{DS}. An analysis giving the shape of the volt-ampere characteristic between these two extremes is complicated. It has already been mentioned that in this region the mobility is at first independent of electric field and then μ varies with $\mathcal{E}_x^{-1/2}$ for larger values of $\mathcal{E}_x$ (before pinch-off). Taking this relationship into account, it is possible[3–5] to obtain an expression for I_D as a function of V_{DS} and V_{GS} which agrees quite well with experimentally determined curves.

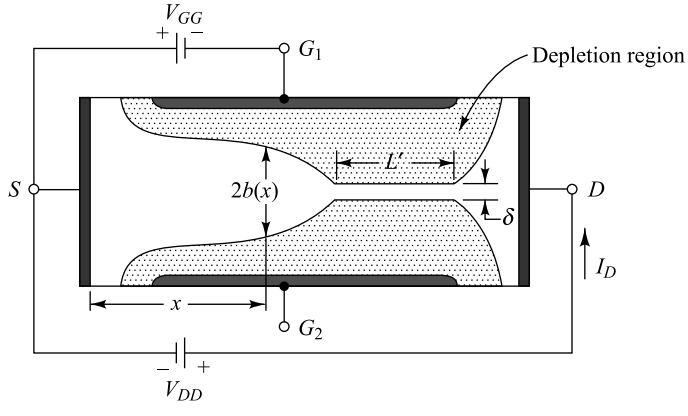


Fig. 10.6 *After pinch-off, as V_{DS} is increased, then L' increases but δ and I_D remain essentially constant. (G_1 and G_2 are tied together.)*

The Transfer Characteristic In amplifier applications the FET is almost always used in the region beyond pinch-off (also called the *constant-current*, *pentode*, or *current-saturation region*). Let the saturation drain current be designated by I_{DS}, and its value with the gate shorted to the source ($V_{GS} = 0$) by I_{DSS}. It has been found[6] that the transfer characteristic, giving the relationship between I_{DS} and V_{GS}, can be approximated by the parabola

$$I_{DS} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \tag{10.8}$$

This simple parabolic approximation gives an excellent fit, with the experimentally determined transfer characteristics for FETs made by the diffusion process.

Cutoff Consider an FET operating at a fixed value of V_{DS} in the constant-current region. As V_{GS} is increased in the direction to reverse-bias the gate junction, the conducting channel will narrow. When $V_{GS} = V_P$, the channel width is reduced to zero, and from Eq. (10.8), $I_{DS} = 0$. With a physical device some leakage current $I_{D,\text{OFF}}$ still flows even under the cutoff condition $|V_{GS}| > |V_P|$. A manufacturer usually specifies a maximum value of $I_{D,\text{ OFF}}$ at a given value of V_{GS} and V_{DS}. Typically, a value of a few nanoamperes may be expected for $I_{D,\text{ OFF}}$ for a silicon FET.

The gate reverse current, also called *the gate cutoff current*, designated by I_{GSS}, gives the gate-to-source current, with the drain shorted to the source for $|V_{GS}| > |V_P|$. Typically, I_{GSS} is of the order of a few nanoamperes for a silicon device.

10.4 The FET Small-signal Model

The linear small-signal equivalent circuit for the FET can be obtained in a manner analogous to that used to derive the corresponding model for a transistor. We employ the same notation in labeling time-varying and dc currents and voltages as used in Secs. 8.1 and 8.2 for the transistor. We can formally express the drain current i_D as a function f of the gate voltage v_{GS} and drain voltage v_{DS} by

$$i_D = f(v_{GS}, v_{DS}) \tag{10.9}$$

The Transconductance g_m and Drain Resistance r_d If both the gate and drain voltages are varied, the change in drain current is given approximately by the first two terms in the Taylor's series expansion of Eq. (10.9), or

$$\Delta i_D = \left.\frac{\partial i_D}{\partial v_{GS}}\right|_{V_{DS}} \Delta v_{GS} + \left.\frac{\partial i_D}{\partial v_{DS}}\right|_{V_{GS}} \Delta v_{DS} \tag{10.10}$$

In the small-signal notation of Sec. 8.1, $\Delta i_D = i_d$, $\Delta v_{GS} = \Delta v_{gs}$, and $v_{DS} = v_{dc}$, so that Eq. (10.10) becomes

$$i_d = g_m v_{gs} + \frac{1}{r_d} v_{ds} \tag{10.11}$$

where

$$g_m \equiv \left.\frac{\partial i_D}{\partial v_{GS}}\right|_{V_{DS}} \approx \left.\frac{\Delta i_D}{\Delta v_{GS}}\right|_{V_{DS}} = \left.\frac{i_d}{v_{gs}}\right|_{V_{DS}} \tag{10.12}$$

is the *mutual conductance*, or *transconductance*. It is also often designated by y_{fs} or g_{fs}, and called the (*common-source*) *forward transadmittance*. The second parameter r_d in Eq. (10.11) is the *drain* (or *output*) *resistance*, and is defined by

$$r_d \equiv \left.\frac{\partial v_{DS}}{\partial i_D}\right|_{V_{GS}} \approx \left.\frac{\Delta v_{DS}}{\Delta i_D}\right|_{V_{GS}} = \left.\frac{v_{ds}}{i_d}\right|_{V_{GS}} \tag{10.13}$$

The reciprocal of r_d is the drain conductance g_d. It is also designated by y_{os} and g_{os} and called the (common-source) output conductance.

An *amplification factor* μ for an FET may be defined by

$$\mu \equiv -\left.\frac{\partial v_{DS}}{\partial v_{GS}}\right|_{I_D} = -\left.\frac{\Delta v_{DS}}{\Delta v_{GS}}\right|_{I_D} = -\left.\frac{v_{ds}}{v_{gs}}\right|_{i_d = 0} \tag{10.14}$$

We can verify that μ, r_d, and g_m are related by

$$\mu = r_d g_m \tag{10.15}$$

by setting $i_d = 0$ in Eq. (10.11).

An expression for g_m is obtained by applying the definition of Eq. (10.12) to Eq. (10.8). The result is

$$g_m = g_{mo}\left(1 - \frac{V_{GS}}{V_P}\right) = \frac{2}{|V_P|}(I_{DSS} I_{DS})^{1/2} \tag{10.16}$$

where g_{mo} is the value of g_m for $V_{GS} = 0$, and is given by

$$g_{mo} = \frac{-2I_{DSS}}{V_P} \tag{10.17}$$

Since I_{DSS} and V_P are of opposite sign, g_{mo} is always positive. Note that the transconductance varies as the square root of the drain current. The relationship connecting g_{mo}, I_{DSS}, and V_P has been verified experimentally.[7] Since g_{mo} can be measured and I_{DSS} can be read on a dc milliammeter placed in the drain lead (with zero gate excitation), Eq. (10.17) gives a method for obtaining V_P.

The dependence of g_m upon V_{GS} is indicated in Fig. 10.6 for the 2N3277 FET (with $V_P \approx 4.5$ V) and the 2N3278 FET (with $V_P \approx 7$V). The linear relationship predicted by Eq. (10.16) is seen to be only approximately valid.

Temperature Dependence Curves of g_m and r_d versus temperature are given in Fig. 10.8. The drain current I_{DS} has the same temperature variation as does g_m. The principal reason for the negative temperature coefficient of I_{DS} is that the mobility decreases with increasing temperature.[8] Since this majority-carrier current decreases with temperature (unlike the bipolar transistor whose minority-carrier current increases with temperature), the troublesome phenomenon of *thermal runaway* (Sec. 9.9) is not encountered with field-effect transistors.

The FET Model A circuit which satisfies Eq. (10.11) is indicated in Fig. 10.9*a*. This low-frequency small-signal model has a Norton's output circuit with a dependent current generator whose current is proportional to the gate-to-source voltage. The proportionality factor is the transconductance g_m, which

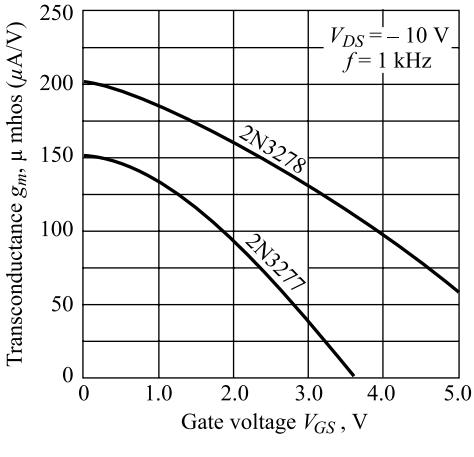


Fig. 10.7 *Transconductance g_m versus gate voltage for types 2N3277 and 2N3278 FETs. (Courtesy of Fairchild Semiconductor Company.)*

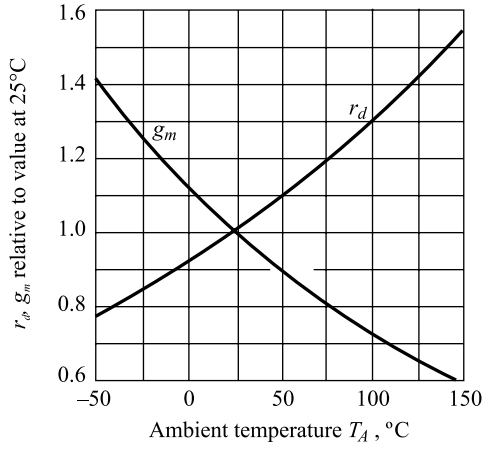


Fig. 10.8 *Normalized g_m and normalized r_d versus T_A (for the 2N3277 and the 2N3278 FETs with $V_{DS} = -10$ V, $V_{GS} = 0$ V, and $f = 1$ kHz). (Courtesy of Fairchild Semiconductor Company.)*

is consistent with the definition of g_m in Eq. (10.12). The output resistance is r_d, which is consistent with the definition in Eq. (10.13). The input resistance between gate and source is infinite, since it is assumed that the reverse-biased gate takes no current. For the same reason the resistance between gate and drain is assumed to be infinite.

The FET model of Fig.10.9*a* should be compared with the *h*-parameter model of the bipolar junction transistor of Fig. 8.6. The latter also has a Norton's output circuit, but the current generated depends upon the input *current*, whereas in the FET model the generator current depends upon the input *voltage*. Note that there is no feedback at low frequencies from output to input in the FET, whereas such feedback exists in the bipolar transistor through the parameter h_{re}. Finally, observe that the high (almost infinite) input resistance of the FET is replaced by an input resistance of about 1 K for a CE amplifier. In summary, the field-effect transistor is a much more ideal amplifier than the conventional transistor *at low frequencies*. Unfortunately, this is not true beyond the audio range, as we now indicate.

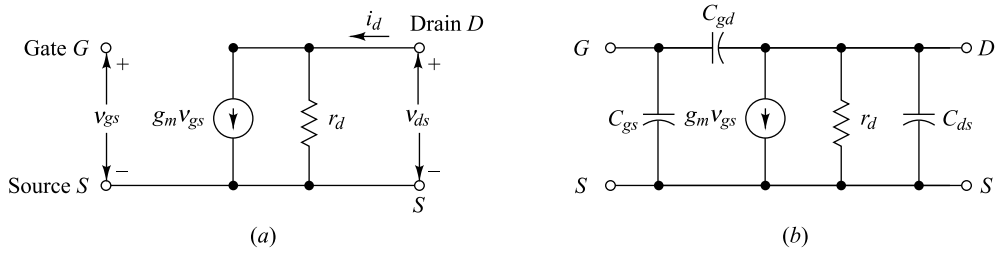


Fig. 10.9 *(a) The low-frequency small-signal FET model. (b) The high-frequency model, taking node capacitors into account.*

The high-frequency model given in Fig. 10.9*b* is identical with Fig. 10.9*a* except that the capacitances between pairs of nodes have been added. The capacitor C_{gs} represents the barrier capacitance between gate and source, and C_{gd} is the barrier capacitance between gate and drain. The element C_{ds}, represents the drain-to-source capacitance of the channel. Because of these internal capacitances, feedback exists between the input and output circuits, and the voltage amplification drops rapidly as the frequency is increased (Sec. 10.11). The order of magnitudes of the parameters in the model for a diffused-junction FET is given in Table 10.1.

Table 10.1 Range of parameter values for an FET

Parameter	*JFET*	*MOSFET†*
g_m	0.1–10 mA/V	0.1–20 mA/V or more
r_d	0.1–1 M	1–50 K
C_{ds}	0.1–1 pF	0.1–1 pF
C_{gs}, C_{gd}	1–10 pF	0.01–1 pF
r_{gs}	$> 10^8\ \Omega$	$> 10^{10}\ \Omega$
r_{gd}	$> 10^8\ \Omega$	$> 10^{14}\ \Omega$

† Discussed in Sec. 10.5.

10.5 The Metal-oxide-semiconductor FET (MOSFET)

In preceding sections we developed volt-ampere characteristics and small-signal properties of the junction field-effect transistor. We now turn our attention to the metal-oxide-semiconductor FET,[9] which is of much greater practical and commercial importance than the junction FET.

The *n*-channel MOSFET consists of a *p*-type substrate into which two highly doped n^+ regions are grown, as shown in Fig. 10.10. These n^+ sections, which will act as the source and drain, are separated by as little as 32 nm (in 2008). A thin (as thin as 12 to 15 Å) layer of insulating silicon dioxide (SiO_2) forms the gate insulator, on top of which is the poly-crystalline silicon (or metal) gate electrode. Metal contacts are made to the source, drain and gate terminals, to connect it to the rest of the circuit on the chip.

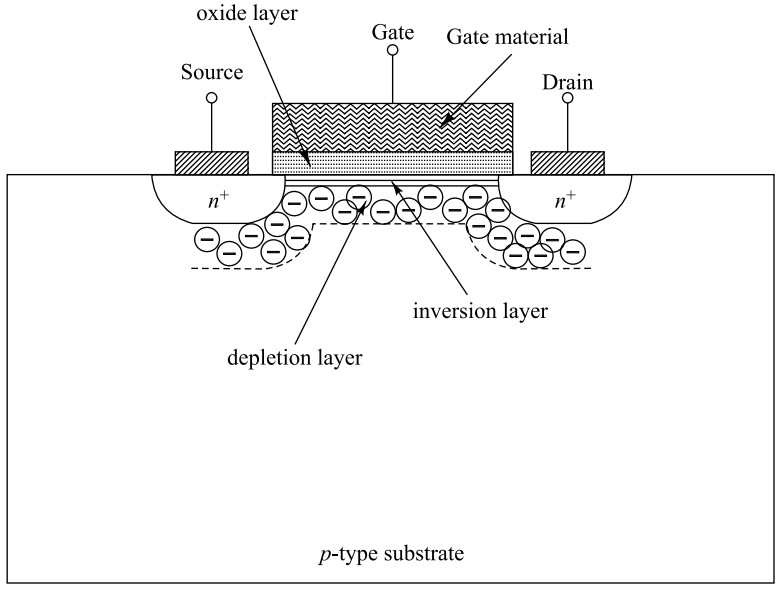


Fig. 10.10 *Schematic of an n-channel MOSFET.*

The gate-oxide-semiconductor form a parallel-plate capacitor. The insulating oxide layer results in an extremely high input resistance (10^{10} to 10^{15} Ω) for the MOSFET (when the gate us used as the input terminal). The area under the gate, in the semiconductor, is called the *channel* of the MOSFET. It is in the *channel* that carriers flow, from the source to the drain.

The MOSFET Structure If we ground the substrate for the structure in Fig. 10.10 and apply a positive voltage at the gate, an electric field will be directed perpendicularly through the oxide. For small magnitudes of the gate voltage, holes in the *p*-type substrate will be repelled away from the surface, leaving behind negative acceptor ions. As the magnitude of the gate voltage is increased, electrons will gradually start accumulating at the silicon-oxide interface, and form a layer of negative charges, called an 'inversion layer'. Now if a voltage is applied between the source and the drain, a current will flow, due to the inversion layer of electrons. The higher the magnitude of the gate voltage, the higher will be the electron charge at the interface, and the higher will be the current between the drain and source terminals. As in the JFET, as the drain-source voltage is increased, at a certain point, the channel *pinches off*, and the drain current becomes saturated.

A *p*-channel MOSFET will have an *n*-type substrate, p^+ source and drain regions, and a negative gate voltage will need to be applied to create an inversion layer of holes at the semiconductor surface. We will refer to the *n*-channel MOS transistor as an NMOSFET, and to the *p*-channel transistor as a PMOSFET.

Threshold Voltage The volt-ampere drain characteristics of an *N*MOSFET are given in Fig. 10.10*a*, and its transfer curve in Fig. 10.11*b*. As V_{GS} is made more positive, the current I_D increases slowly at first, and then much more rapidly with an increase in V_{GS}. The *threshold voltage* (V_T) of a MOSFET is defined as the gate-source voltage at which the drain current per unit width reaches some defined small value, say 10 μA. (In the literature, various definitions of V_T have been proposed, based on the physics of the MOSFET, or on practical requirements. The definition above is one of the more commonly used ones in the industry).

The magnitude of V_T for MOSFETs ranges between 0.3 and 5 V, depending on the channel length and oxide thickness (the lower these two are, the lower is the threshold voltage).

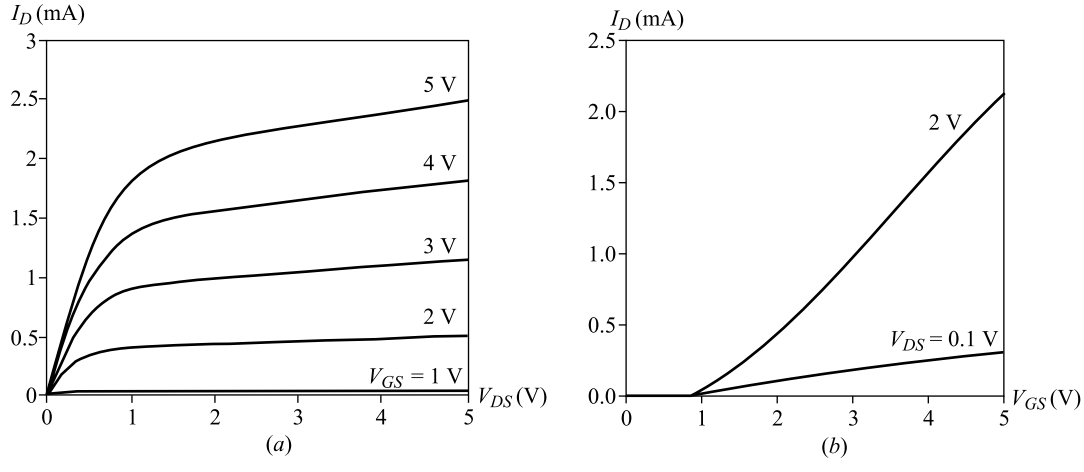


Fig. 10.11 *(a) Drain characteristics of an NMOSFET (b) Transfer characteristics.*

Comparison of *p*-with *n*-channel FETs The hole mobility at the silicon surface in a MOSFET is about 2.5 to 3 times smaller than the electron mobility. Thus *p*-channel devices will have more than twice the ON resistance of an equivalent *n*-channel device of the same geometry and under the same operating conditions. To put it another way, the *p*-channel device must have more than twice the area of the *n*-channel device to achieve the same resistance. The smaller size of the *n*-channel MOS also makes it faster while performing switching functions, and gives it a higher bandwidth in small-signal applications. Modern integrated circuits are invariably made in CMOS technology, which fabricates both NMOS and PMOS transistors on the same chip, and the sizing of *n*-channel and *p*-channel transistors is one of the primary challenges of the circuit designer.

MOSFET Gate Protection Since the insulating layer of the gate is extremely thin, it may easily be damaged by excessive voltage. An accumulation of charge on an open-circuited gate may result in a large enough field to cause breakdown in the dielectric. To prevent this damage, MOS devices that will come in contact with the outside world (as opposed to *core* devices inside an IC chip) are often fabricated with a Zener diode between the gate and source/substrate. In normal operation this diode is open and has no effect upon the circuit. However, if the voltage at the gate becomes excessive, then the diode breaks

down and the gate potential is limited to a maximum value equal to the Zener voltage. Modern ICs often have elaborate circuits to protect against damage that can be caused by excessive electrostatic charge, and are referred to as electro-static discharge (ESD) protection circuits.

Circuit Symbols The various circuit symbols used for the PMOSFET are shown in Fig. 10.12. When the substrate terminal is omitted from the symbol as in (*a*), it is understood to be connected to the source internally. It is possible to bring out the connection to the substrate externally so as to have a four-terminal device. Most MOSFETs on an IC, however, have the substrate connected to the highest (lowest) voltage in the circuit, if it is a *p*-channel (*n*-channel) device, because the substrate is typically common for all devices of one type, and one does not want any of the diodes formed by the substrate-source or substrate-drain junctions to turn on during circuit operation. To connect the substrate of a particular transistor to a voltage other than the highest (lowest), a separate well will have to be created for it, which is extremely expensive in terms of area, and therefore is done only in very special cases, when such a bias is absolutely needed for the circuit. The corresponding symbols for an NMOSFET will have the arrow direction reversed.

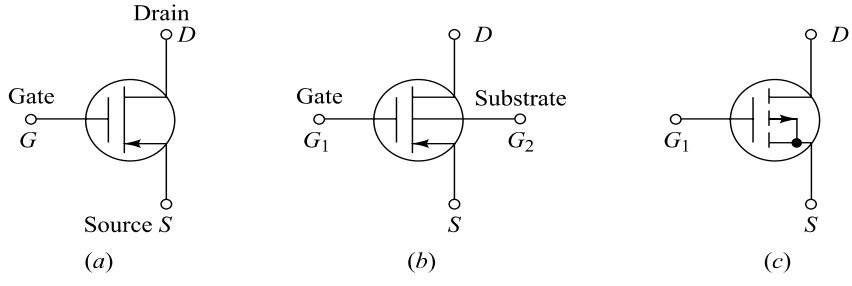


Fig. 10.12 *Three circuit symbols for a p-channel MOSFET (a) and (b) can be either depletion or enhancement types, whereas (c) represents specifically an enhancement device. In (a) the substrate is understood to be connected internally to the source. For an n-channel MOSFET the direction of the arrow is reversed.*

MOSFET Equations The physics of a modern-day MOSFET, with channel lengths as small as 32 nm, is extremely complex, and beyond the scope of this book. We present here a simple mathematical model describing the current-voltage characteristics of the MOSFET, which are more appropriate for long-channel devices (channel lengths longer than 2 μm), but are used universally, for performing paper analysis of both digital and analog circuits.

The model divides the current-voltage characteristics into three regions of operation. For an NMOS transistor,

Cutoff region

for $V_{GS} < V_T$

$$I_D = 0 \qquad (10.18a)$$

for $V_{GS} > V_T$

Triode, or linear, region

$$I_D = \frac{\mu_n C_{ox} W}{L}\left(V_{GS} - V_T - \frac{1}{2}V_{DS}\right)V_{DS} \quad \text{if} \quad V_{DS} \le (V_{GS} - V_T) \qquad (10.18b)$$

Saturation region

$$I_D = \frac{\mu_n C_{ox} W}{2L}(V_{GS} - V_T)^2 \quad \text{if} \quad V_{DS} \geq (V_{GS} - V_T) \tag{10.18c}$$

In the above equations, μ_n is the electron mobility, C_{ox} is the gate-oxide capacitance per unit area ($= \epsilon_0 \epsilon_{ox}/t_{ox}$, ϵ_0 is the dielectric permittivity of vacuum, ϵ_{ox} is the relative dielectric permittivity of the gate oxide material, and t_{ox} is the gate oxide thickness), W is the width of the channel, L is the length of the channel, and I_D is the current *entering* the drain terminal. The triode and saturation region are similar to the linear and saturation regions of the JFET.

For a PMOS transistor, the equations remain the same, except that the drain current is defined to be *leaving* the terminal, and all the inequalities are reversed. For the sake of completeness, and because these equations are so fundamental to circuit analysis, we write the PMOS equations below, with I_D defined as the current leaving the drain terminal.

Cutoff region

for $V_{GS} > V_T$ (or, $V_{SG} < |V_T|$)

$$I_D = 0 \tag{10.19a}$$

for $V_{GS} < V_T$ (or, $V_{SG} > |V_T|$)

Triode, or linear, region

$$I_D = \frac{\mu_n C_{ox} W}{L}\left(V_{GS} - V_T - \frac{1}{2}V_{DS}\right)V_{DS} \quad \text{if} \quad V_{DS} \geq (V_{GS} - V_T) \tag{10.19b}$$

Saturation region

$$I_D = \frac{\mu_n C_{ox} W}{2L}(V_{GS} - V_T)^2 \quad \text{if} \quad V_{DS} \leq (V_{GS} - V_T) \tag{10.19c}$$

If channel length modulation is included then the last equation is modified as follows:

$$I_D = \frac{\mu_n C_{ox} W}{n}(V_{GS} - V_T)^2 [1 + \lambda(V_{DS} - V_{DS,\,sat})] \tag{10.19d}$$

where λ is a constant, and $V_{DS,\,sat} = (V_{as} - V_T)$.

Small-signal MOSFET Circuit Model[11] If the small resistances of the source and drain regions are neglected, the small-signal equivalent circuits of the MOSFET are shown in Fig. 10.13. Note that the low-frequency circuit is identical with that of a JFET (shown in Fig. 10.9(*a*)). The high-frequency model of Fig. 10.13*b* is shown with the substrate terminal shorted to the source. If this is not the case, then there will be one more capacitance, C_{sb} between the source and substrate, and C_{db} will appear between the drain and substrate terminals.

Expressions for g_m and r_d can be obtained using Eqs (10.12), (10.13), and (10.19). Thus, in saturation, using Eq. (10.19*c*),

$$g_m = \frac{\partial i_D}{\partial v_{DS}} = \frac{\mu_n C_{ox} W}{L}(V_{GS} - V_T) = \sqrt{2\frac{\mu_n C_{ox} W}{L} I_D} = \frac{2I_D}{(V_{GS} - V_T)} \tag{10.20a}$$

and using Eq. (10.19d),

$$rd^{-1} = \frac{\partial i_D}{\partial v_{DS}} = \frac{\mu_n C_{ox} W}{L}(V_{GS} - V_T)^2 \;\; \lambda = \lambda I_D, \text{ or } r_d = \frac{1}{\lambda I_D} \tag{10.20b}$$

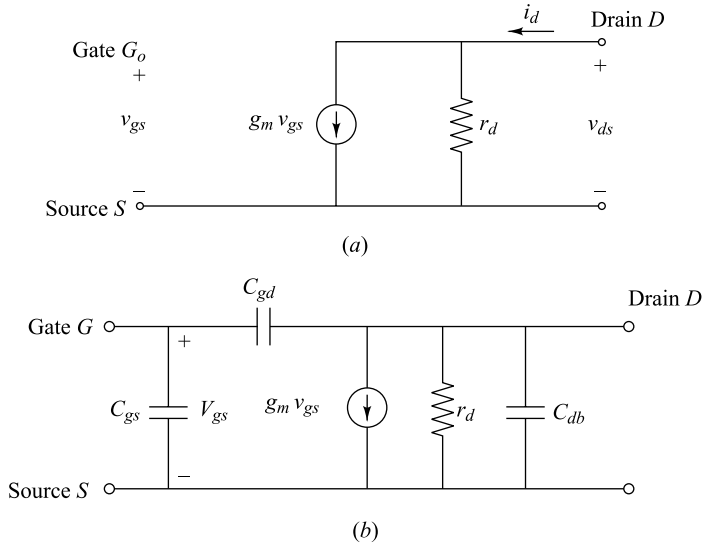


Fig. 10.13 *(a) The low-frequency small-signal MOSFET model. (b) The high-frequency model, taking node capacitors into account.*

Example The MOSFET in Fig. 10.14 has $V_T = 1$ V, and $\mu_n C_{ox}(W/L) = 1$ mA/V^2. Determine the drain current and the drain voltage, for the following cases:

(*a*) $V_G = 0.5$ V, $R_D = 1$ kΩ.
(*b*) $V_G = 2$ V, $R_D = 1$ kΩ.
(*c*) $V_G = 2$ V, $R_D = 10$ kΩ.

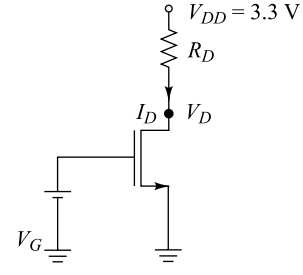


Fig. 10.14 *MOSFET dc analysis.*

Solution (*a*) If $V_G = 0.5$ V, then $(V_{GS} - V_T) = 0.5 - 1 = -0.5$ V, which is less than zero, and therefore, from Eq. (10.18*a*), the transistor will be off. Then,

$$I_D = 0$$

and

$$V_D = V_{DD} = 3.3 \text{ V}$$

(*b*) $(V_{GS} - V_T) = 2 - 1 = 1$ V. Therefore, the transistor is on. Let us assume that the transistor is in saturation. Then from Eq. (10.18*c*),

$$I_D = \frac{\mu_n C_{ox} W}{2L}(V_{GS} - V_T)^2 = \frac{1}{2}(2-1)^2 = 0.5 \text{ mA}$$

and

$$V_D = V_{DD} - R_D I_D = 3.3 - (0.5)(1) = 2.8 \text{ V}$$

Now let us check our assumption of saturation. For saturation,

$$V_{GS} - V_T \le V_{DS}$$

or,

$$2 - 1 \le 2.8$$

which is true. Hence the transistor *is* in saturation.

(*c*) Proceeding as in part (*b*) above, and assuming the transistor in saturation, we find

$$I_D = 0.5 \text{ mA}$$

Then,

$$V_D = V_{DD} - R_D I_D = 3.3 - (0.5)\,(10) = -1.7 \text{ V}$$

Since V_D is negative, clearly $(V_{GS} - V_T)$ is not less than V_{DS}, and therefore the transistor is *not* in saturation. Then it must be in the triode region. Using Eq. (10.18*b*) yields

$$I_D = \frac{\mu_n C_{ox} W}{L}\left(V_{GS} - V_T - \frac{1}{2}V_{DS}\right)V_{DS}$$

$$= 1\left(2 - 1 - \frac{1}{2}V_D\right)V_{DS}$$

$$I_D = \left(1 - \frac{1}{2}V_D\right)V_D$$

We have two unknowns and one equation. We obtain the other equation from R_D:

$$V_{DD} - V_D = R_D I_D$$

or,

$$3.3 - V_D = 10\, I_D$$

Substituting for I_D into the previous equation yields

$$\frac{3.3 - V_D}{10} = \left(1 - \frac{1}{2}V_D\right)V_D$$

or,

$$5V_D^2 - 11V_D + 3.3 = 0$$

Solving for V_D yields

$$V_D = 1.84 \text{ V or } 0.36 \text{ V}$$

Since the transistor is in the triode region, V_D must be less than $(V_{GS} - V_T) = 1$ V. Therefore,

$$V_D = 0.36 \text{ V}$$

Then,

$$I_D = \frac{3.3 - V_D}{10} = 0.29\text{mA}$$

The following points are worth noting about the circuit of Fig. 10.14:

- As the drain resistance is increased, the drain voltage decreases, eventually driving the transistor out of saturation.
- For a given gate voltage and drain resistance, if the transistor size (W) is increased, the drain current will increase; and once again, the transistor will come out of saturation for a large enough W.
  (Both the above can be more simply thought of as consequences of regarding the MOSFET as a resistor – albeit a non-linear one).
- As long as the transistor stays in saturation, the drain current stays constant (neglecting channel length modulation). irrespective of the value of the drain resistace. Thus, in saturation, the MOSFET acts like a current source.

Example The transistor in Fig. 10.15 has $V_T = 1$ V and $\mu_n C_{ox}(W/L) = 2$ mA/V^2. Determine the drain voltage.

Solution As in the previous example, let us begin with the assumption that the transistor is in saturation. Then

$$I_D = \frac{\mu_n C_{ox} W}{2L}(V_{GS} - V_T)^2 = \frac{2}{2}(1.8 - V_S - 1)^2 \text{ mA}$$

or,

$$I_D = (0.8 - V_S)^2$$

For the source resistor,

$$V_S = 0.5\, I_D \text{ (with } I_D \text{ in mA)}$$

Substituting for I_D in the previous equation yields

$$2V_S = (0.8 - V_S)^2 = V_S^2 - 1.6V_S + 0.64$$

Solving for V_S yields,

$$V_S = 0.2 \text{ V or } 3.4 \text{ V}$$

For the transistor to be on, $V_{GS} > V_T$, or $(1.8 - V_S) > 1$, or $V_S < 0.8$ V. Therefore,

$$V_S = 0.2 \text{ V}$$

Then

$$I_D = 2\, V_S = 0.4 \text{ mA}$$

and

$$V_D = 3.3 - (1)\,(0.4) = 2.9 \text{ V}$$

We check if the transistor is in saturation:

$$V_{GS} - V_T \le V_{DS}$$

or,

$$1.8 - 0.2 - 1 \le 2.9 - 0.2$$

or,

$$0.6 \le 2.7$$

which is true. Hence the transistor *is* in saturation.

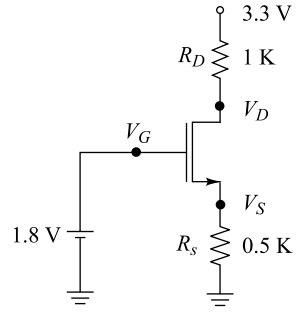


Fig. 10.15 *MOSFET circuit with a source resistor.*

Example Solve the above example again, but with $R_D = 10$ kΩ, and everything else remaining the same.

Solution Proceeding as in the last example, and assuming the transistor in saturation, we conclude that

$$V_S = 0.2 \text{ V}$$

and

$$I_D = 0.4 \text{ mA}$$

Then, with $R_D = 10$ kΩ

$$V_D = 3.3 - (10)\,(0.4) = -0.7 \text{ V}$$

V_D obviously cannot be negative (and it also leads to the condition for saturation not being satisfied), therefore the transistor must be in the triode region. So we start again with Eq. (10.18*b*):

$$I_D = \frac{\mu_n C_{ox} W}{L}\left(V_{GS} - V_T - \frac{1}{2}V_{DS}\right)V_{DS}$$

$$= 2\left(1.8 - V_S - 1 - \frac{(V_D - V_S)}{2}\right)(V_D - V_S)$$

$$I_D = 2(0.8 - 0.5V_S - 0.5V_D)(V_D - V_S)$$

For the source resistance,

$$V_S = 0.5\, I_D$$

and for the drain resistance

$$V_D = 3.3 - 10\, I_D$$

Substituting for V_S and V_D in the I_D equation yields,

$$I_D = 2[0.8 - 0.5 \times 0.5\, I_D - 0.5(3.3 - 10\, I_D)](3.3 - 10\, I_D - 0.5\, I_D)$$
$$= 2(7.15 + 4.75\, I_D)(3.3 - 10.5\, I_D)$$

Solving the quadratic equation for I_D yields

$$I_D = 0.31 \text{ mA} \text{ or } -1.52 \text{ mA}$$

I_D cannot be negative (for the given bias voltages); therefore,

$$I_D = 0.31 \text{ mA}$$

Then,

$$V_S = 0.155 \text{ V}$$

and

$$V_D = 0.2 \text{ V}$$

and

$$V_{DS} = 0.045 \text{ V}$$

which is less than $(V_{GS} - V_T) = (1.8 - 0.155 - 1) = 0.645$ V, thus confirming that the transistor is in the triode region.

Example *The CMOS amplifier*: Determine the drain current and drain voltage in the circuit of Fig. 10.16, if

(*a*) $V_{G1} = 1$ V, $V_{G2} = 2$ V

(*b*) $V_{G1} = 1$ V, $V_{G2} = 2.3$ V

For the NMOS transistor: $V_T = 0.7$ V and $\mu_n C_{ox}(W/L) = 2$ mA/V^2, and

For the PMOS transistor: $V_T = -0.7$ V and $\mu_p C_{ox}(W/L) = 2$ mA/V^2.

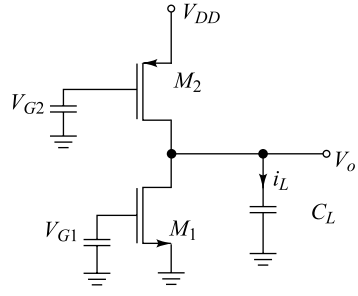


Fig. 10.16 *CMOS inventer amplifier.*

Solution (*a*) If we assume both transistors in saturation, then

$$I_{D1} = \frac{\mu_n C_{ox} W}{2L}(V_{GS1} - V_{Tn})^2 = \frac{2}{2}(1 - 0.7)^2 = 0.09 \text{ mA}$$

and

$$I_{D2} = \frac{\mu_p C_{ox} W}{2L}(V_{GS2} - V_{Tp})^2 = \frac{2}{2}(3.3 - 2 - 0.7)^2 = 0.36 \text{ mA}$$

With both the gate currents being zero, the drain currents have to be equal to satisfy KCL. Since the saturation currents of the two transistors are not equal, both transistors cannot be in saturation simultaneously. Now for a given gate-source voltage, the highest current a MOSFET can carry is the saturation current. Thus the NMOS, which has a saturation current of 0.09 mA, can never carry 0.36 mA. Hence the PMOS transistor cannot be in saturation.

Hence let us try the assumption that the NMOS is in saturation, and the PMOS in triode. Then,

$$I_{D1} = 0.09 \text{ mA} = I_{D2} = \frac{\mu_p C_{ox} W}{L}\left(V_{GS2} - V_{Tp} - \frac{1}{2}V_{DS2}\right)V_{DS2}$$
$$= 2\left(2 - 3.3 + 0.7 - \frac{(V_D - 3.3)}{2}\right)(V_D - 3.3)$$
$$0.09 = (V_D - 2.1)(3.3 - V_D)$$

Therefore,

$$V_D = 3.22 \text{ V or } 2.18 \text{ V}$$

$V_D = 2.18$ V will put the PMOS in saturation. Therefore,

$$V_D = 3.22 \text{ V}$$

which puts the PMOS in the triode region, and the NMOS in saturation. Note that if neither value of V_D had satisfied this condition, then both transistors would have to be in the triode region.

(*b*) $V_{G1} = 1$ V, $V_{G2} = 2.3$ V

Assuming both transistors in saturation, we find

$$I_{D1} = 0.09 \text{ mA, as in (a) above,}$$

and

$$I_{D2} = \frac{\mu_p C_{ox} W}{2L}(V_{GS2} - V_{Tp})^2 = \frac{2}{2}(3.3 - 2.3 - 0.7)^2 = 0.09 \text{ mA}$$

Therefore,

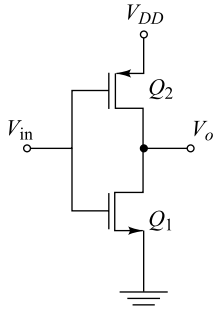
$$I_{D1} = I_{D2}$$

Hence both transistors are in saturation. What is the drain voltage? With Eq. (10.18*c*) as our model for I_D in saturation, both the MOSFETs behave like ideal current sources. For such a circuit, the voltage at the junction of the two current sources is indeterminate. To find V_D, we would have to include the effect of channel length modulation in the MOSFET drain current equation.

10.6 Digital MOSFET Circuits[12]

In this section, we look at the very basic digital gate construction with MOSFETs. Registers and memory arrays made with MOSFETs are discussed in Chap. 17.

Inverter Figure 10.17*a* shows a CMOS inverter, which is the most fundamental building block of CMOS digital circuits. Figure 10.17*b* shows its truth table. Figure 10.18 shows the output characteristics of the NMOS and PMOS transistors used in the inverter. This figure can be used to construct the transfer characteristics (v_O vs. v_I) of the inverter circuit, as we now do. Figure 10.19 shows these v_O vs. v_I characteristics. It also shows the drain current variation as the input voltage is varied.



(*a*)

V_{in}	V_o
0	V_{DD}
V_{DD}	0

(*b*)

Fig. 10.17 *The CMOS inverter (a) Circuit diagram (b) Truth table.*

For convenience, we will assume that the NMOS and PMOS transistors have equal magnitudes of threshold voltages (V_T), and they also have equal values of the quantity ($\mu C_{ox} W/L$). Such an inverter is called a *symmetric* inverter. For very small input voltages (less than the threshold voltage), the NMOS transistor will be in cutoff, and therefore will carry no current. The PMOS transistor is ON, because its source-gate voltage is greater than its threshold voltage, but no current flows through it (since the NMOS is cutoff). Thus the PMOS acts like a short-circuit between V_{DD} and v_O, and the output voltage is equal to V_{DD}. As the drain-source voltage of the PMOS is zero, it is in the triode region. Now as the input voltage is increased, as it crosses V_T, the NMOS transistor turns on, and current starts flowing through it. For v_{IN} only slightly greater than V_T, the PMOS transistor stays in

the triode region, and the NMOS transistor will be in saturation. As v_{IN} increases, the drain current increases, and the voltage drop across the PMOS increases, thus reducing the output voltage. At some point, the PMOS transistor will enter saturation. With both transistors in saturation, as the plots in Figure 10.18 indicate, the operating point is found by the intersection of two nearly-horizontal lines. Thus even a small change in v_{IN} brings about a large change in the output voltage, and thus the transfer characteristic falls rapidly in this region, until v_O becomes small enough that the NMOS transistor goes out of saturation, and enters the triode region. v_O now reduces less rapidly (similar to the condition when the PMOS was in triode), until v_O becomes large enough that the V_{GS} of the PMOS becomes less that its V_T, and it turns off.

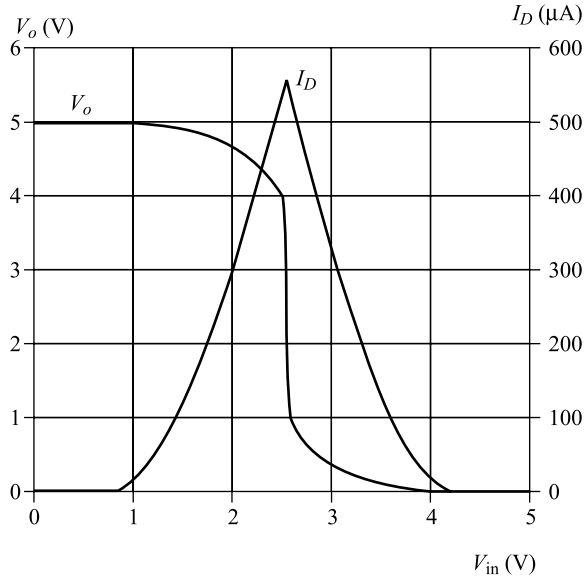


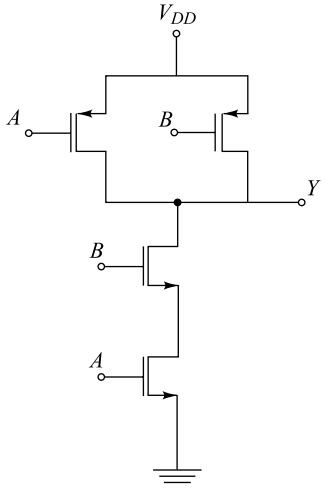
Fig. 10.18 *CMOS inverter characteristics*

The exact shape of the characteristics shown in Fig. 10.18 can be derived by solving the current equations for the NMOS and PMOS simultaneously, with the condition that both the drain currents are equal. When used as a digital inverters, the input voltage applied to this circuit will either be less than V_T, or greater than $(V_{DD} - V_T)$. This means that, as is indicated in the I_D curve in Fig. 10.18, no current flows in the circuit when the input applied is either HIGH or LOW. Thus the CMOS inverter dissipates no power when the input is not changing. It consumes power only when the input is changing from one state to another. As a result, the dc power consumption is negligibly small. It is for this reason *primarily* that it is possible to build integrated circuits with billions of MOS transistors on a single chip; because if a gate consumed dc power, then putting so many gates on a single chip will generate so much heat, even when the circuit was not doing anything, that that small piece of silicon will burn out in no time!

Modern CMOS inverters operate with nanowatts of dc power consumption, and have a switching time of a few tens of picoseconds.

NAND Gate Figure 10.19 shows the circuit, and truth table, of a static CMOS NAND gate. Once the inverter circuit above is understood well, it is very easy to understand all other CMOS logic gates. In Figure 10.20, when the inputs A and B are HIGH (or 1), both the NMOS transistors are ON, and both the PMOS transistors are OFF. Thus the output is shorted to ground, through the two NMOS transistors, and

therefore is LOW (or 0). If at least one of the inputs is low, then at least one of the NMOS transistors is OFF (so that there is no path from the output to ground), and simultaneously, at least one PMOS transistors is ON (so that there is a path from V_{DD} to the output), and therefore the output is equal to V_{DD}.



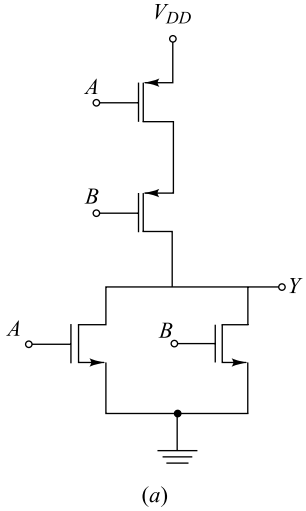
(a)

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

(b)

Fig. 10.19 *A CMOS NAND Gate (a) Circuit diagram, (b) truth table.*

NOR Gate Figure 10.20 shows the circuit of a static CMOS NOR gate. In this figure, when both the inputs *A* and *B* are LOW (or 0), both the PMOS transistors are ON, and both the NMOS transistors are OFF. Thus the output is shorted to V_{DD}, through the two PMOS transistors, and therefore is HIGH (or 1). If at least one of the inputs is HIGH, then at least one of the PMOS transistors is OFF (so that there is no path from the output to V_{DD}), and simultaneously, at least one NMOS transistors is ON (providing a path from ground to the output), and therefore the output is zero (or LOW).



(a)

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

(b)

Fig. 10.20 *A CMOS NOR Gate (a) Circuit diagram, (b) truth table.*

Example For the inverter circuit of Fig. 10.17*a*, determine the input voltage for which both transistors are in saturation. Assume the transistors to be symmetric, that is, $V_{Tn} = -V_{Tp}$, and $\mu_n C_{ox}(W/L) = \mu_p C_{ox}(W/L)$. Also assume that $\lambda_n = \lambda_p = 0$.

Solution When $V_O = V_{DD}/2$, both transistors will be in saturation, as we have discussed above. We therefore write, under this condition,

$$I_{Dn,sat} = I_{Dp,sat}$$

or,

$$\frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)_n (V_{GSn} - V_{Tn})^2 = \frac{\mu_p C_{ox}}{2}\left(\frac{W}{L}\right)_p (V_{GSp} - V_{Tp})^2$$

Cancelling the (equal) prefactors, and substituting for various voltages, yields,

$$(V_{in} - V_{Tn})^2 = (V_{in} - V_{DD} + V_{Tn})^2$$

or,

$$(V_{in} - V_{Tn}) = \pm(V_{in} - V_{DD} + V_{Tn})$$

Therefore,

$$(V_{in} - V_{Tn}) = (V_{in} - V_{DD} + V_{Tn}) \qquad \text{or} \qquad (V_{in} - V_{Tn}) = -(V_{in} - V_{DD} + V_{Tn})$$

That is,

$$V_{Tn} = \frac{V_{DD}}{2} \qquad \text{or} \qquad V_{in} = \frac{V_{DD}}{2}$$

The first of the two equations is meaningless, because both V_{Tn} and V_{DD} are both known constants. Hence,

$$V_{in} = \frac{V_{DD}}{2}.$$

Stated in words, the above results says that for a symmetric inverter, the two transistors are in saturation when the input voltage is half of V_{DD}.

Example Repeat the above example if the transistors are *not* symmetric. Assume $\lambda_n = \lambda_p = 0$.

Solution We again write

$$I_{Dn,sat} = I_{Dp,sat}$$

or,

$$\frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)_n (V_{GSn} - V_{Tn})^2 = \frac{\mu_p C_{ox}}{2}\left(\frac{W}{L}\right)_p (V_{GSp} - V_{Tp})^2$$

or

$$(V_{in} - V_{Tn})^2 = \frac{\mu_n \left(W/L\right)_n}{\mu_p \left(W/L\right)_p}(V_{in} - V_{DD} - V_{Tp})^2$$

or

$$(V_{in} - V_{Tn}) = \pm\alpha(V_{in} - V_{DD} - V_{Tp})$$

where

$$\alpha = \frac{\mu_n \left(W/L\right)_n}{\mu_p \left(W/L\right)_p}$$

Therefore,

$$(V_{in} - V_{Tn}) = \alpha(V_{in} - V_{DD} - V_{Tp}) \qquad \text{or} \qquad (V_{in} - V_{Tn}) = -\alpha(V_{in} - V_{DD} - V_{Tp})$$

That is,

$$V_{\text{in}} = \frac{V_{Tn} - \alpha(V_{DD} + V_{Tp})}{(1-\alpha)} \qquad \text{or} \qquad V_{\text{in}} = \frac{V_{Tn} + \alpha(V_{DD} + V_{Tp})}{(1+\alpha)}$$

Given that the expression for V_{in} must be valid for all possible values of α, the second equation has to be the correct one, because the first one (obviously) does not work for $\alpha = 1$ (as we also saw in the previous example).

Plotting the above expression as a function of α, and of $(V_{Tn} - |V_{Tp}|)$, would show that the input voltage at which both transistors are in saturation increases as α increases, and it also increases as the difference $(V_{Tn} - |V_{Tp}|)$ increases.

Example *Propagation delay of an inverter*: In the CMOS inverter of Fig. 10.17(a), let a load capacitance C_L be connected between the output node and ground. If the input voltage goes from high to low abruptly, calculate the time taken by the output to reach $V_{DD}/2$ (from 0). This time is called the *propagation delay* (τ_p). Assume that the transistors switch instantaneously, and that M_2 is in saturation for the entire duration.

Solution As V_{in} goes from V_{DD} to 0, V_o will go from 0 to V_{DD}. Thus initially (before V_{in} is switched), C_L will be uncharged. When V_{in} switches to 0, M_1 turns off, M_2 turns on, and C_L starts charging through the drain current of M_2. For $V_o$varying from 0 to $V_{DD}/2$, we assume that M_2 will remain in saturation. Then we write

$$I_{Dp,\text{sat}} = i_L = C_L \frac{dV_o}{dt}$$

or,

$$\int_o^{V_{DD}/2} dV_o = \frac{1}{C_L} \int_0^{\tau} I_{Dp,\text{sat}}\, dt$$

In saturation, $I_{Dp,\text{sat}}$ is constant, so we get, after integration,

$$\frac{V_{DD}}{2} = \frac{\tau_p I_{Dp,\text{sat}}}{C_L}$$

or,

$$\tau_p = \frac{C_L V_{DD}}{2 I_{Dp,\text{sat}}}$$

A similar propagation delay can be derived for the input going from 0 to V_{DD}, when C_L will discharge from V_{DD} to 0, through the NMOS transistor. That delay will turn out, by symmetry, to be

$$\tau_p = \frac{C_L V_{DD}}{2 I_{Dn,\text{sat}}}$$

The first delay is referred to as the low-to-high delay (referring to the output going from low to high), and is written as $\tau_{p,LH}$, while the second delay is referred to as the high-to-low delay, and is written as $\tau_{p,HL}$.

10.7 The Low-frequency Common-Source and Common-drain Amplifiers

The common-source (CS) stage is indicated in Fig. 10.21*a*, and the common-drain (CD) configuration in Fig. 10.21*b*. The former is analogous to the bipolar transistor CE amplifier, and the latter to the CC stage. We shall analyze both of these circuits simultaneously by considering the generalized configuration in Fig. 10.22*a*. For the CS stage the output is v_{a1} taken at the drain and $R_s = 0$. For the CD stage the output is v_{o2} taken at the source and $R_d = 0$. The signal-source resistance is unimportant since it is in series with the gate, which draws negligible current. No biasing arrangements are indicated (Sec. 10.8), but it is assumed that the stage is properly biased for linear operation.

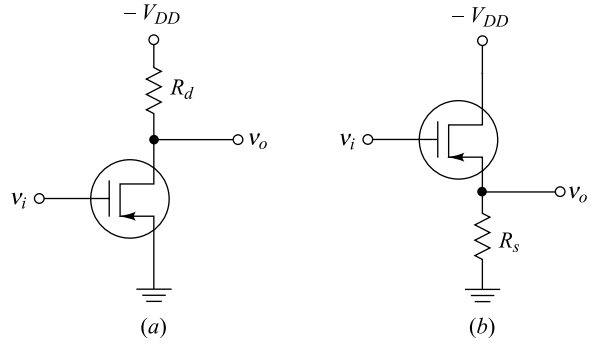


Fig. 10.21 (*a*) *The CS ond* (*b*) *the CD configurations.*

Replacing the FET by its low-frequency small-signal model of Fig. 10.9, the equivalent circuit of Fig. 10.22*b* is obtained. Applying KVL to the output circuit yields

$$i_d R_d + (i_d - g_m v_{gs}) r_d + i_d R_s = 0 \tag{10.21}$$

From Fig. 10.22*b* the voltage from *G* to *S* is given by

$$v_{gs} = v_i - i_d R_s \tag{10.22}$$

Combining Eqs (10.21) and (10.22) and remembering that $\mu = r_d g_m$ [Eq. (10.15)], we find

$$i_d = \frac{\mu v_i}{r_d + R_d + (\mu + 1) R_s} \tag{10.23}$$

The CS Amplifier with an Unbypassed Source Resistance Since $v_{o1} = -i_d R_d$, then

From Eq. (10.24) we obtain the Thévenin's equivalent circuit of Fig. 10.23*a* "looking into" the drain node (to ground). The open-circuit voltage is $-\mu v_i$, and the output resistance is $R_o = r_d + (\mu + 1)R_s$. The voltage gain is $A_V = v_{o1}/v_i$. The minus sign in Eq. (10.24) indicates that the output is 180° out of phase with the input. If R_s is bypassed with a large capacitance or if the source is grounded, the above equations are valid with $R_s = 0$. Under these circumstances,

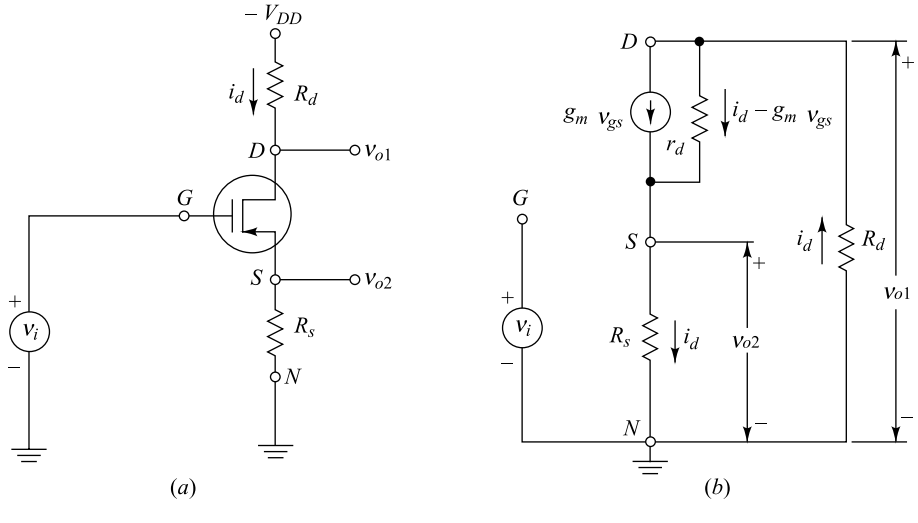


Fig. 10.22 (*a*) *A generalized FET amplifier configuration.* (*b*) *The small-signal equivalent circuit.*

$$A_V = \frac{v_{o1}}{v_i} = \frac{-\mu R_d}{r_d + R_d} = -g_m R'_d \tag{10.24}$$

where $\mu = r_d g_m$ [Eq. (10.15)] and $R'_d = R_d \| r_d$.

$$v_{o1} = \frac{-\mu v_i R_d}{r_d + R_d + (\mu + 1)R_s} \tag{10.25}$$

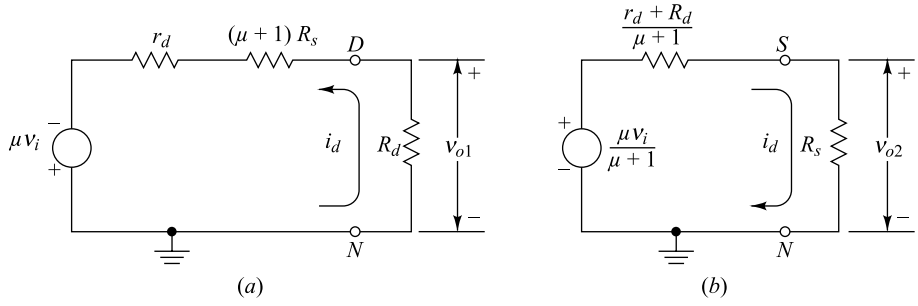


Fig. 10.23 *The equivalent circuits for the generalized amplifier of Fig. 10.22 "looking into" (a) the drain and (b) the source. Note that* $\mu = r_d g_m$.

The CD Amplifier with a Drain Resistance Since $v_{o2} - i_d R_s$, then from Eq. (10.23)

$$v_{o2} = \frac{\mu v_i R_s}{r_d + R_d + (\mu + 1)R_s} = \frac{[\mu v_i /(\mu + 1)]R_s}{(r_d + R_d)/(\mu + 1) + R_s} \tag{10.26}$$

From Eq. (10.26) we obtain the Thévenin's equivalent circuit of Fig. 10.23*b* "looking into" the source node (to ground). The open-circuit voltage is $\mu v_i/(\mu + 1)$, and the output resistance is $R_o = (r_d + R_d)/(\mu + 1)$. The voltage gain is $A_V = v_{o2}/v_i$. Note that there is no phase shift between input and output. If $R_d = 0$ and if $(\mu + 1)R_s >> r_d$, then $A_V \approx \mu/(\mu + 1) \approx 1$ for $\mu >> 1$. A voltage gain of unity means that the output (at the source) follows the input (at the gate). Hence the CD configuration is called a *source follower* (analogous to the *emitter* follower for a bipolar junction transistor).

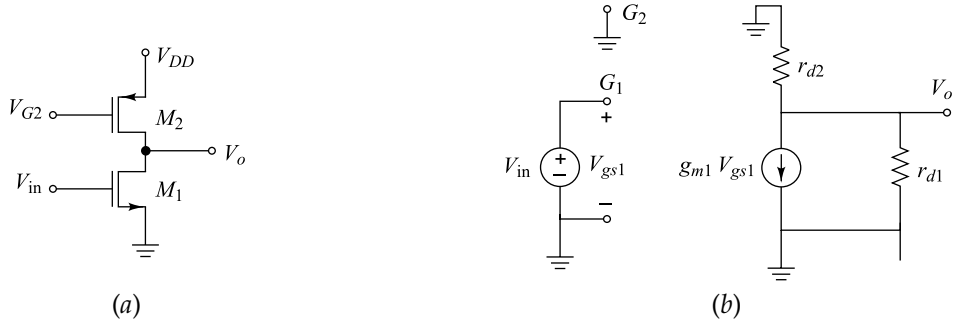
Note that the open-circuit voltage and the output impedance in either Fig. 10.23*a* or *b* are independent of the load (R_d in Fig. 10.23*a* and R_s in Fig. 10.23*b*). These restrictions must be satisfied if the networks in Fig. 10.23 are to represent the true Thévenin equivalents of the amplifier in Fig. 10.22.

For the source follower ($R_d = 0$) with $\mu >> 1$, the output conductance is

$$g_o = \frac{1}{R_o} = \frac{\mu + 1}{r_d} \approx \frac{\mu}{r_d} = g_m \tag{10.27}$$

which agrees with the result obtained in Sec. 10.6 for the conductance looking into the source of a MOSFET with the gate at a constant voltage. In the discussion of diffused resistors in Sec. 7.8, it is indicated that 30 K is about the maximum resistance that can be fabricated. Larger values may be obtained by using the MOS structure as a load with gate connected to drain and tied to a fixed voltage such as $Q2$ in Fig. 10.17. By using a low g_m FET, a high value of effective resistance is obtained. For example, for $g_m = 10\ \mu$A/V, we obtain $R_o = 1/g_m = 100$ K. This value of effective resistance requires approximately 5 mil^2 of chip area compared with 300 mil^2 to yield a diffused 20.K resistance.

Example Figure 10.24*a* shows a CS amplifier with a saturated PMOS load (instead of a resistor). Assuming both transistors in saturation, determine the small-signal voltage gain (v_o/v_{in}).



(*a*) (*b*)

Fig. 10.24 *CS amplifier with a current source load.*

Solution To find (v_o/v_{in}), we draw the small-signal equivalent circuit. Noting that the gate and source of M_2 are at dc, ($g_m v_{gs}$) for this transistor will be zero. Thus we obtain the small-signal circuit of Fig. 10.24*b*. It can be seen from the circuit that

$$v_o = -\,g_{m1}\,(r_{d1} \parallel r_{d2})\,v_{gs1}$$

and

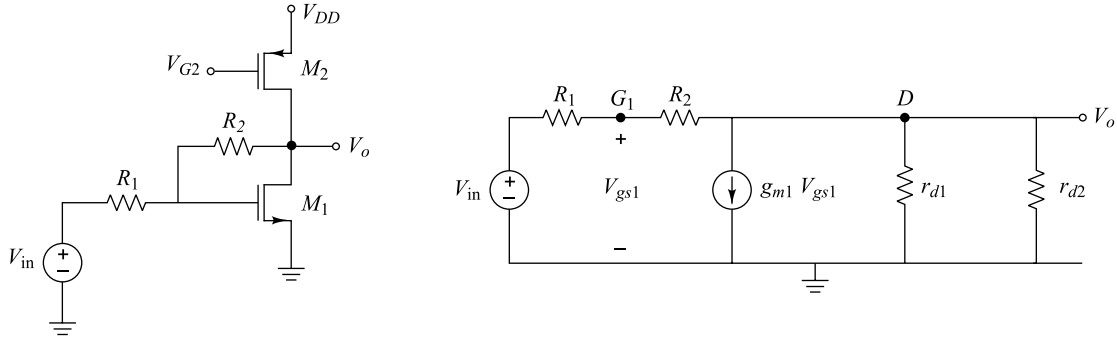
$$v_{gs1} = v_i$$

so that

$$\frac{v_o}{v_i} = -g_{m1}(r_{d1} \parallel r_{d2})$$

Typically, the r_d of a MOSFET is much larger than a resistance R_d that can be placed as a load. As a result, a saturated PMOS load results in much higher voltage gains, and therefore most MOS amplifiers use such loads.

Example Determine (v_o/v_{in}) for the circuit of Figure 10.25*a*. Assume both transistors in saturation.



(*a*) (*b*)

Fig. 10.25 *Inverting amplifier built from a CS amplifier.*

Solution Figure 10.25*b* shows the small-signal equivalent circuit. Writing KCLs at D and $G1$ yields

$$\frac{v_o}{(r_{d1} \parallel r_{d2})} + g_{m1}v_{gs1} + \frac{v_o - v_{gs1}}{R_2} = 0$$

or

$$v_o = -\frac{\left(g_{m1} - \frac{1}{R_2}\right)}{\left(\frac{1}{(r_{d1} \parallel r_{d2})} + \frac{1}{R_2}\right)} \cdot v_{gs1}$$

and

$$\frac{v_{gs1} - v_o}{R_2} + \frac{v_{gs1} - v_{in}}{R_1} = 0$$

or

$$v_{gs1} = \frac{\frac{v_o}{R_2} + \frac{v_{in}}{R_1}}{\left(\frac{1}{R_1} + \frac{1}{R_2}\right)}$$

Substituting for v_{gs1} in the first equation yields,

$$v_o = -\frac{\left(g_{m1} - \frac{1}{R_2}\right)}{\left(\frac{1}{(r_{d1} \parallel r_{d2})} + \frac{1}{R_2}\right)} \cdot \frac{\left(\frac{v_o}{R_2} + \frac{v_{in}}{R_1}\right)}{\left(\frac{1}{R_1} + \frac{1}{R_2}\right)}$$

Solving for (v_o/v_{in}) finally yields

$$\frac{v_o}{v_{in}} = -\frac{r_d(1 - g_{m1}R_2)}{(r_d + R_1 + R_2 + g_{m1}r_dR_1)} = -\frac{R_2}{R_1}\frac{\left(1 - \frac{1}{g_{m1}R_2}\right)}{\left(1 + \frac{r_d + R_1 + R_2}{g_{m1}r_dR_1}\right)}$$

If $g_{m1}R_1$ and $g_{m1}R_2$ are >> 1, then the above expression reduces to,

$$\frac{v_o}{v_{in}} \cong -\frac{R_2}{R_1}.$$

This gain expression is independent of the transistor parameters, and therefore provides a stable gain, even with variation in parameters due to process variations.

Example Determine (v_o/v_{in}) and R_o for the circuit of Fig. 10.26(a). Assume M_1 in saturation. (Note: M_2 is always in saturation because its gate and drain are shorted together).

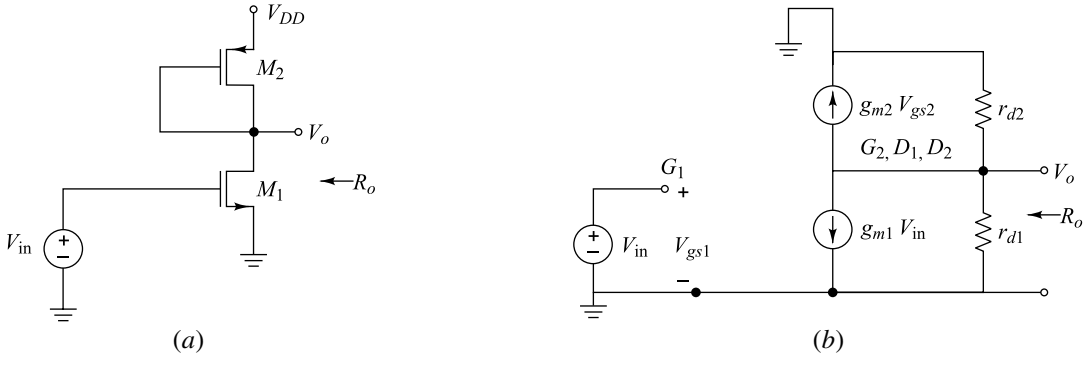


Fig. 10.26 *CS amplifier with a "diode"–connected load.*

Solution Figure 10.26(*b*) shows the small-signal circuit. We note here that when the gate and drain of a MOSFET are shorted, its dependent current source in the small-sginal circuit reduces to a resistor of value $1/g_m$. With this simplification, we see readily that

$$v_o = -\, g_{m1}\,(r_{d1} \parallel r_{d2} \parallel 1/g_{m2})\, v_{\text{in}}$$

For most MOS transistors, r_{d1} and r_{d2} are much greater than $1/g_{m2}$, and (v_o/v_{in}) reduces to

$$\frac{v_o}{v_{\text{in}}} \cong -\frac{g_{m1}}{g_{m2}}$$

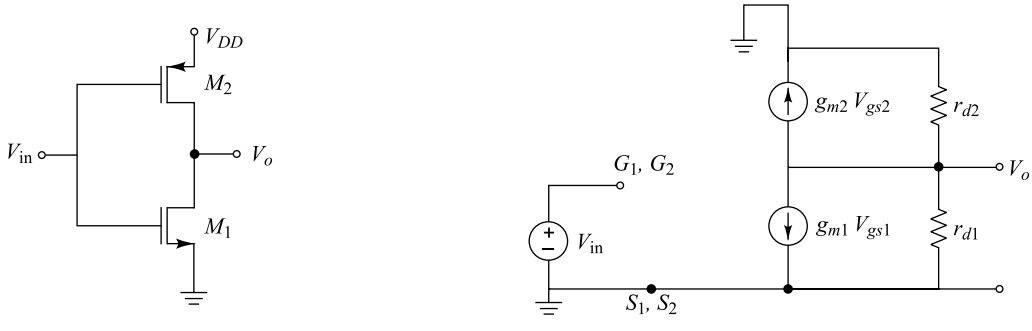
Using Eq. (10.20*a*) yields (given that the same drain current flows through M_1 and M_2),

$$\frac{v_o}{v_{\text{in}}} \cong -\sqrt{\frac{\mu_n (W/L)_n}{\mu_p (W/L)_p}}$$

The noteworthy characteristic of this gain expression is that it is independent of bias voltages or currents, and therefore it provides a highly linear gain. Of course, the gain cannot be made very large, because a large gain would require a large ratio of widths, and a large width ratio, with the same current flowing through both transistors, would require the transistor with the lower width to have a very large gate-source voltage, which is not feasible practically.

The output resistance of the circuit is $(r_{d1} \parallel r_{d2} \parallel 1/g_{m2}) \approx 1/g_{m2}$.

Example Determine (v_o/v_{in}) for the CMOS inverter circuit of Fig. 10.27(*a*). Assume both transistors in saturation.



(*a*) (*b*)

Fig. 10.27 *CMOS inverter amplifier.*

Solution Figure 10.27(*b*) shows the small-signal circuit. Writing a KCL at the output node, and noting that $v_{gs1} = v_{gs2} = v_{\text{in}}$, yields,

$$g_{m1} v_{\text{in}} + g_{m2} v_{\text{in}} + \frac{v_o}{r_{d1}} + \frac{v_o}{r_{d2}} = 0$$

or,

$$\frac{v_o}{v_{\text{in}}} \cong -(g_{m1} + g_{m2})(r_{d1} \parallel r_{d2})$$

Note that this circuit has a higher gain compared to the current-source load amplifier of Fig. 10.24 (by about a factor of 2). But is is also more difficult to provide a stable dc operating point for this circuit.

Example Figure 10.28(a) shows a MOS cascode amplifier, with an ideal current source load. Determine (v_o/v_{in}) for circuit. Assume both transistors in saturation.

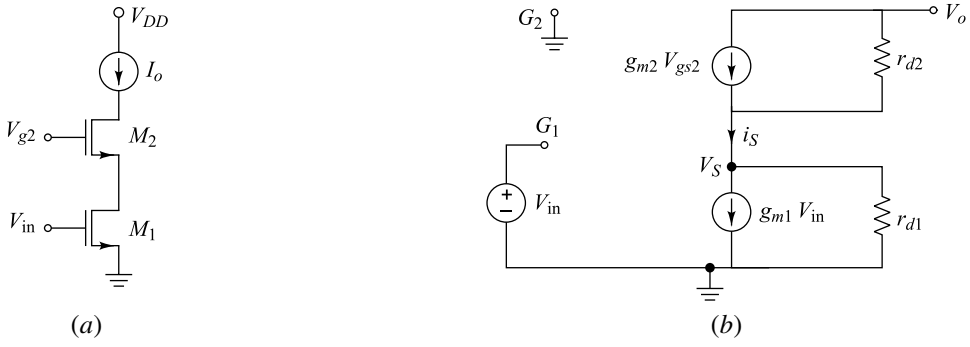


Fig. 10.28 *Cascode amplifier.*

Solution Figure 10.28(*b*) shows the small-signal circuit. Noting that $v_{gs2} = 0 - v_s = - v_s$, and that the current i_s is zero (*why*?), we write

$$v_s = - g_{m1}\, r_{d1}\, v_{\text{in}}$$

and

$$v_o - v_s = - g_{m2}\, r_{d2}\, v_{gs2} = g_{m2}\, r_{d2}\, V_s$$

or,

$$v_o = (1 + g_{m2}\, r_{d2})\, V_s$$

$$= - (1 + g_{m2}\, r_{d2})\, g_{m1}\, r_{d1}\, V_{\text{in}}$$

or,

$$\frac{v_o}{v_{\text{in}}} = -g_{m1}r_{d1}(1 + g_{m2}r_{d2}) \cong -g_{m1}r_{d1} \quad g_{m2}r_{d2}$$

As can be seen, this gain is of the order of $g_m{}^2 r_d{}^2$, which is the square of the gain of a common-source amplifier. Thus a cascode stage provides a much larger gain than a simple common-source or common-gate stage.

Example Figure 10.29(a) shows a two-stage CMOS amplifier. Determine its overall gain, (v_o/v_{in}). Assume all transistors in saturation.

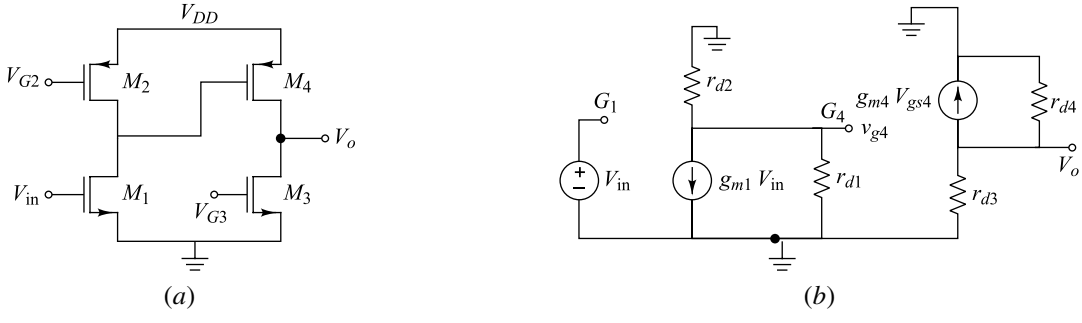


Fig. 10.29 *Two-stage CMOS amplifier.*

Solution Figure 10.29(*b*) shows the small-signal circuit. As with the circuit of Fig. 10.24, the ac gate-source voltages here of M_2 and M_3 are zero. It is significant that because the gate of a MOSFET has infinite impedance, the second stage of the amplifier does not load the first stage, unlike bipolar transistor amplifier circuits. This makes the analysis and design of MOSFET circuits much simpler. Thus we write,

$$v_{g4} = - g_{m1}\, (r_{d1} \parallel r_{d2})\, v_{\text{in}}$$

and

$$v_o = - g_{m4}\, (r_{d3} \parallel r_{d4})\, v_{g4}$$

or

$$\frac{v_o}{v_{\text{in}}} = -g_{m1}g_{m4}(r_{d1} \parallel r_{d2})(r_{d3} \parallel r_{d4})$$

This gain is of the order of $g_m^2 r_d^2/4$, which is similar to the cascode amplifier of the previous example. Considerations of speed and voltage swing determine which of these two configurations is more appropriate for a particular application.

10.8 Biasing the FET

The selection of an appropriate operating point (I_D, V_{GS}, V_{DS}) for an FET amplifier stage is determined by considerations similar to those given to transistors, as discussed in Chap. 9. These considerat-ions are output-voltage swing, distortion, power dissipation, voltage gain, and drift of drain current. In most cases it is not possible to satisfy all desired specifications simultaneously. In this section we examine several biasing circuits for field-effect devices.

Source Self-bias The configuration shown in Fig. 10.30 can be used to bias junction FET devices. For a specified drain current I_D, the corresponding gate-to-source voltage V_{GS} can be obtained applying either Eq. (10.8) or the plotted drain or transfer characteristics. Since the gate current (and, hence, the voltage drop across R_g) is negligible, the source resistance R_s can be found as the ratio of V_{GS} to the desired I_D.

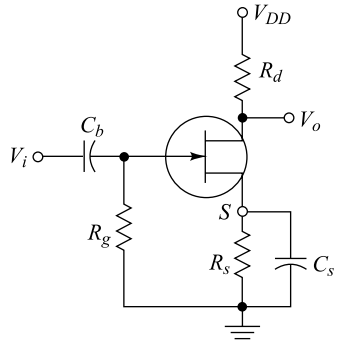


Fig. 10.30 *Source self-bias circuit.*

Example The amplifier of Fig. 10.30 utilizes an *n*-channel FET for which $V_P = -2.0$ V and $I_{DSS} = 1.65$ mA. It is desired to bias the circuit at $I_D = 0.8$ mA, using $V_{DD} = 24$ V. Assume $r_d >> R_d$. Find (*a*) V_{GS}, (*b*) g_m, (*c*) R_s, (*d*) R_d, such that the voltage gain is at least 20 dB, with R_s, bypassed with a very large capacitance C_s.

Solution (*a*) Using Eq. (10.8), we have $0.8 = 1.65(1 + V_{GS}/2.0)^2$. Solving, $V_{GS} = -0.62$ V.

(*b*) Equation (10.17) now yields

$$g_{mo} = -\frac{2I_{DSS}}{V_P} = \frac{(2)(1.65)}{2} = 1.65 \text{ mA/V}$$

and from Eq. (10.16)

$$g_m = g_{mo}\left(1 - \frac{V_{GS}}{V_P}\right) = (1.65)\left(1 - \frac{0.62}{2.0}\right) = 1.14 \text{ mA/V}$$

(*c*)
$$R_s = -\frac{V_{GS}}{I_D} = \frac{0.62}{0.8} = 0.77 \text{ K} = 770\ \Omega$$

(*d*) Since 20 dB corresponds to a voltage gain of 10, then from Eq. (10.23), with $r_d >> R_d$, $|A_V| = g_m R_d \geq 10$, or $R_d \geq 10/1.14 = 8.76$ K.

Biasing against Device Variation FET manufacturers usually supply information on the maximum and minimum values of I_{DSS} and V_P at room temperature. They also supply data to correct these quantities for temperature variations. The transfer characteristics for a given type of *n*-channel FET may appear as in Fig. 10.31*a*, where the top and bottom curves are for extreme values of temperature and device variation. Assume that, on the basis of considerations previously discussed, it is necessary to

bias the device at a drain current which will not drift outside of $I_D = I_A$ and $I_D = I_B$. Then the bias line $V_{GS} = -I_D R_s$ must intersect the transfer characteristics between the points A and B, as indicated in Fig. 10.31*a*. The slope of the bias line is determined by the source resistance R_s. For any transfer characteristic between the two extremes indicated, the current I_2 is such that $I_A < I_Q < I_B$, as desired.

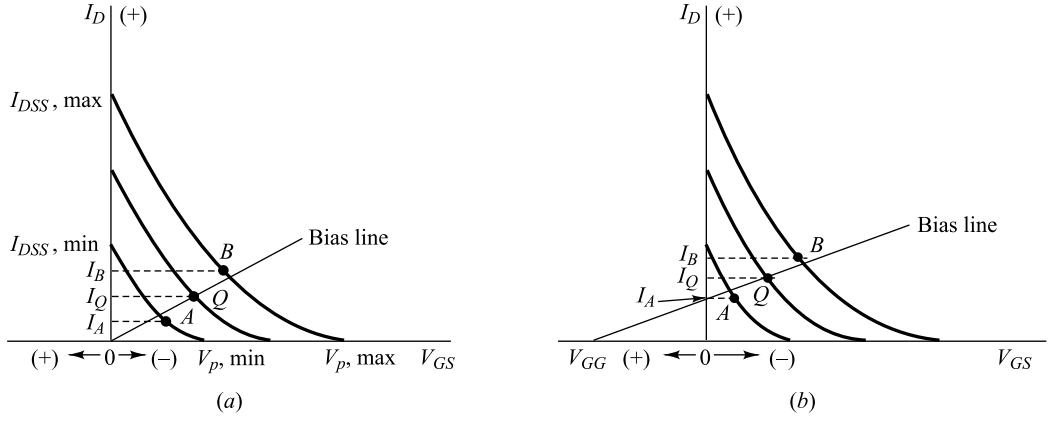


Fig. 10.31 *Maximum and minimum transfer curves for an n-channel FET. The drain current must lie between I_A and I_B. The bias line can be drawn through the origin for the current limits indicated in (a), but this is not possible for the currents specified in (b).*

Consider the situation indicated in Fig. 10.24*b*, where a line drawn to pass between points A and B does not pass through the origin. This bias line satisfies the equation

$$V_{GS} = V_{GG} - I_D R_s \tag{10.28}$$

Such a bias relationship may be obtained by adding a fixed bias to the gate in addition to the source self-bias, as indicated in Fig. 10.32*a*. A circuit requiring only one power supply and which can satisfy Eq. (10.27) is shown in Fig. 10.32*b*. For this circuit

$$V_{GG} = \frac{R_2 V_{DD}}{R_1 + R_2} \qquad R_g = \frac{R_1 R_2}{R_1 + R_2}$$

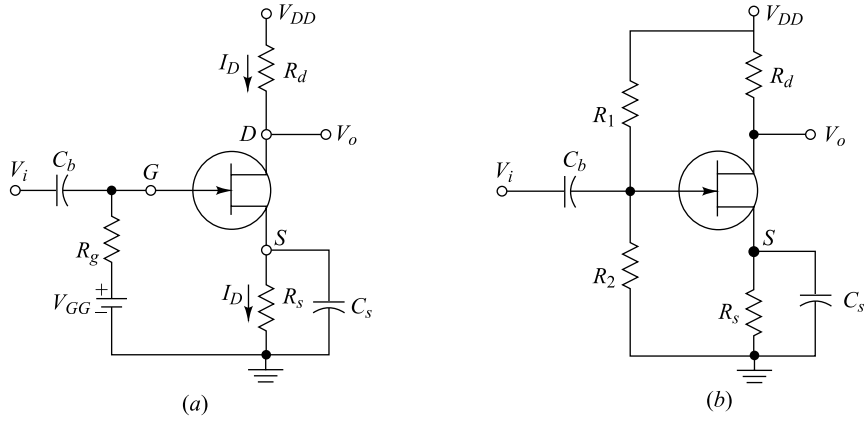


Fig. 10.32 *(a) Biasing an FET with a fixed-bias V_{GG} in addition to self-bias through R_s. (b) A single power-supply configuration which is equivalent to the circuit in (a).*

We have assumed that the gate current is negligible. It is also possible for V_{GG} to fall in the reverse-biased region so that the line in Fig. 10.31*b* intersects the axis of abscissa to the right of the origin. Under these circumstances two separate supply voltages must be used.

Example FET 2N3684 is used in the circuit of Fig. 10.32*b*. For this *n*-channel device the manufacturer specifies $V_{P,\min} = -2$ V$_{P,\max} = -5$ V, $I_{DSS,\min} = 1.6$ mA, and $I_{DSS,\max} = 7.05$ mA. The extreme transfer carves are plotted in Fig. 10.33. It is desired to bias the circuit so that $I_{D,\min} = 0.8$ mA $= I_A$ and $I_{D,\max} = 1.2$ mA $= I_B$ for $V_{DD} = 24$ V. Find (*a*) V_{GG} and R_s, and (*b*) the range o' possible values in I_D if $R_s = 3.3$ K and $V_{GG} = 0$.

Solution (*a*) The bias line will lie between *A* and *B*, as indicated, if it is drawn to pass through the two points $V_{GS} = 0$, $I_D = 0.9$ mA, and $V_{GS} = -4$ V. $I_D = 1.1$ mA. The slope of this line determines R_s, or

$$R_s = \frac{4 - 0}{1.1 - 0.9} = 20 \text{ K}$$

Then, from the first point and Eq. (10.26), we find

$$V_{GG} = I_D R_s = (0.9)(20) = 18 \text{ V}$$

(*b*) If $R_s = 3.3$ K, we see from the curves that $I_{D,\min} = 0.4$ mA and $I_{D,\max}$ 1.2 mA. The minimum current is far below the specified value of 0.8 mA.

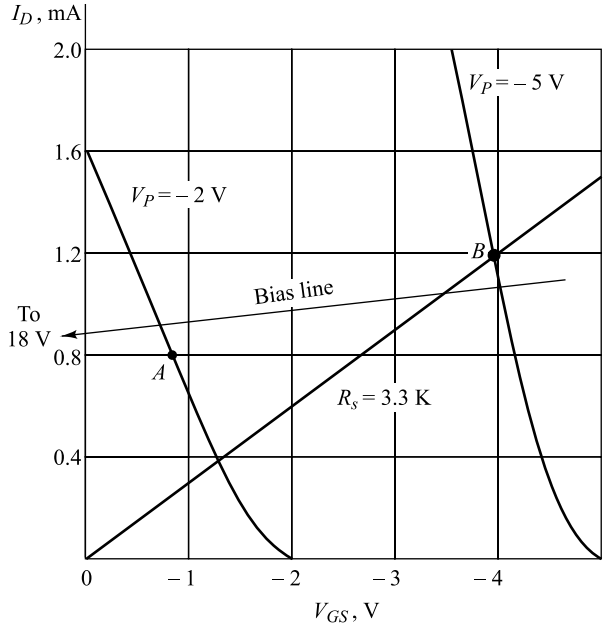


Fig. 10.33 *Extreme transfer curves for the 2N3684 field-effect transistor. (Courtesy of Union Carbide Corporation.)*

Biasing the MOSFET The most common method of biasing integrated circuit MOSFET amplifiers is to use current mirrors, such as the one shown in Fig. 10.34. In this circuit, M_2–M_3 form a current mirror which provides a constant dc drain current to the common-source amplifier formed by M_1–M_2.

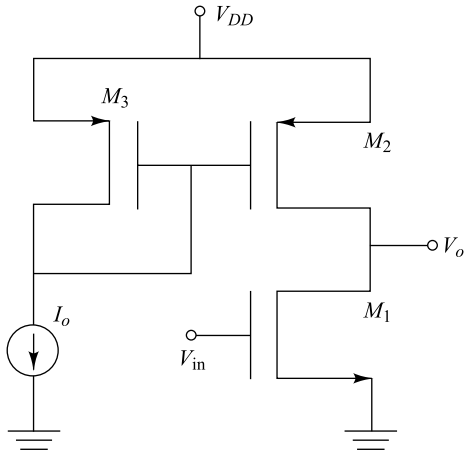


Fig. 10.34 *Biasing for a MOSFET amplifier.*

Example In the circuit if Fig. 10.35, determine the change in the drain current of M_2 if the threshold voltage of both transistors change by 10%. Use Eq. (10.18*c*) for the drain current. Assume that M_1 and M_2 are identical transistors, and are both in saturation.

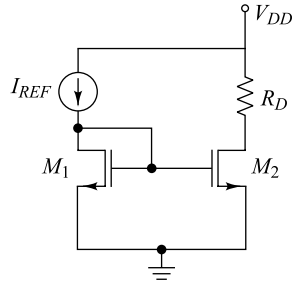


Fig. 10.35 *MOS current mirror.*

Solution From Eq. (10.18*c*),

$$I_{D1} = \frac{\mu_n C_{ox} W}{2L}(V_{GS1} - V_T)^2 = I_{\text{REF}}$$

and

$$I_{D2} = \frac{\mu_n C_{ox} W}{2L}(V_{GS2} - V_T)^2$$

Since $V_{GS1} = V_{GS2}$ for this circuit, and since the two transistors are identical, we conclude from the above two equations that

$$I_{D1} = I_{D2} = I_{\text{REF}}.$$

This equation implies that I_{D2} does not vary at all as V_T varies. This is the reason why the circuit of Fig. 10.35 makes an excellent biasing circuit.

Example In the *AGC* amplifier of Fig. 10.38, assume that $A = 1$. Find v_o for this circuit for an ideal voltage source connected at v_i. For simplicity, assume that $h_{ie} = 0$, $h_{re} = 0$, and $h_{oe} = 0$ for Q_1, and that $h_{fe} >> 1$. Use Eq. (10.29) for Q_2.

Solution Figure 10.36 shows the small-signal circuit for the amplifier of Fig. 10.38, where $R = R_1 \| R_2$, and , from Eq. (10.30), $r_d = \dfrac{r_o}{(1 - Kv_{op})}$, where v_{op} is the peak value of v_o. We write, by inspection,

$$v_i = (1 + h_{fe})\, i_b\, r_d \approx h_{fe}\, i_b\, r_d$$

or,

$$v_i = \frac{h_{fe}\, i_b\, r_o}{(1 - Kv_{op})}$$

or,

$$i_b = \frac{v_i(1 - Kv_{op})}{h_{fe} r_o}$$

and

$$v_o = - h_{fe}\, R_c\, i_b$$

Hence

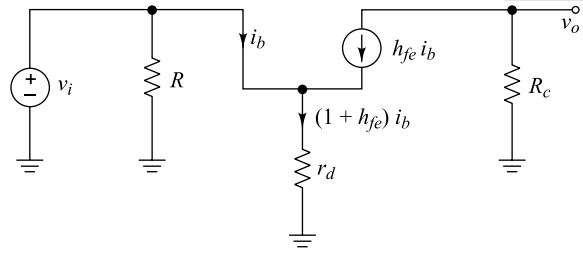


Fig. 10.36 *Small-signal circuit for Fig. 10.38.*

$$v_o = -h_{fe} R_c \frac{v_i(1 - Kv_{op})}{h_{fe} r_o} = -\frac{R_c}{r_o} v_i + Kv_{op} \frac{R_c}{r_o} v_i$$

This is a tricky equation. The way we proceed from here is to assume that v_i and v_o are sinusoidal voltages. Since there are no reactive elements in the circuit, we can write,

$$v_i = v_{ip} \cos\, \omega t$$

and

$$v_o = v_{op} \cos\, \omega t$$

Substituting these in the previous equation yields,

$$v_{op} \cos \omega t = -\frac{R_c}{r_o} \cdot v_{ip} \cos \omega t + Kv_{op} \frac{R_c}{r_o} \cdot v_{ip} \cos \omega t$$

Cancelling cos ωt, and solving for v_{op} yields,

$$v_{op} = -\frac{\frac{R_c}{r_o} v_{ip}}{\left(1 - K \frac{R_c}{r_o} v_{ip}\right)}$$

If $\frac{R_c}{r_o} v_{ip} >> 1$, which is usually how this circuit is designed, then $v_{op} \cong \frac{1}{K}$. This shows that the amplitude of the output voltage is constant, independent of the input voltage, which demonstrates that this circuit performs automatic gain control. It is also important to recognize that all such automatic gain control circuits must have an input-output relationship that is non-linear, as exemplified by the equation above, because to obtain an output voltage magnitude that is independent of the input voltage magnitude, the forward path would cause v_o to vary linearly with v_i, but the feedback path would need to have an inverse dependence between v_o and v_i, so that the two dependences cancel each other to yield a constant v_o magnitude.

10.9 The FET as a Voltage-Variable Resistor[13] (VVR)

In most linear applications of field-effect transistors the device is operated in the constant-current portion of its output characteristics. We now consider FET transistor operation in the region before pinch-off, where V_{DS} is small. In this region the FET is useful as a voltage-controlled resistor; i.e., the drain-to-source resistance is controlled by the bias voltage V_{GS}. In such an application the FET is also referred to as a *voltage-variable resistor* (VVR), or *voltage-dependent resistor* (VDR).

Figure 10.37*a* shows the low-level bidirectional characteristics of an FET. The slope of these characteristics gives r_d as a function of V_{GS}. Figure 10.37*a* has been extended into the third quadrant to give an idea of device linearity around $V_{DS} = 0$.

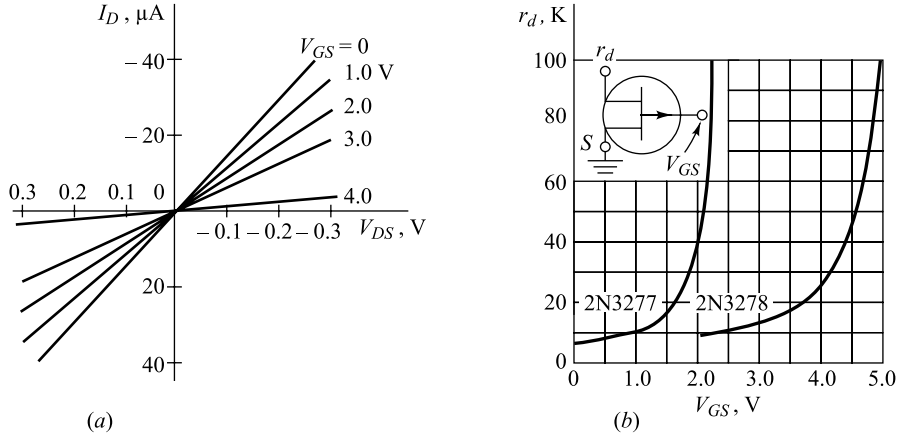


Fig. 10.37 *(a) FET low-level drain characteristics for 2N3278. (b) Small-signal FET resistance variation with applied gate voltage. (Courtesy of Fairchild Semiconductor Company.)*

In our treatment of the junction FET characteristics in Sec. 10.3, we derive Eq. (10.5), which gives the drain-to-source conductance $g_d = I_D/V_{DS}$ for small values of V_{DS}. From this equation we have

$$g_d = g_{do}\left[1 - \left(\frac{V_{GS}}{V_P}\right)^{\frac{1}{2}}\right] \tag{10.29}$$

where g_{do} is the value of the drain conductance when the bias is zero. Variation of r_d with V_{GS} is plotted in Fig. 10.28*b* for the 2N3277 and 2N3278 FETs. The variation of r_d with V_{GS} can be closely approximated by the empirical expression

$$r_d = \frac{r_o}{1 - KV_{GS}} \tag{10.30}$$

where r_o = drain resistance at zero gate bias
K = a constant, dependent upon FET type
V_{GS} = gate-to-source voltage

Applications of the VVR Since the FET operated as described above acts like a variable passive resistor, it finds applications in many areas where this property is useful. The VVR, for example, can be used to vary the voltage gain of a multistage amplifier A as the signal level is increased. This action is called *automatic gain control* (AGC). A typical arrangement is shown in Fig. 10.38. The signal is taken at a high-level point, rectified, and filtered to produce a dc voltage proportional to the output-signal level. This voltage is applied

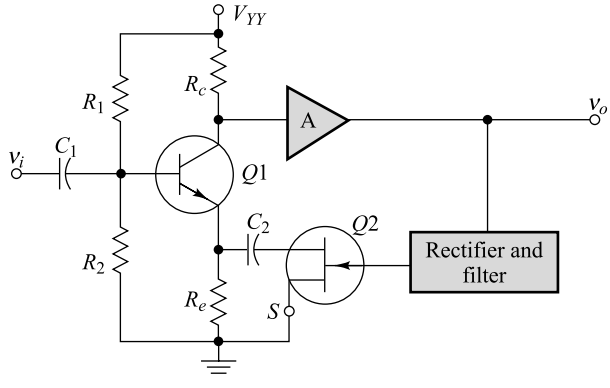


Fig. 10.38 *AGC amplifier using the FET as a voltage-variable resistor.*

to the gate of $Q2$, thus causing the ac resistance between the drain and source to change, as shown in Fig. 10.37*b*. We thus may cause the gain of transistor $Q1$ to decrease as the output-signal level increases. The dc bias conditions of $Q1$ are not affected by $Q2$ since $Q2$ is isolated from $Q1$ by means of capacitor C_2.

10.10 The Common-source Amplifier at High Frequencies

The circuits discussed in this and the following section apply equally well to either JFETs or MOSFETs (except for the method of biasing). The low-frequency analysis of Sec. 10.8 is now modified to take into account the effect of the internal node capacitances.

Voltage Gain The circuit of Fig. 10.39*a* is the basic CS amplifier configuration. If the FET is replaced by the circuit model of Fig. 10.8*b*, we obtain the network in Fig. 10.39*b*. The output voltage V_o between D and S is easily found with the aid of the theorem of Sec. 8.7, namely, $V_o = IZ$, where I is the short-circuit current and Z is the impedance seen between the terminals. To find Z, the independent generator V_i is (imagined) short-circuited, so that $V_i = 0$, and hence there is no current in the dependent generator $g_m V_i$. We then note that Z is the parallel combination of the impedances corresponding to Z_L, C_{ds}, r_d, and C_{gd}. Hence

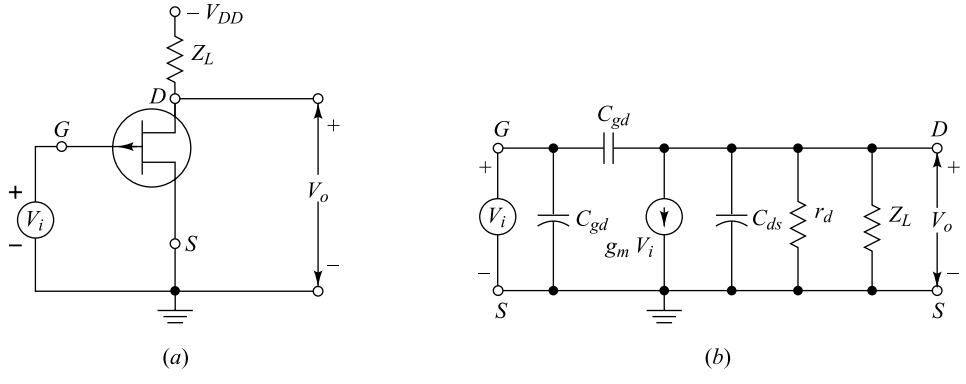


Fig. 10.39 *(a) The common-source amplifier circuit; (b) small-signal equivalent circuit at high frequencies. (The biasing network is not indicated.)*

$$Y = \frac{1}{Z} = Y_L + Y_{ds} + g_d + Y_{gd} \tag{10.31}$$

where $Y_L = 1/Z_L$ = admittance corresponding to Z_L
$Y_{ds} = j\omega C_{ds}$ = admittance corresponding to C_{ds}
$g_d = 1/r_d$ = conductance corresponding to r_d
$Y_{gd} = j\omega C_{gd}$ = admittance corresponding to C_{gd}

The current in the direction from D to S in a zero-resistance wire connecting the output terminals is

$$I = -g_m V_i + V_i Y_{gd} \tag{10.32}$$

The amplification A_V with the load Z_L in place is given by

$$A_V = \frac{V_o}{V_i} = \frac{IZ}{V_i} = \frac{I}{V_i Y} \tag{10.33}$$

or from Eqs (10.31) and (10.32)

$$A_V = \frac{-g_m + Y_{gd}}{Y_L + Y_{ds} + g_d + Y_{gd}} \tag{10.34}$$

At low frequencies the FET capacitances can be neglected and hence

$$Y_{ds} = Y_{gd} = 0$$

Under these conditions Eq. (10.34) reduces to

$$A_V = \frac{-g_m}{Y_L + g_d} = \frac{-g_m r_d Z_L}{r_d + Z_L} = -g_m Z'_L \tag{10.35}$$

where $Z'_L \equiv Z_L || r_d$. This equation agrees with Eq. (10.24), with Z_L replaced by R_d.

Input Admittance An inspection of Fig. 10.39*b* reveals that the gate circuit is not isolated from the drain circuit, but rather that they are connected by C_{gd}. From Miller's theorem (Sec. 8.11), this admittance may be replaced by $Y_{gd}(l - K)$ between G and S, and by $Y_{gd}(1 - 1/K)$ between D and S, where $K = A_V$. Hence the input admittance is given by

$$Y_i = Y_{gs} + (1 - A_V)Y_{gd} \tag{10.36}$$

This expression indicates that for an FET to possess negligible input admittance over a wide range of frequencies, the gate-source and gate-drain capacitances must be negligible.

Input Capacitance (Miller Effect) Consider an FET with a drain-circuit resistance R_d. From the previous discussion it follows that within the audio-frequency range, the gain is given by the simple expression $A_V = -g_m R'_d$, where R'_d is $R_d \| r_d$. In this case, Eq. (10.36) becomes

$$\frac{Y_i}{j\omega} \equiv C_i = C_{gs} + (1 + g_m R'_d)C_{gd} \tag{10.37}$$

This increase in input capacitance C_i over the capacitance from gate to source is called the *Miller effect*.

This input capacitance is important in the operation of cascaded amplifiers. In such a system the output from one stage is used as the input to a second amplifier. Hence the input impedance of the second stage acts as a shunt across the output of the first stage and R_d is shunted by the capacitance C_i. Since the reactance of a capacitor decreases with increasing frequencies, the resultant output impedance of the first stage will be correspondingly low for the high frequencies. This will result in a decreasing gain at the higher frequencies.

Example A MOSFET has a drain-circuit resistance R_d of 100 K and operates at 20 kHz. Calculate the voltage gain of this device as a single stage, and then as the first transistor in a cascaded amplifier consisting of two identical stages. The MOSFET parameters are g_m = 1.6 mA/V, r_d = 44 K, C_{gs} = 3.0 pF, C_{ds} = 1.0 pF, and C_{gd} = 2.8 pF.

Solution

$$Y_{gs} = j\omega C_{gs} = j2\pi \times 2 \times 10^4 \times 3.0 \times 10^{-12} = j3.76 \times 10^{-7} \ \text{℧}$$

$$Y_{ds} = j\omega C_{ds} = j1.26 \times 10^{-7} \ \text{℧}$$

$$Y_{gd} = j\omega C_{gd} = j3.52 \times 10^{-7} \ \text{℧}$$

$$g_d = \frac{1}{r_d} = 2.27 \times 10^{-5} \ \text{℧}$$

$$Y_d = \frac{1}{R_d} = 10^{-5}\ \mho$$

$$g_m = 1.60 \times 10^{-3}\ \mho$$

The gain of a one-stage amplifier is given by Eq. (10.33):

$$A_V = \frac{-g_m + Y_{gd}}{g_d + Y_d + Y_{ds} + Y_{gd}} = \frac{-1.60 \times 10^{-3} + j3.52 \times 10^{-7}}{3.27 \times 10^{-5} + j4.78 \times 10^{-7}}$$

It is seen that the j terms (arising from the interelectrode capacitances) are negligible in comparison with the real terms. If these are neglected, then $A_v = -48.8$. This value can be checked by using Eq. (10.23), which neglects inter electrode capacitances. Thus

$$A_V = \frac{-\mu R_d}{R_d + r_d} = \frac{-1.6 \times 44 \times 100}{100 + 44} = -48.8 = -g_m R'_d$$

Since the gain is a real number, the input impedance consists of a capacitor whose value is given by Eq. (10.37):

$$C_i = C_{gs} + (1 + g_m R'_d) C_{gd} = 3.0 + (1 + 49)(2.8) = 143 \text{ pF}$$

Consider now a two-stage amplifier, each stage consisting of an FET operating as above. The gain of the second stage is that just calculated. However, in calculating the gain of the first stage, it must be remembered that *the input impedance of the second stage acts as a shunt on the output of the first stage*. Thus the drain load now consists of a 100-K resistance in parallel with 143 pF. To this must be added the capacitance from drain to source of the first stage since this is also in shunt with the drain load. Furthermore, any stray capacitances due to wiring should be taken into account. For example, for every 1-pF capacitance between the leads going to the drain and gate of the second stage, 50 pF is effectively added across the load resistor of the first stage! This clearly indicates the importance of making connections with very short direct leads in high-frequency amplifiers. Let it be assumed that the input capacitance, taking into account the various factors just discussed, is 200 pF. Then the load admittance is

$$Y_L = \frac{1}{R_d} + j\omega C_i = 10^{-5} + j2\pi \times 2 \times 10^4 \times 200 \times 10^{-12}$$

$$= 10^{-5} + j2.52 \times 10^{-5}\ \mho$$

The gain is gien by Eq (10.36):

$$A_V = \frac{-g_m}{g_d + Y_L} = \frac{-1.6 \times 10^{-3}}{2.27 \times 10^{-5} + 10^{-5} + j2.52 \times 10^{-5}}$$

$$= -30.7 + j23.7 = 38.8 \angle 143.3°$$

Thus the effect of the capacitances has been to reduce the magnitude of the amplification from 48.8 to 38.8 and to change the phase angle between the output and input from 180 to 143.3°.

If the frequency were higher, the gain would be reduced still further. For example, this circuit would be useless as a video amplifier, say, to a few megahertz, since the gain would then be less than unity. This variation of gain with frequency is called *frequency distortion*. Cascaded amplifiers and frequency distortion are discussed in detail in Chap. 12.

Output Admittance For the common-source amplifier of Fig. 10.39 the output impedance is obtained by "looking into the drain" with the input voltage set equal to zero. If $V_i = 0$ in Fig. 10.39*b*, we see r_d, C_{ds}, and C_{gd} in parallel. Hence the output admittance with Z_L considered external to the amplifier is given by

$$Y_o = g_d + Y_{ds} + Y_{gd} \tag{10.38}$$

10.11 The Common-drain Amplifier at High Frequencies

The source-follower configuration is given in Fig. 10.21*b*, with $R_d = 0$, and is repeated in Fig. 10.31*a*. Its equivalent circuit with the FET replaced by its high-frequency model of Fig. 10.8*b* is shown in Fig. 10.40*b*.

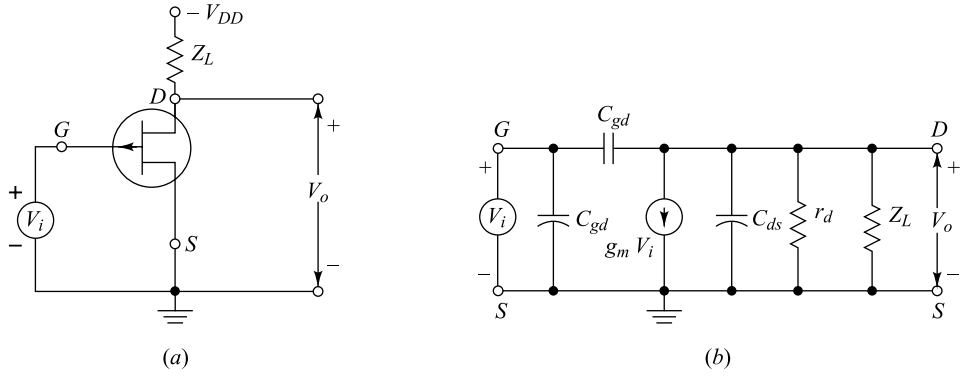


Fig. 10.40 *(a) The source-follower; (b) small-signal high-frequency equivalent circuit. (The biasing network is not indicated.)*

Voltage Gain The output voltage V_o can be found from the product of the short-circuit current and the impedance between terminals S and N. We now find for the voltage gain

$$A_V = \frac{(g_m + j\omega C_{gs})R_s}{1 + (g_m + g_d + j\omega C_T)R_s} \tag{10.39}$$

$$C_T \equiv C_{gs} + C_{ds} + C_{sn} \tag{10.40}$$

where C_{sn} represents the capacitance from source to ground. At low frequencies the gain reduces to

$$A_V \approx \frac{g_m R_s}{1 + (g_m + g_d)R_s} \tag{10.41}$$

Note that the amplification is positive and has a value less than unity. If $g_m R_s >> 1$, then $A_V \approx g_m/(g_m + g_d) = \mu/(\mu + 1)$.

Input Admittance The source follower offers the important advantage of lower input capacitance than the CS amplifier. The input admittance Y_i is obtained by applying Miller's theorem to C_{gs}. We find

$$Y_i = j\omega C_{gd} + j\omega C_{gs}(1 - A_V) \approx j\omega C_{gd} \tag{10.42}$$

because $A_V \approx 1$.

Output Admittance The output admittance Y_o, with R_s considered external to the amplifier, is given by

$$Y_o = g_m + g_d + j\omega C_T \tag{10.43}$$

where C_T is given by Eq. (10.37). At low frequencies the output resistance R_o is

$$R_o = \frac{1}{g_m + g_d} \approx \frac{1}{g_m} \tag{10.44}$$

since $g_m >> g_d$. For $g_m = 2$ mA/V, then $R_o = 500\ \Omega$.

The source follower is used for the same applications as the emitter follower, those requiring high input impedance and low output impedance.

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OBJECTIVE-TYPE QUESTIONS

1. In a JFET, the drain current magnitude decreases as the reverse bias across the gate-channel increases because a larger reverse bias causes
   (*a*) more recombination in the transition region
   (*b*) the transition region to be wider, which narrows the thickness of the conducting channel
   (*c*) the mobile carriers to travel slower in the channel, by reducing their mobility
   (*d*) the reverse bias current to increase, thus diverting the channel current away from the drain
2. The drain characteristics of a JFET show an abrupt increase in current at sufficiently large drain-source voltages. This is because
   (*a*) the reverse-biased drain-gate junction breaks down
   (*b*) of thermal runaway
   (*c*) the drain and source terminals get effectively shorted
   (*d*) the drain-gate junction behaves like a forward-biased diode
3. In the saturation region, the JFET transfer characteristics are
   (*a*) exponential (*b*) linear
   (*c*) parabolic (*d*) hyperbolic
4. The threshold voltage (V_T) of a MOSFET is defined as
   (*a*) the drain-source voltage at which the transistor goes into saturation

(*b*) the gate-source voltage at which the transistor goes into saturation
(*c*) the drain-source voltage at which a predefined value of drain current starts flowing
(*d*) the gate-source voltage at which a predefined value of drain current starts flowing.

5. To achieve the same ON resistance, with the same magnitudes of bias voltages,
(*a*) a PMOS transistor requires a larger area than an NMOS transistor
(*b*) an NMOS transistor requires a larger area than a PMOS transistor
(*c*) a PMOS transistor must have twice the channel length of an NMOS transistor
(*d*) a PMOS transistor must have twice the threshold voltage of an NMOS transistor

6. On an IC, the substrate terminal of an NMOS transistor is more frequently connected to ground, rather than to the source terminal, because
(*a*) connecting to the source increases the threshold voltage of the transistor
(*b*) connecting the substrate to the source requires a separate *p*-well for the transistor, which is very area-expensive
(*c*) the drain-substrate junction may get forward-biased in the latter case
(*d*) this protects the gate oxide from electrostatic breakdown

7. In the saturation region, the $I_D - V_{GS}$ characteristics of a MOSFET are
(*a*) linear (*b*) quadratic
(*c*) exponential (*d*) hyperbolic

8. In the triode region, the $I_D - V_{DS}$ characteristics of a MOSFET are
(*a*) hyperbolic (*b*) linear
(*c*) quadratic (*d*) exponential

9. Of all logic families, CMOS has become the most preferred, and exclusive, logic style for VLSI and ULSI circuits because
(*a*) it is the fastest of all logic families
(*b*) it is the most immune to noise
(*c*) all types of logic gates can be designed in it easily
(*d*) it consumes no static power

10. The source-bias circuit of Fig. 10.23 provides dc biasing for the FET. The resistance from gate to ground (R_g) in that circuit is necessary because, without it,
(*a*) the input time-constant will become infinite
(*b*) the input ac signal will have no path to ground
(*c*) there will be no dc potential established at the gate terminal
(*d*) the circuit will actually work fine; R_g is not really necessary

Ans. **1.** *b* **2.** *a*, **3.** *c*, **4.** *d*, **5.** *a*, **6.** *b*, **7.** *b*, **8.** *c*, **9.** *d*, **10.** *c*

REVIEW QUESTIONS

10.1 (*a*) Sketch the basic structure of an *n*-channel junction field-effect transistor. (*b*) Show the circuit symbol for the JFET.

10.2 (*a*) Draw a family of CS drain characteristics of an *n*-channel JFET. (*b*) Explain the shape of these curves qualitatively.

10.3 How does the FET behave (*a*) for small values of $|V_{DS}|$? (*b*) For large $|V_{Ds}|$?

10.4 (*a*) Define the *pinch-off voltage* V_P. (*b*) Sketch the depletion region before and after pinch-off.

10.5 Sketch the geometry of a JFET in integrated form.

10.6 (*a*) How does the drain current vary with gate voltage in the saturation region? (*b*) How does the transconductance vary with drain current?

10.7 Define (*a*) *transconductance* g_m, (*b*) *drain resistance* r_d, and (c) *amplification factor* μ of an FET.

10.8 Give the order of magnitude of g_m, r_d, and μ for a MOSFET.

10.9 Show the small-signal model of an FET (*a*) at low frequencies and (*b*) at high frequencies.

10.10 (*a*) Sketch the cross section of a p-channel enhancement MOSFET. (*b*) Show two circuit symbols for this MOSFET.

10.11 For the MOSFET in Rev. 10.10 draw (*a*) the drain characteristics and (*b*) the transfer curve.

10.12 (*a*) Draw the circuit of a MOSFET NOT circuit. (*b*) Explain how it functions as an inverter.

10.13 Sketch a two-input NAND gate and verify that it satisfies the Boolean NAND equation.

10.14 Repeat Rev. 10.15 for a two-input NOR gate.

10.15 Sketch a CMOS inverter and explain its operation.

10.16 (*a*) Draw the circuit of an FET amplifier with a source resistance R_s and a drain resistance R_d. (*b*) What is the Thevenin's equivalent circuit looking into the drain at low frequencies?

10.17 Repeat Rev. 10.18 looking into the source.

10.18 (*a*) Sketch the circuit of a source-follower. At low frequencies what is (*b*) the maximum value of the voltage gain? (*c*) The order of magnitude of the out put impedance?

10.19 (*a*) Sketch the circuit of a CS amplifier. (*b*) Derive the expression for the voltage gain at low frequencies. (c) What is the maximum value of A_v?

10.20 (*a*) Draw two biasing circuits for a JFET. (*b*) Explain under what circumstances each of these iwo arrangements should be used.

10.21 Draw two biasing circuits for a MOSFET.

10.22 (*a*) How is an FET used as a voltage-variable resistance? (*b*) Explain.

10.23 (*a*) Sketch the small-signal high-frequency circuit of a CS amplifier. (*b*) Derive the expression for the voltage gain.

10.24 (*a*) From the circuit of Rev. 10.25, derive the input admittance. (*b*) What is the expression for the input capacitance in the audio range?

10.25 What specific capacitance has the greatest effect on the high-frequency response of a cascade of FET amplifiers? Explain.

10.26 Repeat Rev. 10.25 for a source-follower circuit.

10.27 Repeat Rev. 10.26 for a CD amplifier.

PROBLEMS

10.1 The drain resistance R_d of an *n*-channel FET with the source grounded is 2 K. The FET is operating at a quiescent point $V_{DS} = 10$ V, and $I_{DS} = 3$ mA, and its characteristics are given in Fig. 10.3.

(*a*) To what value must the gate voltage be changed if the drain current is to change to 5 mA?

(*b*) To what value must the voltage V_{DD} be changed if the drain current is to be brought back to its previous value? The gate voltage is maintained constant at the value found in part *a*.

10.2 For a *p*-channel silicon FET with $a = 2 \times 10^{-4}$ cm and channel resistivity $\rho = 10$ Ω-cm

(*a*) Find the pinch-off voltage.

(*b*) Repeat (*a*) for a *p*-channel germanium FET with $\rho = 2$ Ω-cm.

10.3 (*a*) Plot the transfer characteristic curve of an FET as given by Eq. (10.8), with $I_{DSS} = 10$ mA and $V_P = -4$ V.

(*b*) The magnitude of the slope of this curve at $V_{GS} = 0$ is g_{mo} and is given by Eq. (10.17). If the slope is extended as a tangent, show that it intersects the V_{GS} axis at the point $V_{GS} = V_P/2$.

10.4 (*a*) Show that the transconductance g_m of a JFET is related to the drain current I_{DS} by

$$g_m = \frac{2}{|V_P|}\sqrt{I_{DSS} I_{DS}}$$

(*b*) If $V_P = -4$ V and $I_{DSS} = 4$ mA, plot g_m versus I_{DS}.

10.5 Show that for small values of V_{GS} compared with V_P, the drain current is given approximately by $I_D \approx I_{DSS} + g_{mo} V_{GS}$.

10.6 (*a*) For the FET whose characteristics are plotted in Fig. 10.3, determine r_d and g_m graphically at the quiescent point $V_{DS} = 10$ V and $V_{GS} = -1.5$ V. Also evaluate μ.

(*b*) Determine $r_{d,\mathrm{ON}}$ for $V_{GS} = 0$.

10.7 (*a*) Verify Eq. (10.15).

(*b*) Starting with the definitions of g_m and r_d, show that if two identical FETs are connected in parallel, g_m is doubled and r_d is halved. Since $\mu = r_d g_m$, then μ remains unchanged.

(*c*) If the two FETs are not identical, show that

$$\frac{1}{r_d} = \frac{1}{r_{d1}} + \frac{1}{r_{d2}}$$

and that

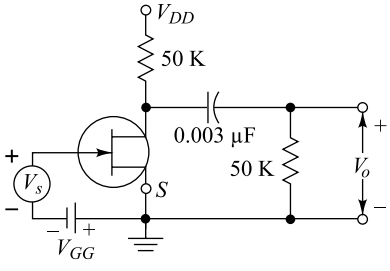
$$\mu = \frac{\mu_1 r_{d2} + \mu_2 r_{d1}}{r_{d1} + r_{d2}}$$

10.8 Given the transfer characteristic of an FET, explain clearly how to determine g_m at a specified quiescent point.

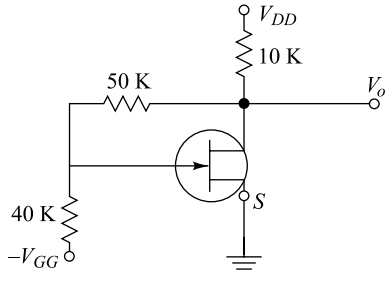
10.9 (*a*) Calculate the voltage gain $A_V = V_o/V_i$ at 1 kHz for the circuit shown. The FET parameters are g_m = 2 mA/V and r_d = 10 K. Neglect capacitances.

(*b*) Repeat part *a* if the capacitance 0.003 μF is taken under consideration.

10.10 If an input signal V_i is impressed between gate and ground, find the amplification $A_V = V_o/V_i$. Apply Miller's theorem to the 50-K resistor. The FET parameters are μ = 30 and r_d = 5 K. Neglect capacitances.



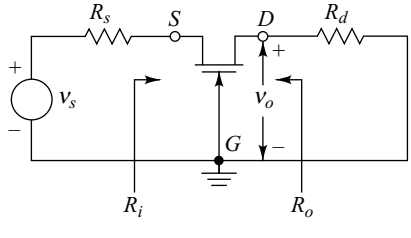
Prob. 10.9



Prob. 10.10

10.11 If in Prob. 10.10 the signal V_i is impressed in series with the 40-K resistor (instead of from gate to ground), find $A_V = V_o/V_i$.

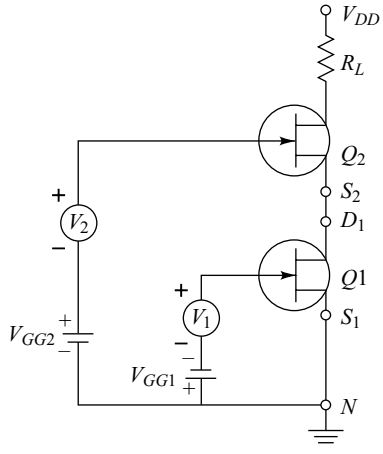
10.12 The circuit shown is called common-gate amplifier. For this circuit find (*a*) the voltage gain, (*b*) the input impedance, (*c*) the output impedance. Power supplies are omitted for simplicity. Neglect capacitances.



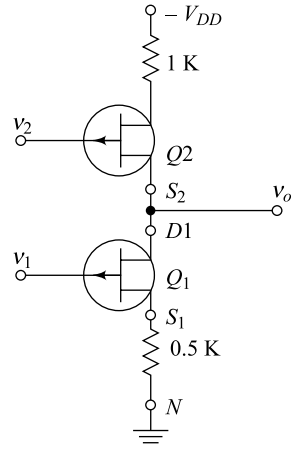
Prob. 10.12

10.13 Find an expression for the signal voltage across R_L. The two FETs are identical, with parameters μ, r_d, and g_m.

10.14 Each FET shown has the parameters r_d = 10 K and g_m = 2 mA/V. Using the equivalent circuits in Fig. 10.23 at S_2 and D_1, find the gain (*a*) v_o/v_1 if $v_2 = 0$, (*b*) v_o/v_2 if $v_1 = 0$.



Prob. 10.13



Prob. 10.14

10.15 (*a*) Prove that the magnitude of the signal current is the same in both FETs provided that

$$r = \frac{1}{g_m} + \frac{2R_L}{\mu}$$

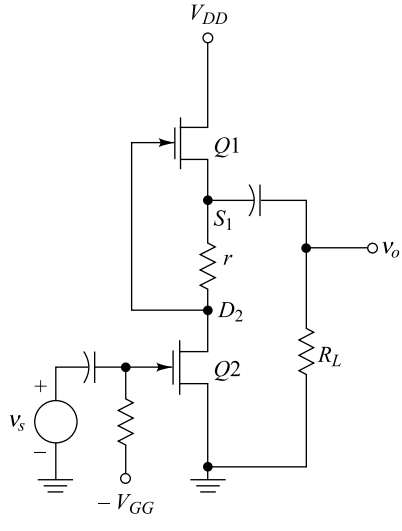
Neglect the reactance of the capacitors.

(*b*) If *r is* chosen as in part *a*, prove that the voltage gain is given by

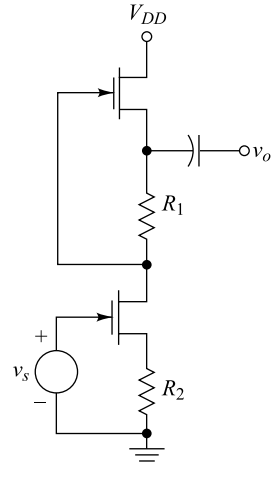
$$A = \frac{-\mu^2}{\mu + 1} \frac{R_L}{R_L + r_d/2}$$

10.16 (*a*) If $R_1 = R_2 = R$ and the two FETs have identical parameters, verify that the voltage amplification is $V_o/V_s = -\mu/2$ and the output impedance is $\frac{1}{2}[r_d + (\mu + 1)R]$.

(*b*) Given $r_d = 62$ K, $\mu = 10$, $R_1 = 2$ K, and $R_2 = 1$ K. Find the voltage gain and the output impedance.



Prob. 10.15



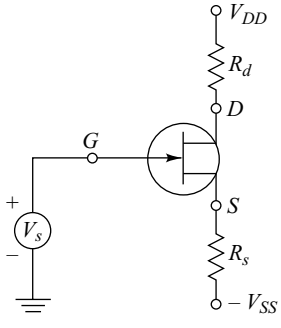
Prob. 10.16

10.17 (*a*) If in the amplifier stage shown the positive supply voltage V_{DD} changes by $\Delta V_{DD} = v_a$, how much does the drain-to-ground voltage change?

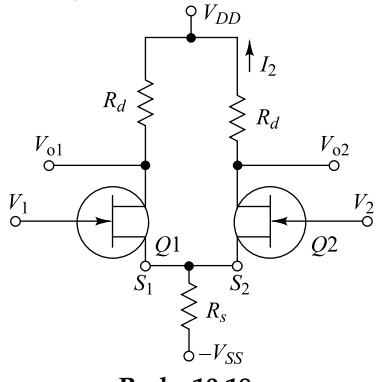
(*b*) How much does the source-to-grouud voltage change under the conditions in part *a*?

(*c*) Repeat parts *a* and *b* if V_{DD} is constant but V_{SS} changes by $\Delta V_{SS} = v_s$.

10.18 If in the circuit shown $V_2 = 0$, then this circuit becomes a source-coupled phase inverter, since $V_{o1} = -V_{o2}$. Solve for the current I_2 by drawing the equivalent circuit, looking into the source of $Q1$. Then replace $Q2$ by the equivalent circuit, looking into its drain. The source resistance R_s may be taken as arbitrarily large.



Prob. 10.17



Prob. 10.18

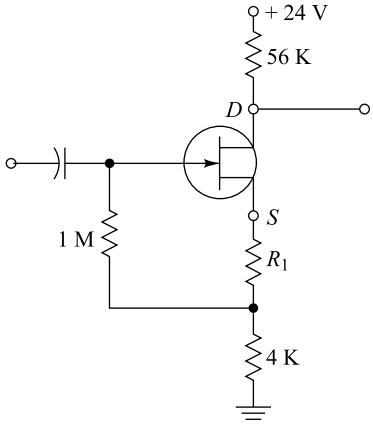
10.19 In the circuit of Prob. 10.25, assume that $V_2 = 0$, $R_d = r_d = 10$ K, $R_s = 1$ K, and $\mu = 19$. If the output is taken from the drain of $Q2$, find (*a*) the voltage gain, (*b*) the output impedance.

10.20 In the circuit of Prob. 10.18, $V_2 \neq V_1$, $R_d = 30$ K, $R_s = 2$ K, $\mu = 19$, and $r_d = 10$ K. Find (*a*) the voltage gains A_1 and A_2 defined by $V_{o2} = A_1 V_1 + A_2 V_2$.

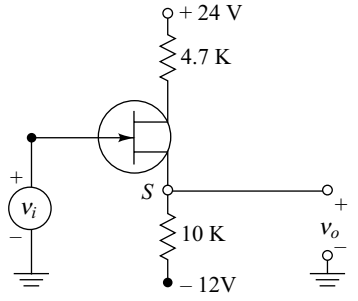
If R_s is arbitrarily large, show that $A_2 = -A_1$. Note that the circuit now behaves as a difference amplifier.

10.21 The CS amplifier stage shown in Fig. 10.16 has the following parameters: $R_d = 12$ K, $R_g = 1$ M, $R_s = 470\ \Omega$, $V_{DD} = 30$ V, C_s is arbitrarily large, $I_{DSS} = 3$ mA, $V_P = -2.4$ V, and $r_d >> R_d$. Determine (*a*) the gate-to-source bias voltage V_{GS}, (*b*) the drain current I_D, (*c*) the quiescent voltage V_{DS}, (*d*) the small-signal voltage gain A_V.

10.22 The amplifier stage shown uses an *n*-channel FET having $I_{DSS} = 1$ mA, $V_P = -1$ V. If the quiescent drain-to-ground voltage is 10 V, find R_1.



Prob. 10.22

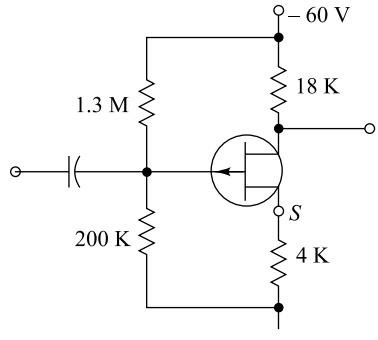


Prob. 10.23

10.23 The FET shown has the following parameters: $I_{DSS} = 5.6$ mA and $V_F = -4$ V.
(*a*) If $v_i = 0$, find v_o.
(*b*) If $v_i = 10$ V, find v_o.
(*c*) If v_o, $= 0$, find v_i.
Note: v_i and v_o are constant voltages (and not small-signal voltages).

10.24 If $|I_{DSS}| = 4$ mA, $V_P = 4$ V, calculate the quiescent values of I_D, V_{GS}, and V_{DS}.

10.25 In the figure shown, two extreme transfer characteristics are indicated. The values of $V_{P,\max}$ and $V_{P,\min}$ are difficult to determine accurately. Hence these values are calculated from the experimental values of $I_{DSS,\,\max}$, $I_{DSS,\,\min}$, $g_{m,\max}$ and $g_{m,\min}$. Note that g_m is the slope of the transfer curve and that both $g_{m,\max}$ and $g_{m,\,\min}$ are measured at a drain current corresponding to $I_{DSS,\min}$. Verify that



Prob. 10.24

(*a*) $$V_{P,\max} = -\frac{2}{g_{m,\min}}(I_{DSS,\max} I_{DSS,\min})^{\frac{1}{2}}$$

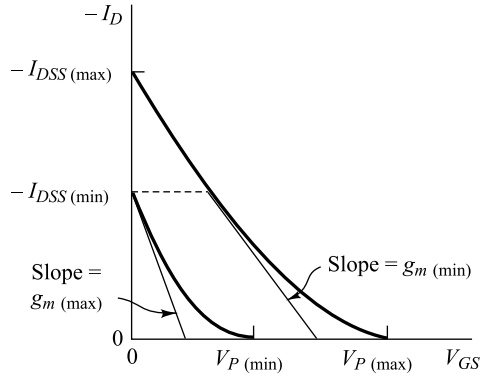
(*b*) $$V_{P,\min} = -\frac{2I_{DSS,\min}}{g_{m,\max}}$$

(*c*) If for a given FET, $I_{DSS,\,\min} = 2$ mA, $I_{DSS,\max} = 6$ mA, $g_{m,\min} = 1.5$ mA/V, and $g_{m,\max} = 3$ mA/V, evaluate $V_{p,\max}$ and $V_{p,\min}$.

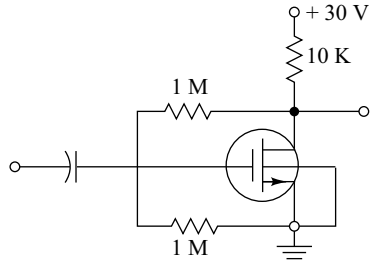
10.26 The drain current in milliamperes of the enhancement-type MOSFET shown is given by

$$I_D = 0.2(V_{GS} - V_P)^2$$

in the region $V_{DS} \geq V_{GS} - V_P$. If $V_P = +3$ V, calculate the quiescent values I_D, V_{GS}, and V_{DS}.



Prob. 10.25



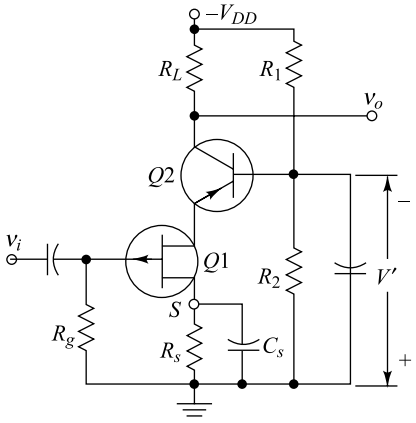
Prob. 10.26

10.27 Show that if $R_L \ll 1/h_{ob2}$, the voltage gain of the hybrid cascode amplifier stage shown is given to a very good approximation by

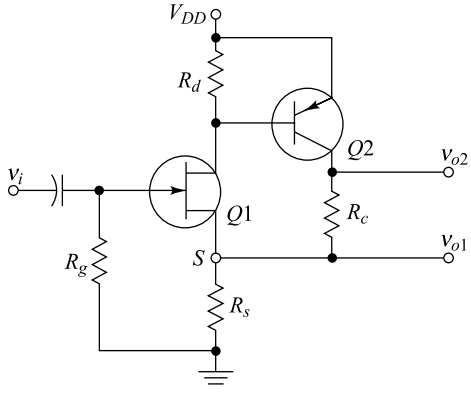
$$A_V = g_m h_{fb} R_L$$

where g_m is the FET transconductance.

10.28 If $h_{ie} << R_d$, $h_{ie} << r_d$, $h_{fe} >> 1$ and $\mu >> 1$ for the circuit, show that



Prob. 10.27



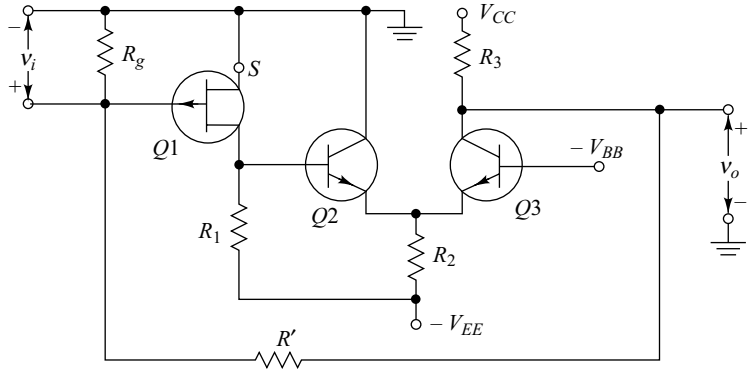
Prob. 10.28

(*a*) $A_{V1} = \dfrac{v_{o1}}{v_i} \approx \dfrac{g_m h_{fe} R_s}{1 + g_m h_{fe} R_s}$ (*b*) $A_{V2} = \dfrac{v_{o2}}{v_i} \approx \dfrac{g_m h_{fe}(R_s + R_c)}{1 + g_m h_{fe} R_s}$

where g_m is the FET transconductance.

10.29 If $r_d >> R_1$, $R_2 >> h_{ib3}$, $1/h_{oe2} >> h_{ib3}$, $R' >> R_3$, and $1/h_{ob3} >> R_3$, show that the voltage gain at low frequencies is given by

$$A_o = \frac{v_o}{v_i} = g_m(1 + h_{fe2})h_{fb3}\,\frac{R_1 R_3}{R_1 + h_{ie2} + h_{ib3}(1 + h_{fe2})}$$



Prob. 10.29

10.30 In the circuit shown, the FET is used as an adjustable impedance element by varying the dc bias, and thereby the g_m of the FET.

(*a*) Assume that there is a generator V between the terminals A and B. Draw the equivalent circuit. Neglect interelectrode capacitances.

(*b*) Show that the input admittance between A and B is

$$Y_i = Y_d + (1 + g_m R)Y_{CR}$$

where Y_d is the admittance corresponding to r_d, and Y_{CR} is the admittance corresponding to R and C in series.

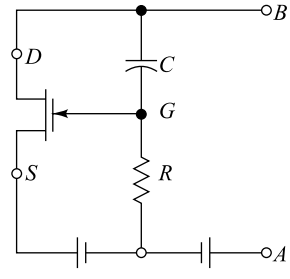
(*c*) If $g_m R >> 1$, show that the effective input capacitance is

$$C_i = \frac{g_m \alpha}{\omega(1 + \alpha^2)}$$

and the effective input resistance is

$$R_i = \frac{(1 + \alpha^2) r_d}{1 + \alpha^2 (1 + \mu)}$$

where $\alpha \equiv \omega CR$.



Prob. 10.30

(*d*) At a given frequency, show that the maximum value of C_i (as either C or R is varied) is obtained when $\alpha = 1$, and

$$(C_i)_{\max} = \frac{g_m}{2\omega}$$

Also show that the value of R_i corresponding to this C_i is

$$(R_i)_{\max} = \frac{2 r_d}{2 + \mu}$$

which, for $\mu >> 2$, reduced to $(R_i)_{\max} = 2/g_m$.

10.31 Solve Prob. 10.30 if the capacitance C is replaced by an inductance L.

10.32 (*a*) A MOSFET connected in the CS configuration works into a 100-K resistive load. Calculate the complex voltage gain and the input admittance of the system for frequencies of 100 and 100,000 Hz. Take the interelectrode capacitances into consideration. The MOSFET parameters are $\mu = 100$, $r_d = 40$ K, $g_m = 2.5$ mA/V, $C_{gs} = 4.0$ pF, $C_{ds} = 0.6$ pF, and $C_{gd} = 2.4$ pF. Compare these results with those obtained when the interelectrode capacitances are neglected.

(*b*) Calculate the input resistance and capacitance.

10.33 Calculate the input admittance of an FET at 10^3 and 10^6 Hz when the total drain circuit impedance is (*a*) a resistance of 50 K, (*b*) a capacitive reactance of 50 K at each frequency. Take the interelectrode capacitances into consideration. The FET parameters are $\mu = 20$, $r_d = 10$ K, $g_m = 2.0$ mA/V, $C_{gs} = 3.0$ pF, $C_{ds} = 1.0$ pF, and $C_{gd} = 2.0$ pF. Express the results in terms of the input resistance and capacitance.

10.34 (*a*) Starting with the circuit model of Fig. 10.31, verify Eq. (10.37) for the voltage gain of the source follower, taking interelectrode capacitances into account.

(*b*) Verify Eq. (10.41) for the input admittance.

(*c*) Verify Eq. (10.42) for the output admittance.

Hint: For part *c*, set $V_i = 0$ and impress an external voltage V_o from S to N; the current drawn from V_o divided by V_o is Y_o.

10.35 Starting with the circuit model of Fig. 10.9, show that, for the *CG* amplifier stage with $R_s = 0$ and $C_{ds} = 0$,

(*a*) $A_V = \dfrac{(g_m + g_d) R_d}{1 + R_d (g_d + j\omega C_{gd})}$ (*b*) $Y_i = g_m + g_d (1 - A_V) + j\omega C_{sg}$

(*c*) Repeat (*a*), taking the source resistance R_s into account.

(*d*) Repeat (*b*), taking the source resistance R_s into account.

10.36 (*a*) For the source follower with $g_m = 2$ rnA/V, $R_s = 100$ K, $r_d = 50$ K, and with each internode capacitance 3 pF, find the frequency at which the reactive component of the output admittance equals the resistive component.

(*b*) At the frequency found in part *a* calculate the gain and compare it with the low-frequency value.