



Contents

Preface to Third Edition	xiii
1. Deep Submicron Digital IC Design	1
1.1 Introduction	1
1.2 Brief History of IC Industry	3
1.3 Review of Digital Logic Gate Design	6
1.3.1 Basic Logic Functions	6
1.3.2 Implementation of Logic Circuits	9
1.3.3 Definition of Noise Margin	11
1.3.4 Definition of Transient Characteristics	12
1.3.5 Power Estimation	14
1.4 Digital Integrated Circuit Design	15
1.4.1 MOS Transistor Structure and Operation	16
1.4.2 CMOS Versus NMOS	17
1.4.3 Deep Submicron Interconnect	19
1.5 Computer-Aided Design of Digital Circuits	24
1.5.1 Circuit Simulation and Analysis	24
*1.6 The Challenges Ahead	26
1.7 Summary	31
2. Transistors and Devices—MOS and Bipolar	35
2.1 Introduction	35
2.2 The MOS Transistor	37
2.2.1 Structure and Operation of the MOS Transistor	37
2.2.2 Threshold Voltage of the MOS Transistor	41
2.2.3 First-Order Current-Voltage Characteristics	52
2.2.4 Derivation of Velocity-Saturated Current Equations	57
2.2.4.1 Effect of High Fields	57
2.2.4.2 Current Equations for Velocity-Saturated Devices	61
*2.2.5 Alpha-Power Law Model	66

2.2.6	Subthreshold Conduction	68
2.2.7	Capacitances of the MOS Transistor	70
2.2.7.1	Thin-Oxide Capacitance	71
2.2.7.2	<i>pn</i> Junction Capacitance	73
2.2.7.3	Overlap Capacitance	79
2.2.8	Summary	81
2.3	Bipolar Transistors and Circuits	83
2.3.1	The Bipolar Junction Transistor	83
2.3.2	The Schottky-Barrier Diode	86
2.3.3	BJT Model for Circuit Simulation	88
2.3.4	Bipolar Transistor Inverter	89
2.3.5	Voltage Transfer Characteristics	90
2.3.6	Schottky-Clamped Inverter	92
2.3.7	BJT Inverter Switching Times	93
2.3.8	Bipolar Digital Gate Circuits	94
2.3.9	Voltage Transfer Characteristics	94
2.3.10	Propagation Delay Time	97
2.3.11	Input Clamp Diodes	97
3.	Fabrication, Layout, and Simulation	103
3.1	Introduction	103
3.2	IC Fabrication Technology	104
3.2.1	Overview of IC Fabrication Process	104
3.2.2	IC Photolithographic Process	106
3.2.3	Making Transistors	107
3.2.4	Making Wires	111
3.2.5	Wire Capacitance and Resistance	114
3.3	Layout Basics	118
3.4	Modeling the MOS Transistor for Circuit Simulation	121
3.4.1	MOS Models in SPICE	121
3.4.2	Specifying MOS Transistors	122
3.5	SPICE MOS LEVEL 1 Device Model	125
3.5.1	Extraction of Parameters for MOS LEVEL 1	127
*3.6	BSIM3 Model	129
3.6.1	Binning Process in BSIM3	129
3.6.2	Short-Channel Threshold Voltage	130
3.6.3	Mobility Model	133
3.6.4	Linear and Saturation Regions	134
3.6.5	Subthreshold Current	136
3.6.6	Capacitance Models	137
3.6.7	Source/Drain Resistance	138

*3.7	Additional Effects in MOS Transistors	139
3.7.1	Parameter Variations in Production	139
3.7.2	Temperature Effects	139
3.7.3	Supply Variations	141
3.7.4	Voltage Limitations	142
3.7.5	CMOS Latch-up	142
*3.8	Silicon-on-Insulator (SOI) Technology	144
*3.9	SPICE Model Summary	146
4.	MOS Inverter Circuits	157
4.1	Introduction	157
4.2	Voltage Transfer Characteristics	158
4.3	Noise Margin Definitions	161
4.3.1	Single-Source Noise Margin (SSNM)	162
4.3.2	Multiple-Source Noise Margin (MSNM)	164
4.4	Resistive-Load Inverter Design	167
4.5	NMOS Transistors as Load Devices	176
4.5.1	Saturated Enhancement Load	176
4.5.2	Linear Enhancement Load	180
4.6	Complementary MOS (CMOS) Inverters	182
4.6.1	DC Analysis of CMOS Inverter	182
4.6.2	Layout Design of CMOS Inverter	190
4.7	Pseudo-NMOS Inverters	192
4.8	Sizing Inverters	195
4.9	Tristate Inverters	198
4.10	Summary	199
5.	Static MOS Gate Circuits	209
5.1	Introduction	209
5.2	CMOS Gate Circuits	211
5.2.1	Basic CMOS Gate Sizing	212
5.2.2	Fanin and Fanout Considerations	216
5.2.3	Voltage Transfer Characteristics (VTC) of CMOS Gates	219
5.3	Complex CMOS Gates	223
5.4	XOR and XNOR Gates	226
5.5	Multiplexer Circuits	228
5.6	Flip-Flops and Latches	228
5.6.1	Basic Bistable Circuit	229
5.6.2	SR Latch	230
5.6.3	JK Flip-Flop	234
5.6.4	JK Master-Slave Flip-Flop	235

5.6.5	JK Edge-Triggered Flip-Flop	236
5.7	D Flip-Flops and Latches	237
5.8	Power Dissipation in CMOS Gates	241
5.8.1	Dynamic (Switching) Power	242
5.8.2	Static (Standby) Power	249
5.8.3	Complete Power Equation	251
5.9	Power and Delay Tradeoffs	252
5.10	Summary	255
6.	High-Speed CMOS Logic Design	263
6.1	Introduction	263
6.2	Switching Time Analysis	265
6.2.1	Gate Sizing Revisited—Velocity Saturation Effects	269
6.3	Detailed Load Capacitance Calculation	271
6.3.1	Fanout Gate Capacitance	272
6.3.2	Self-Capacitance Calculation	274
6.3.3	Wire Capacitance	281
6.4	Improving Delay Calculation with Input Slope	281
6.5	Gate Sizing for Optimal Path Delay	290
6.5.1	Optimal Delay Problem	290
6.5.2	Inverter Chain Delay Optimization—FO4 Delay	291
6.5.3	Optimizing Paths with NANDs and NORs	297
6.6	Optimizing Paths with Logical Effort	300
6.6.1	Derivation of Logical Effort	300
6.6.2	Understanding Logical Effort	306
6.6.3	Branching Effort and Sideloads	311
6.7	Summary	315
7.	Transfer Gate and Dynamic Logic Design	323
7.1	Introduction	323
7.2	Basic Concepts	324
7.2.1	Pass Transistors	324
7.2.2	Capacitive Feedthrough	327
7.2.3	Charge Sharing	330
7.2.4	Other Sources of Charge Loss	332
7.3	CMOS Transmission Gate Logic	332
7.3.1	Multiplexers Using CMOS Transfer Gates	334
7.3.2	CMOS Transmission Gate Delays	339
7.3.3	Logical Effort with CMOS Transmission Gates	345
7.4	Dynamic D-Latches and D Flip-Flops	347
7.5	Domino Logic	350
7.5.1	Logical Effort for Domino Gates	356

7.5.2	Limitations of Domino Logic	357
7.5.3	Dual-Rail (Differential) Domino Logic	360
7.5.4	Self-Resetting Circuits	363
7.6	Summary	363
8.	Semiconductor Memory Design	373
8.1	Introduction	373
8.1.1	Memory Organization	374
8.1.2	Types of Memory	376
8.1.3	Memory Timing Parameters	377
8.2	MOS Decoders	378
8.3	Static RAM Cell Design	382
8.3.1	Static Memory Operation	382
8.3.2	Read Operation	385
8.3.3	Write Operation	388
8.3.4	SRAM Cell Layout	390
8.4	SRAM Column I/O Circuitry	391
8.4.1	Column Pull-Ups	392
8.4.2	Column Selection	394
8.4.3	Write Circuitry	396
8.4.4	Read Circuitry	396
8.5	Memory Architecture	404
8.6	Summary	407
9.	Additional Topics in Memory Design	413
9.1	Introduction	413
*9.2	Content-Addressable Memories (CAMs)	414
*9.3	Field-Programmable Gate Array	421
9.4	Dynamic Read-Write Memories	427
9.4.1	Three-Transistor Dynamic Cell	428
9.4.2	One-Transistor Dynamic Cell	429
9.4.3	External Characteristics of Dynamic RAMs	433
9.5	Read-Only Memories	435
9.5.1	MOS ROM Cell Arrays	435
9.6	EPROMs and E ² PROMs	439
*9.7	Flash Memory	446
*9.8	FRAMs	449
9.9	Summary	450
10.	Interconnect Design	455
10.1	Introduction	455
10.2	Interconnect RC Delays	458

10.2.1	Wire Resistance	458
10.2.2	Elmore Delay Calculation	460
10.2.3	RC Delay in Long Wires	463
10.3	Buffer Insertion for Very Long Wires	467
10.4	Interconnect Coupling Capacitance	471
10.4.1	Components of Coupling Capacitance	471
10.4.2	Coupling Effects on Delay	477
10.4.3	Capacitive Noise or Crosstalk	481
*10.5	Interconnect Inductance	482
*10.6	Antenna Effects	487
10.7	Summary	491
11.	Power Grid and Clock Design	497
11.1	Introduction	497
11.2	Power Distribution Design	498
11.2.1	IR Drop and Ldi/dt	499
11.2.2	Electromigration	502
11.2.3	Power Routing Considerations	505
11.2.4	Decoupling Capacitance Design	507
11.2.5	Power Distribution Design Example	509
11.3	Clocking and Timing Issues	513
11.3.1	Clock Definitions and Metrics	513
11.3.2	Clock Skew	515
11.3.3	Effect of Noise on Clocks and FFs	518
11.3.4	Power Dissipation in Clocks	520
11.3.5	Clock Generation	521
11.3.6	Clock Distribution for High-Performance Designs	523
11.3.7	Example of a Clock Distribution Network	525
11.4	Phase-Locked Loops/Delay-Locked Loops	528
11.4.1	PLL Design Considerations	530
11.4.2	Clock Distribution Summary	536
Appendix A	A Brief Introduction to SPICE	543
A.1	Introduction	543
A.2	Design Flow	544
A.3	Syntax	545
A.3.1	Title	546
A.3.2	Settings of Various Global Parameters	546
A.3.3	Listing of Sources and Active and Passive Elements	548
A.3.4	Analysis Statements	555
A.4	Complete SPICE Examples	559
Index		561