Chapter 5: Power Semiconductor Devices

I POWER TRANSISTORS

In recent years, transistors have become available in high voltage and high current rating. These transistors, called power transistors, are mostly used in the switching mode. In fact, their applications in motor control circuits are becoming increasingly popular. Power transistors are becoming a viable alternative to thyristors. When power transistor conduct an appreciable current, the forward voltage drop (collector emitter saturation voltage) is in the order of 0.3 to 0.8 V as compared to 1.2 to 2 V for thyristors. Therefore, the power loss in a power transistor is lower than that in a thyristor of similar power rating. The switching speed of modern transistors is much higher than that of thyristors and they are extensively employed in d.c.–d.c. and d.c.–a.c. converters, with inverse parallel connected diodes to provide bidirectional current flow. However, the voltage and current ratings of power transistors available at present are not high as those of thyristors and therefore, transistors are normally used in low to medium power applications. Power transistors have no surge current capacity and can withstand only a low rate of change of current.

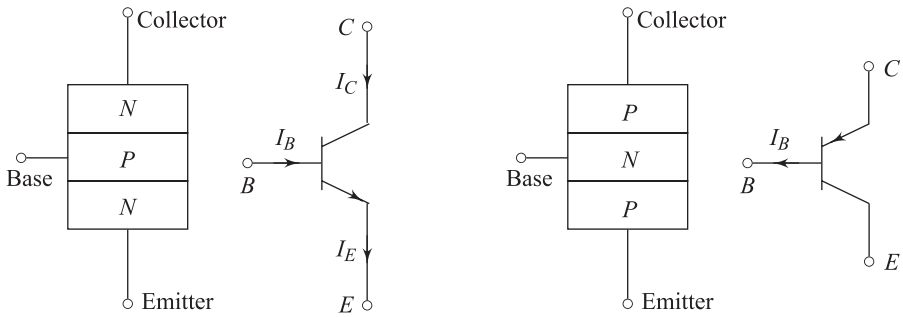
To keep a power transistor in the conducting state, a continuous base current is required. In a high current device, the base-to-collector current gain is as low as 10 and therefore, a base current of several amperes is required to keep the device in the "on" condition. The power loss in the base circuit may be appreciable. If the base current is reduced to zero, the power transistor will turn OFF. However, the turn-off will be slow. For faster turn-on, excess base current is applied. For faster turn-off, the excess charge in the base region must be removed quickly. This can be achieved by reverse-biasing the base during turn-off. The power transistors can be classified broadly into the following categories:

(a) Bipolar junction transistors (BJTs)
(b) Metal oxide semiconductor field effect transistors (MOSFETs)
(c) Insulated-gate bipolar transistors (IGBTs)
(d) Static-induction transistors (SITs)

Due to the pre-eminence of the power bipolar transistor until the late 1970's, the term "power transistor" has been synonymous with "power bipolar transistors." However, in recent years several new device developments have begun to challenge the bipolar transistors. These new devices must now also be regarded as part of the transistor family.

II POWER BIPOLAR JUNCTION TRANSISTORS

As is well known, the bipolar junction transistor is a three-layer device with emitter (E), base (B), and collector (C) regions. The term "bipolar" indicates that current flow consists of a movement of both positive and negative charges, that is, holes and electrons. As indicated in Fig. 5.1 (a), the outer elements may be of N-type material, separated by a P-type base region. This is the N-P-N transistor which has the circuit symbol shown. Alternatively, an N-type base region separates P-type elements, giving the P-N-P transistor, with the circuit symbol of Fig. 5.1(b).



(a) *NPN* transistor (b) *PNP* transistor

Fig. 5.1 *Bipolar transistors*

In each case, the base and emitter form a P-N junction that conducts like a diode in the direction indicated by the arrowhead. For high voltage and high current applications, N-P-N transistors are more widely used because they are easier to manufacture and cheaper to buy.

For a normal transistor operation, the base–emitter junction is forward biased and the emitter acts as a source of mobile carriers which enter the base region, these injected carriers are electrons in the N-P-N transistor and holes in the N-P-N transistor. In general, the emitter region is made of heavily doped material to increase the number of injected carriers, which become minority carriers when they enter the base. Most of these minority carriers diffuse through the base region, which is very narrow, and arrive at the collector base junction. This junction is reversed by an external voltage and hence, the minority base carriers injected by the emitter are swept into the collector region by the electric field at the collector base junction. Figure 5.2 shows the diagrammatic representation of the electron current flow in an N-P-N transistor. Some electron recombine in the base region and do not reach the collector. Hence, collector current, I_C, is slightly less than emitter current, I_E. The difference between these currents is responsible for the small base current, I_B. Thus,

$$I_B = I_E - I_C \tag{5.1}$$

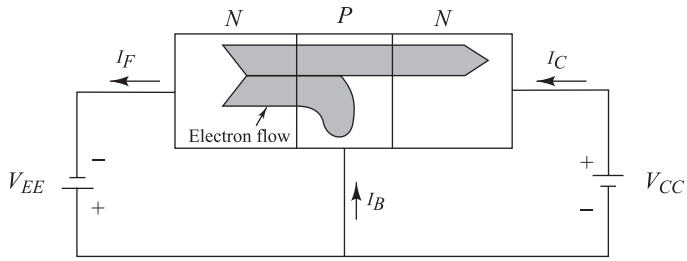


Fig. 5.2 *Electron flow in an NPN transistor*

The ratio of collector to emitter current is defined as the forward current gain, α. Thus,

$$\alpha = \frac{I_C}{I_E} \tag{5.2}$$

and is typically in the range 0.95 to 0.99.

If the current I_E in Fig. 5.2 is reduced to zero by open-circuiting the emitter terminal, there is a small collector leakage current, I_{CBO}, in the reverse-biased collector–base junction.

In practice, the transistor is usually connected in the common-emitter configuration, in which the emitter serves as a common terminal for the input at the base and the output at the collector. This configuration has a high current and power gain. Figure 5.3 shows the common emitter configurations of the *N-P-N* and *P-N-P* transistors. As explained above, operation in the active, or conducting, region requires that the base emitter junction be forward-biased. This implies a base supply voltage, V_{BB}, with the polarity indicated in Fig. 5.3. Simultaneously, the collector base junction is reverse biased by the collector supply voltage, V_{CC}, of appropriate polarity. Normally, V_{CC} is much greater than V_{BB}. As shown in Fig. 5.3(a), both base–emitter and collector–emitter voltages are positive for *N-*

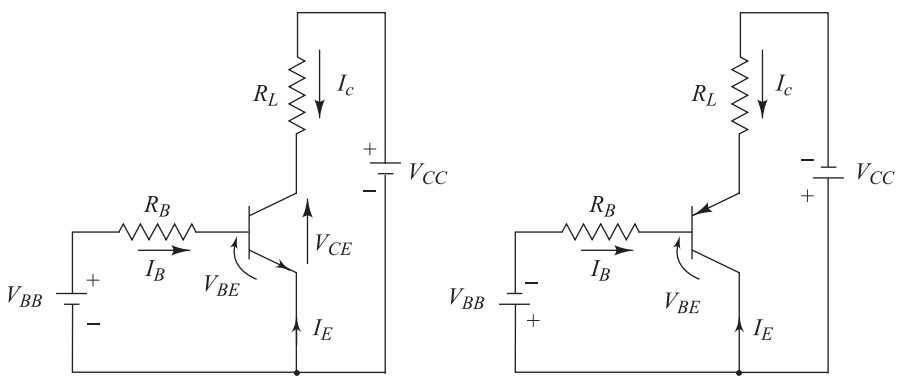


Fig. 5.3 *Common emitter connection of (a) NPN transistor and (b) PNP transistor*

P-N transistors. Conversely, the base–emitter and collector–emitter voltages are both negative for *P-N-P* transistors. The transistor has a very low voltage capability for reverse collector-to-emitter voltages and should not be operated in the reverse mode.

In the common emitter connection, base current I_B is the input current which controls collector current, I_C, at the output. The ratio of d.c. collector current to d.c. base current is the forward current transfer ratio, or current gain, β (or h_{FE}). Thus,

$$\beta = \frac{I_C}{I_B} \tag{5.3}$$

Starting with the current formula $I_E = I_C + I_B$ (Eq. 5.1) and dividing by I_C, we get

$$\frac{I_E}{I_C} = \frac{I_C}{I_C} + \frac{I_B}{I_C} = 1 + \frac{I_B}{I_C}$$

Since $\beta = I_C/I_B$ and $\alpha = I_C/I_E$, the equation becomes

$$\frac{1}{\alpha} = 1 + \frac{1}{\beta}, \quad \text{Rearranging, we get}$$

$$\frac{1}{\alpha} = \frac{\beta + 1}{\beta} \qquad \text{or} \qquad \alpha = \frac{\beta}{\beta + 1} \tag{5.4}$$

Equation (5.4) allows us to calculate α if we know β. By simple algebra, a formula for β in terms of α is derived as follows from Eq. (5.4).

$$\alpha(\beta + 1) = \beta,\ \alpha \cdot \beta + \alpha = \beta,\ \alpha = \beta - \alpha\beta$$

or
$$\beta(1 - \alpha) = \alpha,\ \therefore\ \beta = \frac{\alpha}{1 - \alpha} \tag{5.5}$$

Consequently, for values of α between 0.95 and 0.99, β falls approximately in the range 20 to 100.

1 Common Emitter Characteristics

The output, or collector, characteristics of a transistor in the common-emitter connection plot collector current, I_C, against collector emitter voltage, V_{CE}, for fixed values of base current, I_B. Typical characteristics for an *N-P-N* transistor are shown in Fig. 5.4, where it is evident that collector–emitter voltage exerts little control over collector current. For zero base current, the collector current is very small and the transistor is said "to operate in the cut-off region", corresponding to the off-state. At point *Q* on the rising portion of the collector characteristics, the collector–emitter voltage is small, and the transistor is said "to operate in the saturation region", corresponding to the on-state. Between these two extremes, there is the active, or transition, region where the transistor can operate as a linear amplifier. The product $I_c\ V_{CE}$ gives the power dissipation in the transistor,

assuming the base-power is negligible, and the maximum allowable power dissipation is indicated by the dotted curve in Fig. 5.4. If junction overheating is to be avoided, the transistor must normally operate in the region below this curve.

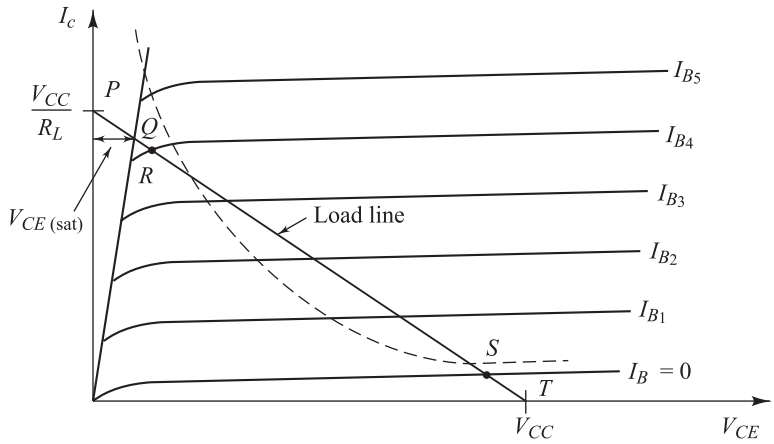


Fig. 5.4 *Collector characteristics for a transistor in C–E mode*

For a particular load registor R_L, as in Fig. 5.3, the collector current, I_c, is given by

$$I_c = \frac{V_{CC} - V_{CE}}{R_L} \tag{5.6}$$

This is the equation of a load line which may be superimposed on the collector characteristics and which represents the locus of all possible operating points. Ideally, when the transistor is fully conducting, there is negligible collector-to-emitter voltage drop, and the full supply voltage, V_{CC}, appears across R_L, producing a current of V_{CC}/R_L. This collector current value locates point P on the vertical axis of Fig. 5.4. Conversely, when the ideal transistor is in the nonconducting, or cut-off region the supply voltage, V_{CC}, appears across the transistor and there is zero collector current. This value locates point T on the horizontal axis of Fig. 5.4. For a purely resistive load, the straight line connecting points P and T is the load-line.

For linear operation in an amplifier circuit, the transistor is biased to an appropriate operating point on the load line. In a switching circuit, however, the transistor is often required to operate as close as possible to the idealized operating points, P and T, corresponding to the saturated and cut-off conditions, respectively. In practice, a large base current will cause the transistor to operate in the saturated condition at point Q with a small saturation voltage, $V_{CE(\text{sat})}$, between the collector and emitter. This value represents the on-state voltage of the transistor and is typically less than 1 V. Full conduction, or hard saturation, gives a low $V_{CE(\text{sat})}$ and minimizes on-state losses. Hard saturation is achieved by supplying excess base current. Thus, as explained above, the collector current at saturation is limited to a value $I_{C(\text{sat})} = V_{CC}/R_L$, and excess base current has no influence on

this value. By forcing a base current, I_B, which is greater than $I_{C(\text{sat})}/h_{FE}$, hard saturation is ensured. The ratio $I_{C(\text{salt})}/I_B$ is called the "forced current gain", β_F, and is obviously less than the natural transistor gain β, or h_{FE}. It should also be noted that in the saturated state, the base–emitter voltage, $V_{BE(\text{sat})}$, is greater than $V_{EC(\text{sat})}$, and, as a result, both transistor junctions are forward biased.

When the base drive current is reduced to zero, the transistor is in the cut-off region at point *S* in Fig. 5.4. A small leakage current, I_{CO}, flows in the collector circuit but this may be significantly reduced by the application of a reverse bias to the base emitter junction. As a result, both transistor junctions are reverse-biased and the operating point moves closer to the ideal operating point, *T*.

In switching applications, the load line may pass through the region of excessive power dissipation, as indicated in Fig. 5.4. When switching between the saturated and cut-off states occurs, the operating point must traverse the active region, and instantaneous power dissipation is high. However, the average power dissipation is not excessive if the operating points *Q* and *S* lie outside the region of excessive power dissipation and if the transistor switches rapidly from one state to the other at moderate repetition frequencies.

2 Switching Performance

(a) Resistive load switching An important application of the transistor is in the ever-increasing area of switching circuits. This broad category of circuits includes applications in such fields as power electronics, digital computers, control systems, counting and timing systems, data processing systems, digital instrumentation, pulse communications, radar, telemetry and television. When it is used as a switch, the transistor is operated in one of the two states, conducting or non-conducting. The non-conducting state is cut-off, while the conducting state may be either in the active region or in the saturation region.

In switching circuits, the cut-off condition is refered to as the "off" condition and the saturated condition as the "on" condition. The active condition retains its name. The transition time between states of a transistor switch is the principle factor limiting the maximum frequency at which switching can occur. As such, it is important to understand the response of a transistor to an input pulse.

Figure 5.5 shows switching waveforms for an *N-P-N* transistor feeding a purely resistive collector load. These waveforms indicate that collector current does not respond immediately to changes in input base current. At $t = 0$, V_{in} is negative, reverse biasing the *E–B* junction, and the transistor is ''off,'' corresponding to the condition in which $I_B \approx 0$ and $I_C \approx 0$. The value of V_{BE} is simply $-V_2$ of reverse bias. At $t = t_1$, V_{in} is suddenly increased to V_1. As shown in figure, the base-emitter voltage increases gradually toward its forward-bias value after V_{in} has switched. As a result, the collector current will not begin increasing toward its saturation value until V_{BE} becomes forward biased. Even then, I_C will increase only gradually towards its saturation value. The time interval from $t = t_1$, when V_{in} switches, to the time when the collector current rises to 10 per cent of its final value is called *delay time*, t_d, as indicated in the figure. The

time it takes the collector current to rise from 10 per cent to 90 per cent of its final value is called *rise-time*, t_r. The sum of the delay time and rise time is the amount of time the transistor takes to turn "on" and is called as turn-on time, t_{on}.

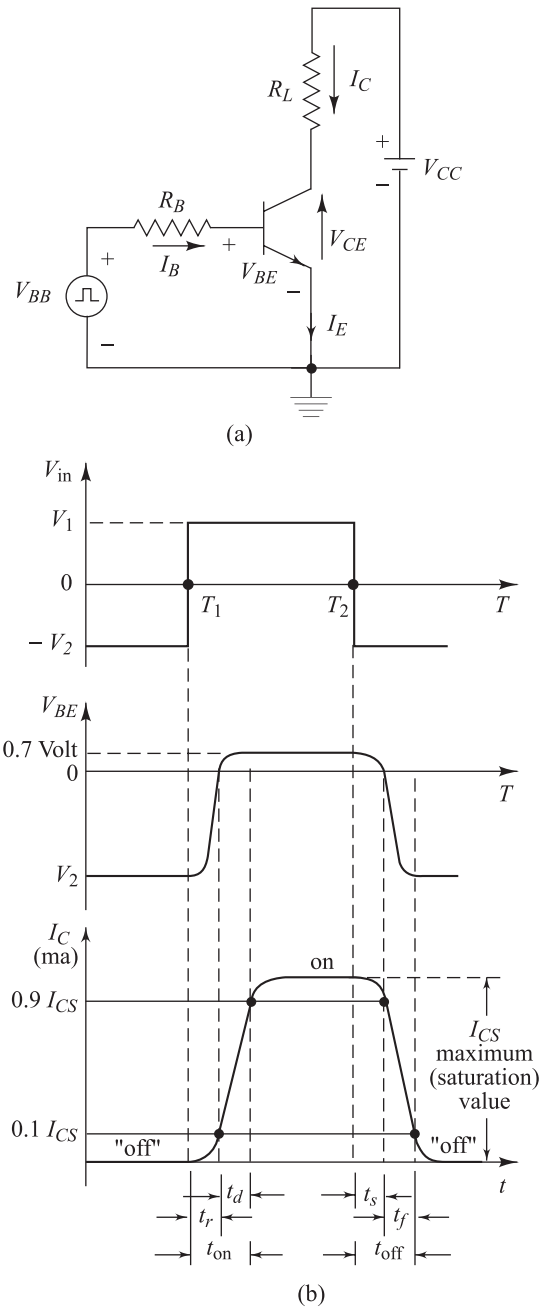


Fig. 5.5 *Transistor switching waveforms for a resistive load*

That is,

$$t_{on} = t_d + t_r \tag{5.7}$$

The turn-on time depends on many factors, including transistor parameters and external circuit components. The principle factors determining t_{on} are:

(1) The transistor junction capacitances which prevent the transistor voltages from changing instantaneously (these junction capacitances must change and discharge gradually through the circuit resistances); and
(2) The time required for the emitter current to diffuse across the base region into the collector region once forward bias is established.

Value of t_{on} ranging from 10–300 nanoseconds are typical and can vary even for the same transistor under different circuit conditions.

Once the collector current reaches its steady state value, it will remain there as long as V_{in} stays at V_1. At $t = t_2$, when V_{in} suddenly returns to $-V_2$, the transistor does not respond immediately. As can be seen in Fig. 5.5, a certain amount of time elapses before I_C even begins to decrease. The storage time, t_s, is defined as the time it takes for the collector current to drop to 90 per cent of its "on" value once the input has switched. The fall time, t_f, is defined as the time it takes the collector current to drop from 90 per cent to 10 per cent. The total turn-off time, t_{off}, is the sum of storage time and full time. That is,

$$t_{off} = t_s + t_f \tag{5.8}$$

The full-time is determined mainly by the same factors which were mentioned in conjunction with turn-on time. The storage time, however, deserves special consideration. It comes about because of the fact that when the transistor is in the "on" state, before switching has occurred, it is saturated. In saturation, the *C–B* junction is forward biased and the collector will inject carriers into the base region in the same way that the emitter does. These charges injected into the base recombine there and are called stored charges. When the transistor is being turned "off", these stored charges must return to the collector region. This process takes time and the movement of these charges maintains the flow of collector current. After all of the stored charge has been removed from the base, the collector current will begin to decrease. The storage time depends on the transistor doping profile but is also dependent on how saturated the transistor is in the "on" state. That is, if I_B is greater than the minimum value needed $[I_{B(sat)}]$ to cause I_C to saturate, the transistor will be essentially overdriven, or oversaturated, and the stored charge will be greater, resulting in a lo nger storage time. As I_B is made larger, the value of t_s and, therefore, t_{off} will increase.

Typical value for t_{off} are in the range of 10–300 and, again, depend not only on the transistor but also on other circuit parameters. The total circuit switching time, T_t, is defined as:

$$T_t = t_{on} + t_{off} \tag{5.9}$$

and is a figure of merit. Its value essentially limits how many times per second the circuit can be pulsed. The smaller the value of T_t, the higher the frequency of switching which the circuit can follow. For example, if the value of T_t is 1 μs,

then we cannot expect the circuit to be able to switch more often than once every 1 μs, or one million times per second. Mathematically, this can be written as

$$f_{\max} = \frac{1}{T_t} \tag{5.10}$$

where $f_{\max}$ is the maximum circuit switching frequency.

(b) Inductive load switching Transistor switching of a resistive load has been studied in previous section. In practice, however, the collector load is usually inductive, at least to the extent that load current remains constant for the duration of the switching interval. Such behaviour is characteristic of the simplified circuit of Fig. 5.6, in which a d.c. supply feeds an inductive load through an *N-P-N* transistor switch. A continuous load current, I_L, is assumed and when the transistor is turned OFF, I_L is diverted into the freewheeling or clamping diode D_1.

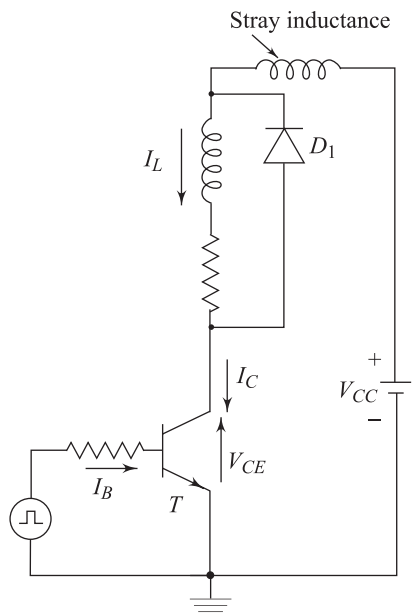


Fig. 5.6 *Switching circuit for a inductive load*

In the switching waveforms of Fig. 5.7, it is assumed that the time constant of the load circuit is large compared with the switching period, T. Consequently, the load current is practically constant and is circulating in the freewheeling diode at time zero when the transistor is turned ON. As the current I_L transfers from diode to transistor, the transistor is subjected to the full collector supply voltage, V_{CC}, as shown in Fig. 5.7, because the conducting diode has a small on-state voltage drop. Thus, the transistor experiences maximum voltage and maximum current simultaneously, and the power dissipation at turn-on is greater than that with a resistive load. When the diode current has totally transferred to the transistor, the diode turns OFF, and the transistor voltage, V_{CE}, decreases rapidly to the saturation voltage, $V_{CE(\text{sat})}$. In practice, the transient characteristics of the freewheeling diode play an important part in circuit behaviour at transistor turn-on because the diode reverse recovery current is carried by the transistor and a fast-recovery diode should be used. Transistor turn-on dissipation can be quite high with a slow recovery diode, but stray circuit inductance, or added series inductance, will ease the problem by delaying the build-up of transistor current.

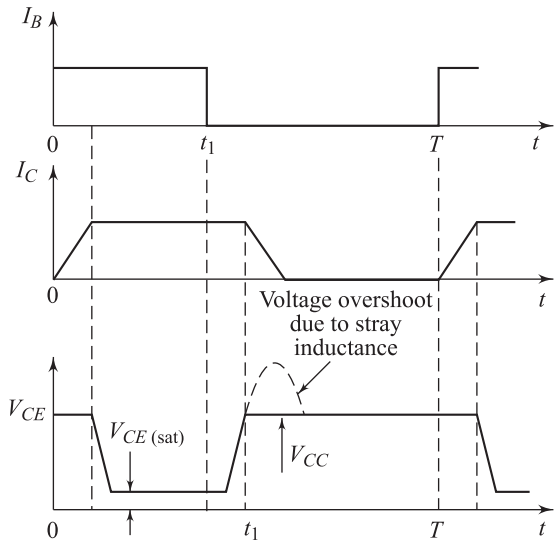


Fig. 5.7 *Switching waveforms*

At turn-off, as shown in Fig. 5.7, the base drive is removed at time t_1, but conduction continues due to free carriers within the base region. After this storage time, the collector–emitter voltage increases rapidly to the d.c. supply voltage, V_{CC}, before the transistor current starts to transfer to the freewheeling diode. Again, this means that turn-off dissipation in the transistor is higher than that with a resistive load. Stray circuit inductance will now cause the collector–emitter voltage to overshoot the supply voltage, V_{CC}, as shown in Fig. 5.7, thereby increasing the instantaneous power dissipation and accentuating the risk of transistor breakdown. In general, the transistor losses at turn-off are much more significant than at turn-on.

3 Breakdown Voltages

A breakdown voltage is defined as the absolute maximum voltage between two terminals with the third terminal open, shorted, or biased in either forward or reverse direction. At breakdown the voltage remains relatively constant, where the current rises rapidly. The following breakdown voltages are quoted by the manufactures:

V_{CEV} or V_{CEX}: The maximum voltage between the collector terminal and emitter terminal at a specified negative voltage applied between base and emitter.

V_{EBO}: The maximum voltage between the emitter terminal and base terminal with collector terminal open circuited.

$V_{CEO(SUS)}$: The maximum sustaining voltage between the collector terminal and emitter terminal with the base open circuited. This rating is specified at the maximum collector current and voltage, appearing simultaneously across the device with a specified value of load inductance.

4 Second Breakdown

Bipolar junction transistors, and to some degree other types of minority carrier devices, have a potential failure mode, usually termed as second breakdown. It appears on the output characteristics of the BJT as a precipitous drop in the collector–emitter voltage at large collector currents. As the collector voltage drops, there is often a significant increase in the collector current and a substantial increase in the power dissipation. What makes this situation particularly dangerous for the bipolar junction transistor is that the dissipation is not uniformly spread over the entire volume of the device, but is concentrated in highly localized regions where the local temperature may grow very quickly to unacceptably high values. If this situation is not terminated in very short time, device destruction results. When devices that have been so destroyed are analyzed, they often show dramatic evidence of the localized power dissipation and attendant heating in the form of melted and then recrystallized silicon.

Second breakdown does not originate from impact ionization and an attendant avalanche breakdown of a *PN* junction. This is clear from the fact that a drop in voltage accompanies second breakdown, whereas no such drop is observed in avalanche breakdown.

Several intrinsic aspects of the transistor combine to give the BJT its susceptibility to second breakdown. First, there is the general propensity of minority carrier devices to thermal runaway when the voltage across them is held approximately constant as the device temperature increases. Minority carrier devices have a negative temperature coefficient of resistivity. This means that the power dissipation will increase as the resistance drops as long as the voltage remains constant. If the rate of increase in power dissipation with temperature is greater than linear with temperature (the rate of heat removal is linear with temperature, i.e., characterized by a thermal resistance), then an unstable situation will result when the power dissipated exceeds the rate at which heat energy can be removed (a function of the thermal resistance). The situation becomes a classic case of positive feedback in which the power dissipation leads to an increase in temperature, which leads to further increase in power dissipation, and so on until device destruction results. It is often and quite appropriately termed thermal runaway. The potential for thermal runaway is made much more dangerous if the current density in the device is non-uniform across the device cross section current filaments when the current density is substantially larger than in surrounding areas may occur and localized thermal runaway becomes likely.

To cause a substantial rise in the temperature of the filament, the formation of the current filaments and subsequent localized thermal runaway requires only a non-uniformity in the current density and enough localized power dissipation. Indeed, the increase in carrier density in the current filament may often cause a drop in the external voltage across the device if the external resistance in series with the device is appreciable, and yet device destruction may still occur. The device is said to be in second breakdown, when the shorting effect of the filament is strong enough to cause this voltage drop.

The second breakdown can be avoided by:

(1) keeping the total power dissipation under control and, more important,
(2) avoiding any current density non-uniformities, especially during turn-on and turn off, when the instantaneous power dissipation is the largest. However, the basic construction of the transistor leads to current constrictions via mechanisms such as emitter current crowding, while current crowding can be postponed until specific current levels are reached. Once these levels are exceeded, the current constriction can be severe enough to lead to the formation of a current filament and to possible localized thermal runaway. One more condition, which is favourable for thermal runaway is the crowding of the emitter current toward the centre of the emitter. To avoid this current crowding, power transistors are constructed with many narrow emitter fingers, in parallel rather than a few very large cross-sectional area emitters. Other measures to reduce the possibility of second breakdown include the use of a controlled rate of change of base current during turn-off, the use of protective circuitry such as snubbers and freewheeling diodes, and the positioning of the switching trajectory within the safe operating area (discussed in the following Section) boundaries.

5 Safe Operating Area (SOA)

(a) Forward biased safe operating area (FBSOA) The capability of the transistor is represented in the form of a safe operating area (SOA or SOAR) in the plane of collector current and collector emitter voltage. The operating locus of collector current and voltage must always lie within this area, even under fault conditions. When the base emitter junction is forward biased to turn ON the transistor, the relevant area is known as the forward bias safe operating area (FBSOA). Figure 5.8 shows typical limits for d.c. and single pulse operation with the usual logarithmic scales for the I_C and V_{CE} axes. Boundary AB is determined by the maximum current capability of the device, with the continuous-current rating as the limit for d.c. operation and the peak current rating setting the limit for pulsed operation. Boundary BC represents the maximum permissible power dissipation at the stated case temperature. This constraint ensures that rated junction temperature is not exceeded. Boundary CD defines the secondary breakdown limit which is related to the formation of the localized hot spots. Boundary DE is the maximum voltage capability as defined by the VCEO(SUS) rating.

Reliable operation of the forward biased transistor requires that its operating point always lie within the FBSOA. This requirement is readily satisfied when the transistor is in the saturated state and operates close to the I_C axis. However, the dynamic load line at turn-on must also lie within the FBSOA. For pulsed operation, the FBSOA is expanded, as shown in Fig. 5.8, because of the small but finite

thermal capacity of the transistor. Modern transistors have turn-on times of a few microseconds, and for these short switching times, the FBSOA is essentially the rectangle bounded by the maximum voltage and current limits.

The manufacturer usually specifies the FBSOA curves for a case temperature of 25°C and for d.c. and single-pulse operation. For normal operation at more realistic case temperatures, and with repetitive pulses, the circuit designer must modify the curves with the help of the transient thermal impedance characteristic of the device.

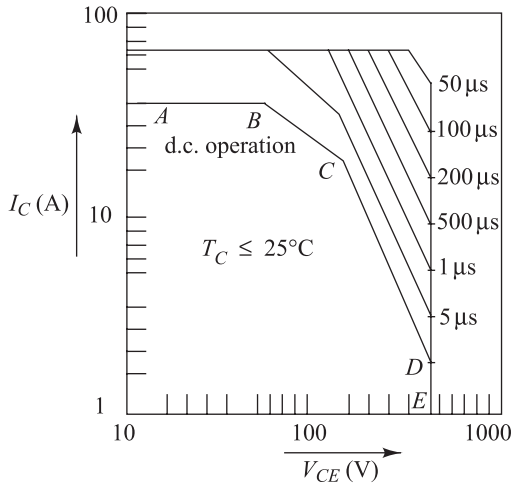


Fig. 5.8 *Typical forward biased safe operating area (FBSOA) for a power transistor*

(b) Reverse biased safe operating area (RBSOA) Transistors are usually more severely stressed at turn-off when they are particularly susceptible to secondary breakdown. It is now common practice to specify a reverse bias safe operating area (RBSOA) which is applicable at turn-off, when the base current is removed or the base–emitter junction is reverse-biased (Fig. 5.9). The RBSOA is smaller than the FBSOA and is usually the limiting factor when a transistor converter is designed. For safe operation under normal or fault conditions, the converter must be designed so that the dynamic load line at turn-off lies within the RBSOA. If this condition is not satisfied, a more rugged transistor is required, or the load-line must be modified by means of a snubber network. As discussed in previous sections, the application of a reverse base–emitter bias minimizes storage time and enhances the OFF condition by reducing the collector leakage current. However, if this reverse bias is applied during the turn-off interval, there is reduction in size of the RBSOA, as shown in Fig. 5.9, and a greater possibility of secondary breakdown.

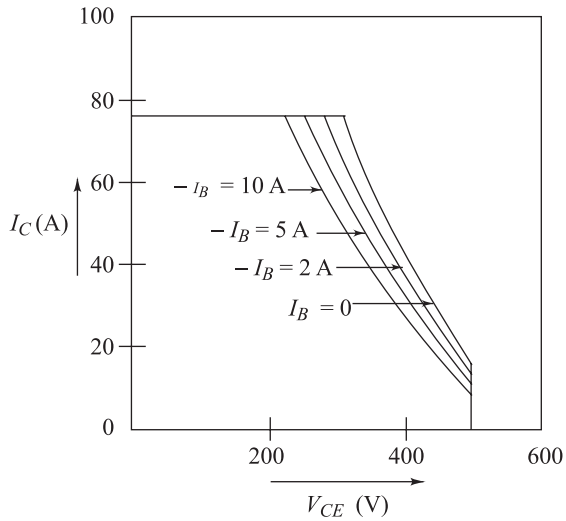


Fig. 5.9 *Typical reverse biased safe operating area (RBSOA) for a power transistor*

6 Power Transistor Voltage and Current Ratings

(a) Transistor current ratings To avoid destructive overheating of the semiconductor, transistor junction temperature must be limited. For a silicon transistor, the rated junction temperature is typically 150°C. In the on-state, the continuous, or d.c., current ratings of the device must be specified so that the rate of energy dissipation at the junction does not exceed the rate at which heat can be removed. This constraint defines thermal limits for the continuous collector, emitter, and base currents. Peak or pulsed current ratings are also specified, based on the fusing current of bonding wires within the device package. The maximum power that the transistor can dissipate and the continuous current ratings are often specified for a transistor case temperature of 25°C. This temperature is unrealistic for most practical applications, and the transistor must be derated for operation at higher case temperatures.

The maximum usable value of collector current may be limited by factors other than junction temperature. The d.c. current gain, h_{FE}, falls off at high collector currents and the on-state saturation voltage, $V_{CE(\text{sat})}$, increases rapidly, as shown in Fig. 5.10. To reduce $V_{CE(\text{sat})}$ and the associated on-state losses by overdriving the base requires a large base current because of the low h_{FE}, hence, the maximum allowable base current is quickly reached. High values of h_{FE} should be available at rated collector current to provide low values of $V_{CE(\text{sat})}$ with reasonable value of forced gain β_F (= I_C/I_B), and to permit optimization of turn-on time by overdriving the base.

On the basis of gain limit, the continuous collector-current rating is that current which results in a minimum acceptable value of h_{FE}. The circuit designer must be careful when comparing devices because same manufacturer specify a collector

current rating based on a d.c. current gain of 10, while other manufacturer use higher values. Indeed, "Specmanship" is widely practised in semiconductor data sheets, with the result that the maximum usable continuous collector current at normal operating junction temperatures may be only 60 or 70 per cent of the headlined continuous rating.

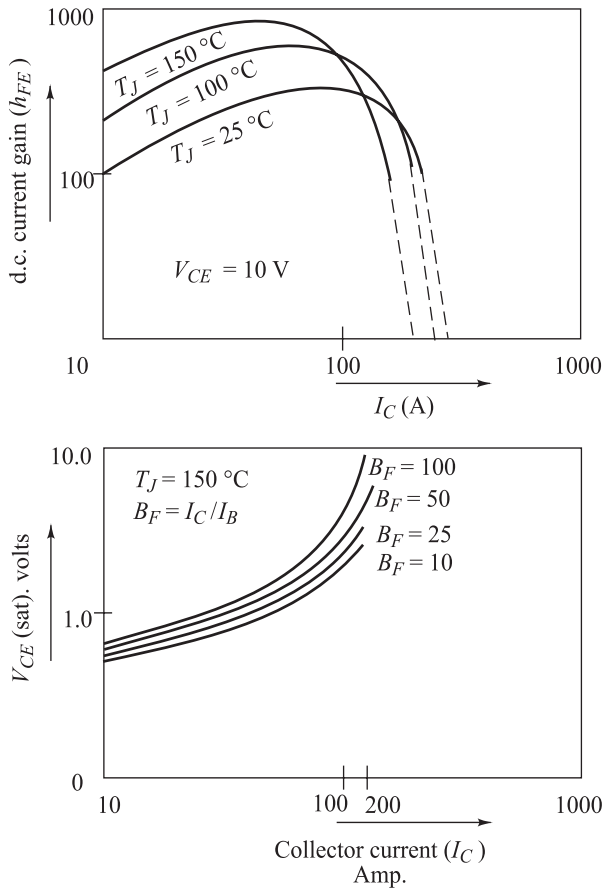


Fig. 5.10 *Variation of d.c. current gain h_{FE}, and $V_{CE\,(sat)}$, as a function of I_C*

Most transistor parameters are affected by junction temperature. At high collector currents, an increase in junction temperature raises the saturation voltage and increases the switching times. Data sheet values for a junction temperature of 25°C are unduly optimistic for normal operating junction temperatures of 150°C to 200°C. Thus, the saturation voltage specification is meaningless without the corresponding values of collector current, base current, and junction temperature.

(b) Transistor voltage ratings Like all semiconductor devices, the power transistor cannot be subjected to excessive voltage without suffering breakdown.

In general, a breakdown of either transistor junction occurs when the applied reverse voltage is increased to a value that causes the leakage current to dislodge additional carriers, thereby initiating avalanche breakdown. For the emitter–base junction, the breakdown voltage $V_{(BR)EBO}$, is typically about 6 V. When the collector base junction is reverse-biased with the emitter open circuited, there is a small collector leakage current, I_{CBO}, until the breakdown voltage, V_{CBO}, is exceeded. This is the highest voltage rating for the transistor.

There are a number of collector-to-emitter voltage ratings, in the usual common emitter configuration, each one being specified for particular base-emitter conditions. Across the collector-base junction, most of the applied collector-to-emitter voltage appears as a reverse bias, producing the leakage current, I_{CBO}. This current flows across the interval base–emitter junction if the base terminal is open circuited, producing by transistor action, a collector current of $h_{FE}\, I_{CBO}$. Therefore, the total collector leakage current is,

$$I_{CEO} = I_{CBO}\,(1 + h_{FE}) \tag{5.11}$$

where $(1 + h_{FE})$ is much greater than unity. Consequently, the junction power limit is reached at a lower voltage than before, and the collector-to-emitter breakdown voltage for this condition is V_{CEO}.

The multiplying transistor action is diminished if the collector leakage current, I_{CBO}, is partially diverted away from the emitter base junction, thereby reducing the total collector leakage current and enhancing the collector-to-emitter voltage capability. By connecting a resistor, R, between the base and emitter terminals, this outcome can be achieved. The resulting collector-to-emitter breakdown voltage is designated by V_{CER}. The collector to emitter breakdown voltage is termed V_{CES} when the base and an emitter terminals are short circuited. When the base–emitter junction is reverse biased by an external voltage, V, a more effective diversion of the base–emitter current is achieved. The resulting collector-to-emitter breakdown voltage is termed as V_{CEV}.

The various breakdown voltages listed above define the ability of the transistor to block voltage at very low collector currents without destroying itself. In general, when collector-to-emitter breakdown commences and the leakage current rises, the flow of collector current is enhanced by transistor action, causing a regenerative build-up of current. The collector-to-emitter breakdown voltage then collapses to the same value regardless of the base condition. This breakdown voltage, which is also relatively insensitive to changes in collector current, as shown in Fig. 5.11, is termed the collector-to-emitter

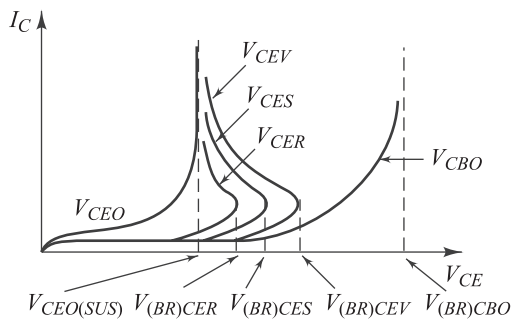


Fig. 5.11 *Collector–emitter avalanche characteristics of a transistor*

sustaining voltage with the base open circuited, $V_{CEO(SUS)}$. This is the most critical voltage rating for the device (power transistor) and is a measure of the voltage capability of the device when high current in an inductive load is interrupted. Transistor manufacturers often recommend that the $V_{CEO(SUS)}$ rating should not be exceeded by high supply voltages, inductive voltage spikes, or any other voltage transient; but the device's voltage switching capability can be extended beyond $V_{CEO(SUS)}$ with proper control of the operating locus and appropriate base drive conditions.

There is a further restriction on the operating region of the power transistor due to the onset of secondary breakdown, in addition to the junction thermal limits and the operating limits on voltage and current.

7 Transistor Thermal Equivalent Circuit

The thermal equivalent circuit of a transistor is shown in Fig. 5.12. If the total average power loss is P_{av}, the case temperature is

$$T_C = T_J - P_{av}\,\Theta_{JC}$$

The sink temperature is

$$T_S = T_C - P_{av} \cdot \Theta_{CS}$$

The ambient temperature is

$$T_A = T_S - P_{av}\,\Theta_{SA}$$

and
$$T_J - T_A = P_{av}\,(\Theta_{JC} + \Theta_{CS} + \Theta_{SA}) \qquad (5.12)$$

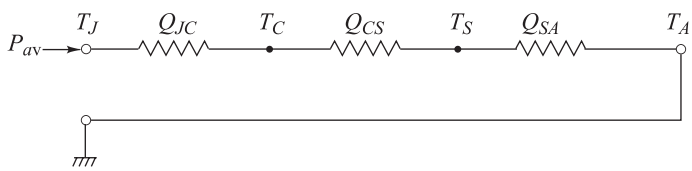


Fig. 5.12 *Thermal equivalent circuit*

where Q_{JC} = thermal resistance from junction to case, $O_{C/\omega}$.
Q_{CS} = thermal resistance from case to sink, $O_{C/\omega}$.
Q_{SA} = thermal resistance from sink to ambient, $O_{C/\omega}$.

The maximum power dissipation P_{av} is normally specified at $T_C = 25°C$. If the ambient temperature is increased to $T_A = T_{J(max)} = 150°C$, the transistor can dissipate zero power. On the other hand, if the junction temperature is $T_J = O_C$, the device can dissipate maximum power and this is not practical. Therefore, while interpreting the ratings of the devices, the ambient temperature and thermal resistances must be considered. Manufacturers shows the derating curves for the thermal derating and second-breakdown derating.

8 Power Darlington Transistor

One of the disadvantages of the power transistor is its relatively low current gain in the saturated state, necessitating substantial base drive current throughout the

on-period. Thus, a power transistor with a collector current of 100 A may require a continuous base current of 10 A in the saturated mode. However, a substantial improvement in gain (100–300), with a consequent reduction in the base drive, is obtained by connecting two transistors in cascade to form what is known as a Darlington connection as shown in Fig. 5.13. In a classical Darlington connection of Fig. 5.13, the input base current requirement of the driver transistor is typically 300 to 500 μA for a collector current of 100 A in the output transistor.

In the modern monolithic power Darlington, the two transistors are fabricated on a single silicon chip. Leakage current stabilization resistors may be added, as shown in Fig. 5.14, and the resulting three terminal device has the characteristics of a high current, high gain transistor.

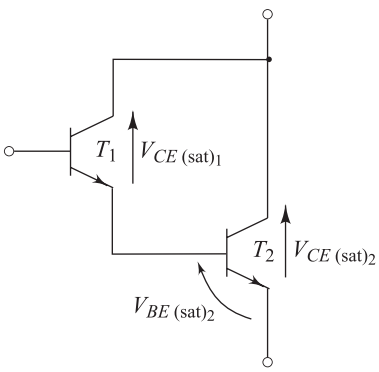


Fig. 5.13 *Basic Darlington connection*

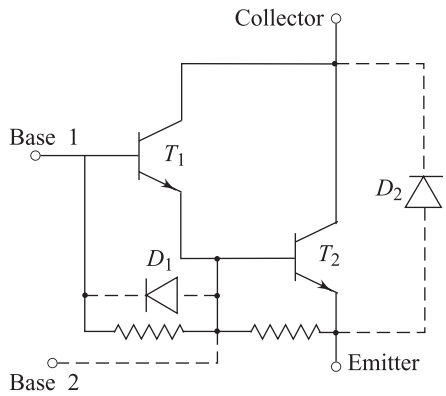


Fig. 5.14 *Typical configuration of monolithic Darlington transistor*

A disadvantage of the Darlington connection is that the collector-to-emitter saturation voltage is somewhat higher than that of a single transistor of the same rating, resulting in a higher on-state power dissipation. This fact can be explained with reference to Fig. 5.13. For a single transistor in the fully saturated condition, the collector-emitter voltage, $V_{CE(sat)}$, is less than the base emitter voltage, $V_{BE(sat)}$. However, it is evident from Fig. 5.12 that the Darlington connection imposes the constraint $V_{CE(sat)2} = V_{CE(sat)1} + V_{BE(sat)2}$. Thus, the $V_{CE(sat)}$ of the output transistor is equal to the $V_{CE(sat)}$ of the input transistor plus the $V_{BE(sat)}$ of the output transistor. For this reason, the output transistor cannot be driven into hard saturation, and because it operates in quasi saturation, it has an increased collector emitter saturation voltage. However, this on-state voltage is not unduly high compared with other power semiconductor devices.

In the basic Darlington connection, the driver transistor must turn-on or off before the transistor begins to turn-on and off. This serial, or sequential, operation inevitably means slow device switching, particularly at turn-off when the storage time of the Darlington is the sum of the storage times of the two transistors. If the switching process is to be accelerated, the output transistor must be switched simultaneously with the input transistor. Faster turn-off may be achieved by the

speed-up diode, such as D_1 in Fig. 5.14. When the base terminal of T_1 is reverse biased at turn-off, diode D_1 provides a path for the reverse base current for T_2, and so speeds up the turn-off process.

In the modern monolithic Darlington, the base of the output transistor is often made accessible at an external terminal, as shown in Fig. 5.14. The output transistor can then be turned ON or OFF simultaneously with the input transistor to optimize the switching performance. The monolithic Darlington transistor also has a parasitic diode, D_2, in inverse parallel with the device, as shown in Fig. 5.14. However, this diode has a long recovery time and cannot be used as a feedback diode in high-frequency inverter circuits. For such applications, several manufactures have introduced a power Darlington with a very fast recovery diode on a separate chip within the device package.

9 Power Transistor Base Drive Control

As discussed in previous sections, the switching speed of the transistor depends on its turn-on and turn-off time. Therefore, by reducing the turn-on time and turn-off, its switching speed can be improved. Turn-on time can be reduced by allowing base current peaking during turn-on resulting in low forced $\beta(\beta_F)$ at the beginning. β_f can be increased to a sufficiently high value to maintain the transistor in the quasi saturation region after turn-on. The turn-off time can be reduced by reversing base current and allowing base current peaking during turn-off. The storage time can be reduced by increasing the value of reverse base current I_{B_2} (Fig. 5.15). A fixed shape of the base current is shown in Fig. 5.15.

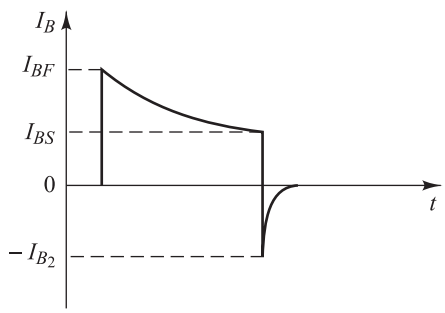


Fig. 5.15 *Base drive current waveform*

Apart from a fixed shape of base current of Fig. 5.15 to match the collector current variations, the forced β may be controlled continuously. For optimizing the base drive of a transistor, the following techniques are commonly used:

(a) Turn-on control
(b) Turn-off control
(c) Proportional base control
(d) Antisaturation control.

(a) Turn-on control During turn-on, the base current peaking can be provided by the circuit of Fig. 5.16. When the input voltage V_1 is applied, the resistor R_1 limits the base current whose initial value is given by the equation

$$I_{B_1} = \frac{V_1 - V_{BE}}{R_1} \tag{5.13}$$

and the final value of the base current is

$$I_{BF} = \frac{V_1 - V_{BE}}{R_1 + R_2} \tag{5.14}$$

The final charging value of the capacitor is given by

$$V_C \cong V_1 \cdot \frac{R_2}{R_1 + R_2} \tag{5.15}$$

and the charging time is given by the equation

$$T_1 = \frac{R_1 \cdot R_2 \cdot C_1}{R_1 + R_2} \tag{5.16}$$

Once the input voltage V_B becomes zero, the base emitter junction is reverse biased and capacitor C_1 discharges through R_2. The discharging time constant is given by $T_2 = R_2\, C_1$. The width of the base pulse must be $t_1 \geq 5T_1$ and the off-period of the pulse must be $t_2 \geq 5T_2$, to allow sufficient charging and discharging times. The maximum switching frequency is, therefore,

$$f_s = \frac{1}{T} = \frac{1}{(t_1 + t_2)} = \frac{0.2}{(T_1 + T_2)} \tag{5.17}$$

(b) Turn-off control In Fig. 5.16, when the input voltage is changed to $-V_2$ during turn-off, the capacitor voltage V_c in Eq. (5.15) is added to V_2 as a reverse voltage across the transistor. During turn off, there will be base current peaking. As the capacitor C_1 discharges, the reverse voltage will be reduced to a steady state value, V_2. A turn-off circuit (using C_2, R_3 and R_4) as shown in Fig. 5.17 may be added, if the different turn-on and turn-off characteristics are required. During turn-off, diode D_1 isolates the forward base drive circuit from the reverse base drive circuit.

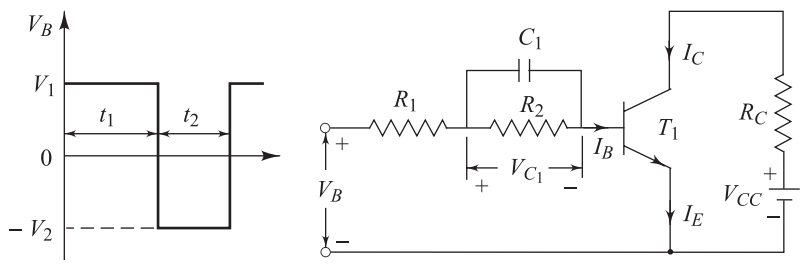


Fig. 5.16 *Base current peaking during turn-on*

(c) Proportional base-control Proportional base drive circuit arrangement is shown in Fig. 5.18. The base drive current is changed in proportion to the collector current, if the collector current changes due to change in load demand. A pulse current of short duration would flow through the base of transistor T_1, when switch S_1 is closed, and T_1 is driven into saturation. Due to the transformer action, a corresponding base current is induced, once the collector current starts

to flow. The transistor would latch on itself, and S_1 can be turned OFF. The turns ratio is $N_2/N_1 = I_C/I_B = \beta$. The magnetizing current, which must be much smaller than the collector current, should be as small as possible for proper operation of the circuit. Switch S_1 can be implemented by a small single transistor, and an additional circuitry is necessary to discharge capacitor C_1, and to reset the transformer core during turn-off of the power transistor.

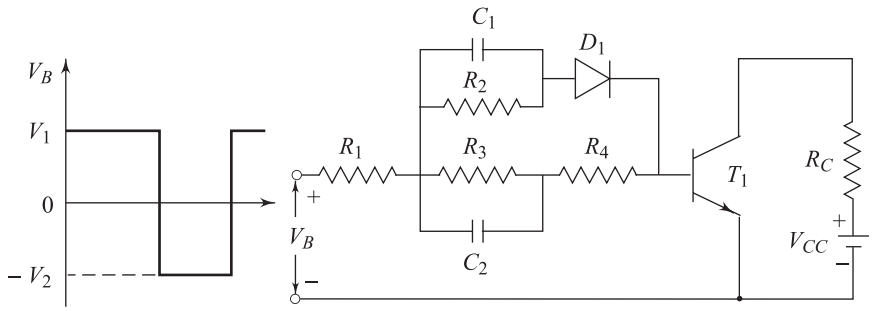


Fig. 5.17 *Base current peaking during turn-on and turn-off*

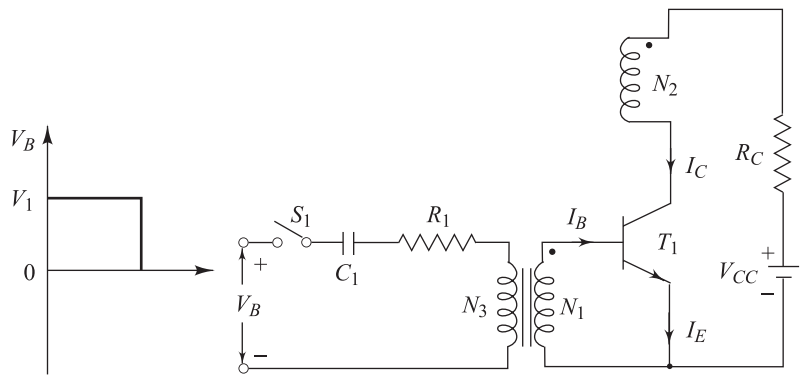


Fig. 5.18 *Proportional base drive circuit*

(d) Antisaturation control The storage time, which is proportional to the base-current increases, if the transistor is driven hard and therefore, the switching speed is reduced. By operating the transistor in soft saturation, the storage time can be reduced. This can be accomplished by clamping the collector–emitter voltage to a predetermined level and the collector current is given by

$$I_C = \frac{V_{CC} - V_p}{R_C} \tag{5.18}$$

where V_P is the clamping voltage and $V_P > V_{CE(\text{sat})}$. A circuit with clamping action (also known as Baker's clamp) is shown in Fig. 5.19.

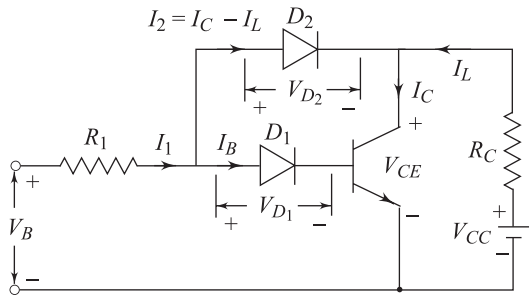


Fig. 5.19 *Collector clamping circuit*

The base current without clamping, which is adequate to drive the transistor hard, can be found from

$$I_B = T_1 = \frac{V_B - V_{D_1} - V_{BE}}{R_B} \tag{5.19}$$

and the corresponding collector current is

$$I_C = \beta \cdot I_B \tag{5.20}$$

After the collector current rises, the transistor is turned ON, and the clamping takes place (due to the fact that D_2 gets forward biased and conducts), then

$$V_{CE} = V_{BE} + V_{D_1} - V_{D_2} \tag{5.21}$$

The load current is given by

$$I_L = \frac{V_{CC} - V_{CE}}{R_C} = \frac{V_{CC} - V_{BE} - V_{D_1} + V_{D_2}}{R_C} \tag{5.22}$$

and the collector current with clamping is

$$I_C = \beta \cdot I_B = \beta(I_1 - I_C + I_L) = \frac{\beta}{1+\beta}(I_1 + I_L) \tag{5.23}$$

For clamping, $V_{D_1} > V_{D_2}$, and this can be accomplished by connecting two or more diodes in place of D_1. The load resistance R_C should satisfy the following condition.

$$\beta I_B > I_L$$

From Eq. (5.22),

$$\beta I_B R_C > (V_{CC} - V_{BE} - V_{D_1} + V_{D_2}) \tag{5.24}$$

The clamping action results in a reduced collector current and almost elimination of the storage time. A fast turn-on is accomplished at the same time. However, due to increased V_{CE}, the on-state power dissipation in the transistor is increased, whereas the switching power loss is decreased.

10 Switching Transistor Protective Networks: RC Snubbers

It is now very clear from the previous discussion that the most critical portion of the switching cycle occurs during transistor turn-off. Normally, reverse-base current is made very large in order to minimize storage time. Unfortunately, this condition may avalanche the base-emitter junction and destroy the transistor. Alternatively, there are two options to prevent this from happening:

(i) turning OFF the transistor at low values of collector-to-emitter voltage V_{CE} and
(ii) reducing collector current with rising collector voltage.

When the power supply design is an off-the-line type, the second solution seems to be the more realistic one. Figure 5.20 shows how this can be accomplished by using an RC snubber network across the transistor to divert collector current during turn-off.

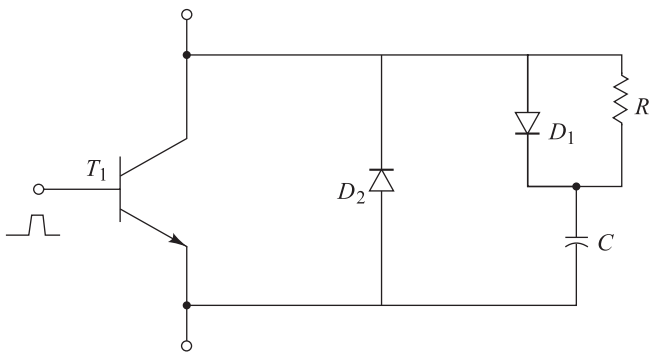


Fig. 5.20 *Turn-off snubber*

Operation When transistor T_1 is OFF, capacitor C is charged through diode D_1 to a voltage ($V_{CC} - V_D$).

When T_1 turns-on, the capacitor discharges through resistor R. The snubber actually dissipates a fair amount of power, thus relieving the switching transistor, which would have to dissipate this power in the absence of the snubber.

Design Procedure (i) The energy area during transistor turn-off is given by

$$E = \frac{1}{2} C \cdot V_{CE}^2 = \frac{1}{2} I_C \cdot V_{CE} \left(t_r + t_f \right) \tag{5.25}$$

where I_C = maximum collector current, A; V_{CE} = maximum collector emitter voltage, V; t_r = maximum collector voltage rise-time, μs; and t_f = maximum collector current fall time, μs

Solving Eq. (5.25) for capacitance C, we get

$$C = \frac{I_C \left(t_r + t_f \right)}{V_{CE}} \tag{5.26}$$

(ii) Capacitor C charges at turn-off and discharges through R during the transistor turn-on time t_{on}. The voltage across the capacitor may be written as

$$V_C = V_{CE}\, e^{-(t_{on}/RC)} \tag{5.27}$$

In order to guarantee a fully charged capacitor prior to turn-off near V_{CE}, we must choose RC such that the expression $e^{-(t_{on}/RC)}$ approaches unity. We must choose RC such that the capacitor will be discharged at the end of the turn-on time ton.

(iii) From basic circuit theory, we know that it takes five time constants (5τ, where $\tau = RC$) for a capacitor to discharge fully through a resistor. Assuming in this case that the capacitor will be essentially at the end of three time constants, the following expression may be derived for maximum discharge resistor value:

$$R = \frac{t_{on}}{3C} \tag{5.28}$$

With value calculated for R in Eq. (5.28), we must check the capacitor discharge current through the transistor at turn-on and restrict it to about 0.25 I_C using the following formula:

$$I_{\text{dis}} = \frac{V_{CE}}{R} \tag{5.29}$$

If the resistor is too low, and $I_{\text{dis}} > 0.25\ I_C$, then R may arbitrarily be raised to fulfill the constraint.

The maximum resistor power rating is given by

$$p_R = \frac{1}{2} C V_{CE}^2 f \tag{5.30}$$

where f is the converter working frequency.

Solved Problems

Example 5.1 During turn-on and turn-off of a power transistor, the current–voltage and current–time relationships are shown in Fig. 5.21. Calculate the energy loss during both turn-on and turn-off periods, and the mean power loss if the transistor is being switched at a frequency of 1 kHz.

Solution: Energy dissipation $= \int_0^t Vi\, dt \quad \therefore \quad I_c = \frac{200}{80 \times 10^{-6}} t = 2.5 \times 10^6\, t$ A,

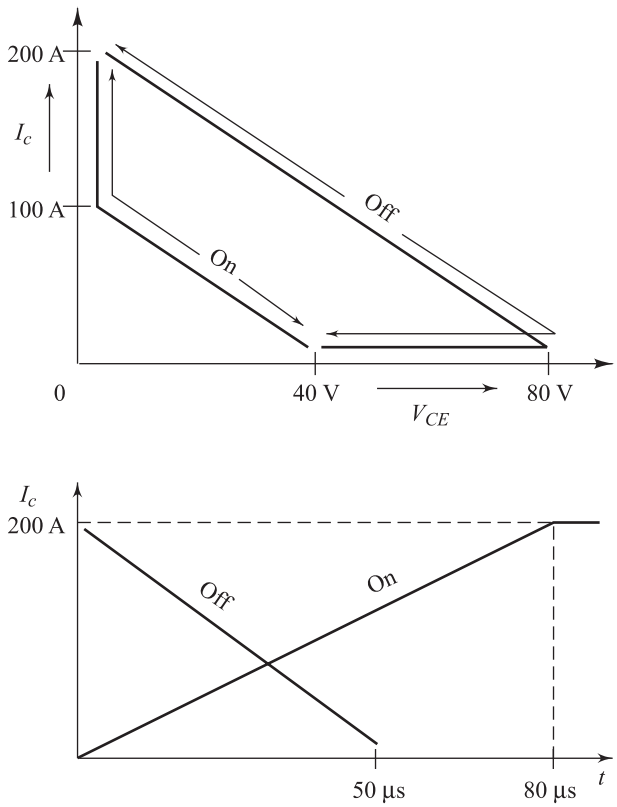


Fig. 5.21 *Current–voltage and current–time relationships*

Also, $I_c = 100 - \dfrac{100}{40} V_{CE}$, from zero to 100 A, giving

$$V_{CE} = 40 - 10^6 t, \text{ from } t = 0 \text{ to } t = 80 \times \frac{80 \times 100}{200} = 40 \text{ μs}.$$

For the time 40 to 80 μs,

$I_c = 100$ mA and V_{CE} is zero.

Hence, the loss is zero in this period.

$$\text{Turn-on energy} = \int_{t=0}^{t=40\mu s} (40 - 10^6 t)(2.5 \times 10^6 t)\,\mathrm{d}t = 27 \text{ mJ}$$

$$\text{Turn-off } I_c = 200 - \frac{200}{50 \times 10^{-6}} t = 200 - (4 \times 10^6) t \text{ A}$$

$$V_{CE} = 80 - \frac{80}{200} I_c = 1.6 \times 10^6\, t \text{ V}.$$

$$\text{Turn-off energy} = \int_{t=0}^{t=50\mu s} (1.6\times10^{6}t)\,[200-(4\times10^{6}t)]\,dt = 133 \text{ mJ}$$

Mean power loss at 1 kHz = $(27 + 133) \times 10^{-3} \times 1000 = 160$ W.

Example 5.2 A transistor has the switching characteristics shown in Fig. 5.22. If the mean power loss in the transistor is limited to 200 W, what is the maximum switching rate that can be achieved?

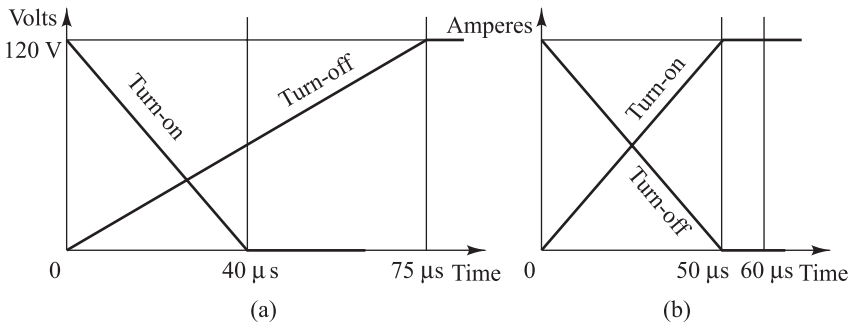


Fig. 5.22 *Switching characteristics*

Solution: Energy loss in transistor = $\int_0^t i_c\, V_{CE}\, dt$.

$$\text{Turn-on energy loss} = \int_0^{40\times10^{-6}} 120\,(1-2.5\times10^{4}t)\times1.6\times10^{6}t\,dt = 51 \text{ mJ}$$

$$\text{Turn-off energy loss} = \int_0^{60\times10^{-6}} 1.6\times10^{6}t\times80\,(1-1.667\times10^{4}t)\,dt = 76.8 \text{ mJ}$$

$\therefore$ Total loss in one cycle = (51 + 76.8) mJ = 127.8 mJ

$$\text{Number of cycle in one second} = \frac{20}{0.1278} = 1564.9.$$

Example 5.3 The beta (β) of bipolar transistor in Fig. 5.3 varies from 15 to 65. The load resistance is $R_L = 10\ \Omega$. The d.c. supply voltage is $V_{CC} = 120$ V and the input voltage to the base circuit is $V_{BB} = 8$ V. If $V_{CE(sat)} = 1.5$ V and $V_{BE(sat)} = 1.75$ V, calculate: (a) the value of RB that will result in saturation with an overdrive factor of 10; (b) the forced b, and (c) the power loss (P_T) in the transistor.

Solution:

Given: $\beta_{min} = 15$, $\beta_{max} = 65.$, $R_L = 10\ \Omega$, $V_{CC} = 120$ V.
$V_{BB} = 8$ V, $V_{CE(sat)} = 1.5$ V $V_{BE(sat)} = 1.75$, Overdrive factor (ODF) = 10.

From Eq. (5.6),

$$I_{cs} = \frac{V_{CC} - V_{CE(\text{sat})}}{R_L} = \frac{120 - 1.5}{10} = 11.85 \text{ A.}$$

Also, $$I_{BS} = \frac{I_{CS}}{I\beta} = \frac{11.85}{\beta_{\min}} = \frac{11.85}{15} = 0.79 \text{ A.}$$

As defined, the ratio of I_B to I_{BS} is called as the overdrive factor, *ODF*:

$$ODF = I_B/I_{BS} \quad \therefore \quad I_B = 10 \times 0.79 = 7.9 \text{ A.}$$

(a) From Fig. 5.3, we can write, $R_B = \frac{V_{BB} - V_{BE(\text{sat})}}{I_B} = \frac{8 - 1.75}{7.9} = 0.79\ \Omega.$

(b) As defined, $$\beta_{f\,(\text{forced }\beta)} = \frac{I_{cs}}{I\beta} = \frac{11.85}{7.9} = 1.5$$

(c) The total power loss in the two junctions of Fig. 5.25 can be written as

$$P_T = V_{BE(\text{sat})}I_B + V_{CE(\text{sat})}I_{CS}. = 1.75 \times 7.9 + 1.5 \times 11.85 = 31.6 \text{ W.}$$

Example 5.4 Typical waveforms of a transistor switch (Fig. 5.5) are shown in Fig. 5.23. The parameters are V_{CC} = 200 V, $V_{BE(\text{sat})}$ = 2.6 V, I_B = 9 A, $V_{CE(\text{sat})}$ = 1.8 V, I_{CE} = 90 A, t_d = 0.4 µs, t_r = 0.8 µs, t_s = 4.5 µs, t_f = 2.5 µs, and f_s = 10 kHz. The duty-cycle (D) is 60%. The collector-to-emitter leakage current is I_{CEO} = 2.8 mA. Calculate the power loss due to collector current:

(a) during turn-on, $t_{\text{on}} = t_d + t_r$,
(b) during conduction period t_c,
(c) during turn-off, $t_{\text{off}} = t_s + t_f$,
(d) during off-time t_0, and
(e) total average power losses, P_T.
(f) Plot the instantaneous power due to collector current, $P_c(t)$.

Solution:

Total time, $T = 1/f_s = 1/10 \times 10^3 = 100$ µs.

Duty-cycle, $D = 0.6$.

But, $D \cdot T = t_d + t_r + t_c = 60$ µs.

$\therefore$ $t_c = 60 - 0.4 - 0.8 = 58.8$ µs.

Also, we can write,

$$(1 - D)T = t_s + t_f + t_0 = 40 \text{ µs}$$

$\therefore$ $t_0 = 40 - 4.5 - 2.5 = 33$ µs.

(a) Now, during delay time, $0 \le t \le t_d$,

$$i_c(t) = I_{CEO}, \qquad V_{CE}(t) = V_{CC}$$

The instantaneous power due to the collector current is given by

$$P_c(t) = i_c V_{CE} = I_{CEO} \cdot V_{CC} = 2.8 \times 10^{-3} \times 200 = 0.56 \text{ W.}$$

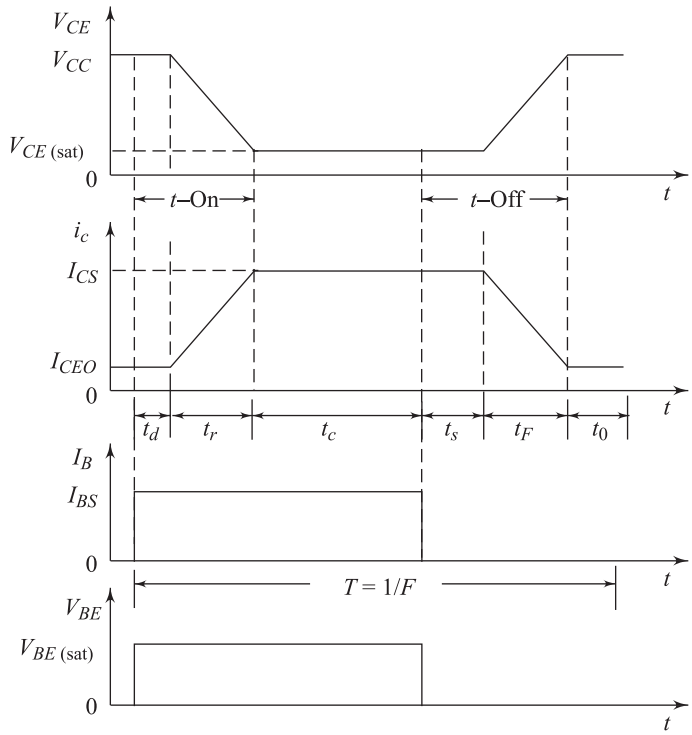


Fig. 5.23 *Waveforms of transistor switch*

The average power loss during the delay time is

$$P_d = \frac{1}{T}\int_0^{t_d} P_c(t)\,\mathrm{d}t = I_{CEO}\ V_{CC}\ t_d f_s \tag{5.31}$$

$$= 2.8 \times 10^{-3} \times 200 \times 0.4 \times 10^{-6} \times 10 \times 10^3 = 2.24 \text{ mW}.$$

During rise time, $0 \le t \le t_r$:

$$i_c(t) = \frac{I_{cs}}{t_r}\,t$$

$$V_{CE}(t) = V_{CC} + (V_{CE(\text{sat})} - V_{CC})\frac{t}{t_r} \tag{5.32}$$

$$P_c(t) = i_c\ V_{CE} = I_{cs}\ \cdot\frac{t}{t_r}\left[V_{CC} + (V_{CE(\text{sat})} - V_{CC})\frac{t}{t_r}\right]$$

The power $P_c(t)$ will be maximum when $t = t_m$, where

$$t_m = \frac{t_r \cdot V_{CC}}{2[V_{CC} - V_{CE(\text{sat})}]} = \frac{0.8 \times 10^{-6} \times 200}{2[200 - 1.8]} = 0.401\ \mu\text{s}. \tag{5.33}$$

and Eq. (5.32) yields the peak power

$$P_{pp} = \frac{V_{CC}^2 I_{cs}}{4[V_{CC} - V_{CE(\text{sat})}]} = (200)^2 \times \frac{90}{4[200 - 1.8]} = 4540.87 \text{ W} \tag{5.34}$$

$$P_r = \frac{1}{T}\int_0^{t_r} p_c(t)\,\mathrm{d}t = f_s \cdot I_{cs} \cdot t_r \left[\frac{V_{CC}}{2} + \frac{V_{CE(\text{sat})} V_{CC}}{3}\right] \tag{5.35}$$

$$= 10 \times 10^3 \times 90 \times 0.8 \times 10^{-6}\left[\frac{200}{2} + \frac{1.8 - 200}{3}\right] = 24.43 \text{ W}.$$

During the turn-on, the total power loss is

$$P_{\text{on}} = P_d + P_r = 0.00224 + 24.43 = 24.43 \text{ W} \tag{5.36}$$

(b) The conduction period, $0 \le t \le t_c$:

$$i_c(t) = I_{cs},\ V_{CE}(t) = V_{CE(\text{sat})}$$
$$P_c(t) = i_c V_{CE} = V_{CE(\text{sat})} I_{cs} = 1.8 \times 90 = 162 \text{ W} \tag{5.37}$$

$$P_n = \frac{1}{T}\int_0^{t_c} P_c(t)\,dt = V_{CE(\text{sat})} \cdot I_{cs} \cdot t_c \cdot f_s$$
$$= 1.8 \times 90 \times 58.8 \times 10^{-6} \times 10 \times 10^3 = 95.26 \text{ W}.$$

(c) The storage period, $0 \le t \le t_s$:

$$i_c(t) = I_{cs},\ V_{CE}(t) = V_{CE(\text{sat})}$$
$$P_c(t) = i_c V_{CE} = V_{CE(\text{sat})} I_{cs} = 1.8 \times 90 = 162 \text{ W} \tag{5.38}$$

$$P_s = \frac{1}{T}\int_0^{t_s} p_c(t)\mathrm{d}t = V_{CE(\text{sat})} I_{cs} t_s \cdot f_s = 1.8 \times 90 \times 4.5 \times 10^{-6} \times 10 \times 10^3 = 7.29 \text{ W}.$$

The fall time, $0 \le t \le t_f$:

$$i_c(t) = I_{cs}(1 - t/t_f), \text{ neglecting } I_{CEO}.$$

$$V_{CE}(t) = \frac{V_{CC}}{t_f} \cdot t \text{ , neglecting } I_{CEO} \tag{5.39}$$

$$P_c(t) = i_c V_{CE} = V_{CC} I_{cs}\left[\left(1 - \frac{t}{t_f}\right)\frac{t}{t_f}\right]$$

This power loss during fall time will be maximum when $t = t_f/2 = 1.25$ μs therefore, peak power,

$$P_m = \frac{V_{CC} I_{cs}}{4} = 200 \times \frac{90}{4} = 4500 \text{ W} \tag{5.40}$$

$$P_f = \frac{1}{T}\int_0^{t_f} p_c(t)\,\mathrm{d}t = \frac{V_{CC} \cdot I_{cs} \cdot t_f \cdot f_s}{6} \tag{5.41}$$

$$= \frac{200 \times 90 \times 2.5 \times 10^{-6} \times 10 \times 10^{3}}{6} = 75 \text{ W}$$

The power loss during turn-off is

$$p_{\text{off}} = p_s + p_f = V_{CC} \cdot I_{cs} \cdot f_s \left(t_s + \frac{t_f}{6} \right) \tag{5.42}$$

$$= 7.29 + 75 = 82.29 \text{ W}$$

(d) Off period, $0 \le t \le t_0$:

$$i_c(t) = I_{CEO}.$$

$$V_{CE}(t) = V_{CC}, P_C(t) = i_C V_{CE} = I_{CEO} \cdot V_{CC} \tag{5.43}$$

$$= 2.8 \times 10^{-3} \times 200 = 0.56 \text{ W}$$

$$P_0 = \int_0^{t_0} p_c(t)\mathrm{d}t = I_{CEO} \cdot V_{CC} \cdot t_0 \cdot f_s. = 2.8 \times 10^{-3} \times 200 \times 33 \times 10^{-6} \times 10 \times 10^{3} = 0.184 .$$

(e) The total power loss in the transistor due to collector current is

$$P_T = P_{\text{on}} + P_n + P_{\text{off}} + P_0 \tag{5.44}$$

$$= 24.43 + 95.26 + 82.29 + 0.184 = 202.164 \text{ W}.$$

(f) Plot of the instantaneous power is shown in Fig. 5.24.

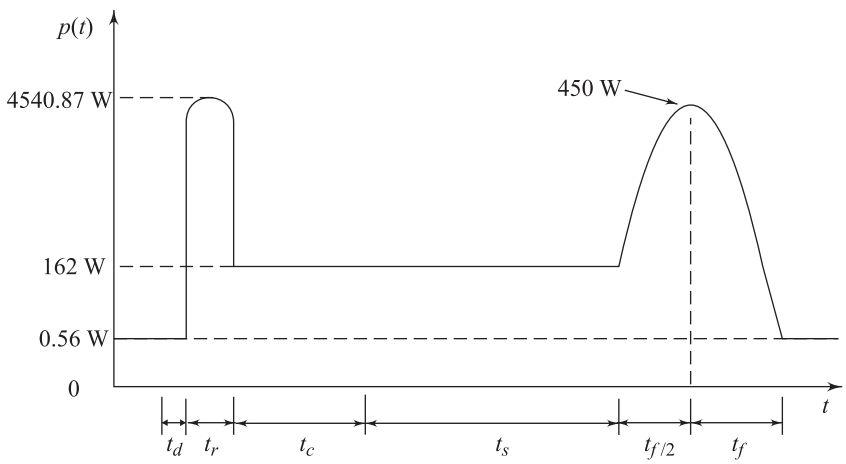


Fig. 5.24 *Instantaneous power plot*

Example 5.5 Compute the average power loss due to the base current for the parameter value of Example 5.4.

Solution: From Example 5.4, we have $V_{BE(\text{sat})} = 2.6\text{V}, I_B = 9 \text{ A}$

$$T = \frac{1}{f_s} = 100 \text{ μs, duty-cycle, } D = 0.6.$$

$\therefore$ $D \cdot T = 0.6 \times 100 \text{ μs} = 60 \text{ μs}.$

$t_d = 0.4\ \mu s$, $t_r = 0.8\ \mu s$, $t_c = 58.8\ \mu s$, $t_s = 4.5\ \mu s$, $t_f = 2.5\ \mu s$,

$t_{on} = t_d + t_r = 1.2\ \mu s$, and $t_{off} = t_s + t_f = 7\ \mu s$.

Now, during the period, $0 \le t \le (t_{on} + t_c)$:

$$i_l(t) = I_{BS}, \qquad V_{BE}(t) = V_{BE(sat)}$$

The instantaneous power due to the base current is

$$P_b(t) = i_b \cdot V_{BE} = I_{BS}\, V_{BS(sat)} = 9 \times 2.6 = 23.4\ \text{W}.$$

During the period, $0 \le t \le t_0 = (T - t_{on} - t_c - t_s - t_f)$, $P_b(t) = 0$. The average power loss is

$$P_{av} = I_{BS}\, V_{BE(sat)}\, (t_{on} + t_c + t_s) f_s \qquad (5.45)$$
$$= 9 \times 2.6 \times (1.2 + 58.8 + 4.5) \times 10^{-6} \times 10 \times 10^3\ P_{av} = 15.093\ \text{W}.$$

Example 5.6 For a power transistor, if the maximum junction temperature is $T_J = 150°C$, the ambient temperature is 30°C. If the thermal impedances are $R_{QJC} = 0.3°C/W$, $R_{QCS} = 0.16°C/W$, and $R_{OSA} = 0.6°C/W$, compute:

(a) the maximum power dissipation, and (b) the case-temperature.

Solution:

(a) $$T_J - T_A = P_T\,(R_{Q_{JC}} + R_{Q_{CS}} + R_{Q_{SA}}) = P_T\, R_{Q_{JA}}$$

$\therefore$ $$R_{Q_{JA}} = 0.3 + 0.16 + 0.6 = 1.06°C/W.$$

$\therefore$ $$1.06\, P_T = 150 - 30$$

$\therefore$ Maximum power dissipation,

$$P_T = 113.21\ \text{W}.$$

(b) The case-temperature can be obtained as

$$T_C = T_J - P_T\, R_{Q_{JC}} = 150 - 113.21 \times 0.3 = 116.04°C.$$

Example 5.7 Two bipolar junction transistors are connected in parallel as shown in Fig. 5.25. Carry a total current of $I_T = 200$ A. The collector–emitter voltage of transistor T_1 is $V_{CE} = 1.5$ V and that of transistor T_2 is $V_{CE_2} = 1.1$ V. Determine the collector current of each transistor and difference in current sharing, if the current sharing series resistances are

(a) $R_{e_1} = 10\ \text{m}\Omega$ and $R_{e_2} = 20\ \text{m}\Omega$, and

(b) $R_{e_1} = R_{e_2} = 20\ \text{m}\Omega$.

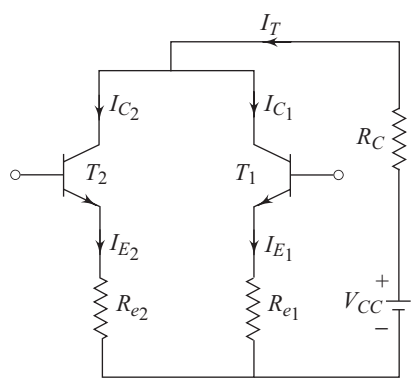


Fig. 5.25 *Parallel connection of transistors*

Solution:

(a) Total current, $I_T = I_{C_1} + I_{C_2}$

and $V_{CE_1} + I_{C_1} \cdot Re_1 = V_{CE_2} + I_{C_2} Re_2.$

Also, $Re_2 \cdot I_{C_2} = Re_2 (I_T - I_{C_1})$

$\therefore$ $V_{CE_1} + I_{C_1} \cdot Re_1 = V_{CE_2} + Re_2 (I_T - I_{C_1})$

or, $V_{CE_1} + I_{C_1} (Re_1 + Re_2) = V_{CE_2} + Re_2 \cdot I_T.$

$$\therefore \quad I_{C_1} = \frac{V_{CE_2} - V_{CE_1} + Re_2 \cdot I_T}{Re_1 + Re_2} = \frac{1.1 - 1.5 + 20 \times 10^{-3} \times 200}{(10 + 20)10^{-3}} = 120 \text{ A or } 60\%.$$

$\therefore$ $I_{C_2} = 200 - 120 = 80$ A or 40%, $\therefore$ $\Delta I = I_{C_1} - I_{C_2} = 60 - 40 = 20\%$

(b) $$I_{C_1} = \frac{1.1 - 1.5 + 200 \times 20 \times 10^{-3}}{(20 + 20)10^{-3}} = 90 \text{ A or } 45\%$$

$\therefore$ $I_{C_2} = 200 - 90 = 110$ A or 55%.

Difference in current sharing $\Delta I = 55 - 45 = 10\%$.

Example 5.8 Figure 5.26 shows the transistor switch-circuit with di/dt and dv/dt protection. Derive the expressions for L_s, C_s and, R_s with associated waveforms and equivalent circuits.

Solution: Protection circuits are normally required to keep the operating di/dt and dv/dt within the allowable limits of the transistor. The operating waveforms are shown in Fig. 5.27. The RC network across the transistor is known as the snubber circuit and limits the dv/dt. The inductor L_s limits the di/dt. Let us assume that under steady-state conditions, the load current I_L is freewheeling through diode D_f, which has negligible reverse-recovery time. When transistor T_1 is turned ON, the collector current rises and current of diode D_f falls because D_f will behave as short-circuited.

Transistors requires certain turn-on and turn-off times. The typical voltage and current waveforms of a BJT switch, neglecting the delay time and the storage time, are shown in Fig. 5.28.

During turn-on, the collector current rises and the di/dt is given by

$$\frac{\mathrm{d}i}{\mathrm{d}t} = \frac{I_L}{t_r} = \frac{I_{cs}}{t_r} \tag{5.46}$$

Now, during turn-off, the collector–emitter voltage must rise in relation to the fall of the collector current, and dv/dt becomes

$$\frac{\mathrm{d}v}{\mathrm{d}t} = \frac{E_{\mathrm{dc}}}{t_f} = \frac{V_{CC}}{t_f} \tag{5.47}$$

The conditions di/dt and dv/dt in Eqs (5.46) and (5.47) are set by the transistor switching characteristics and must be satisfied during turn-on and turn-off.

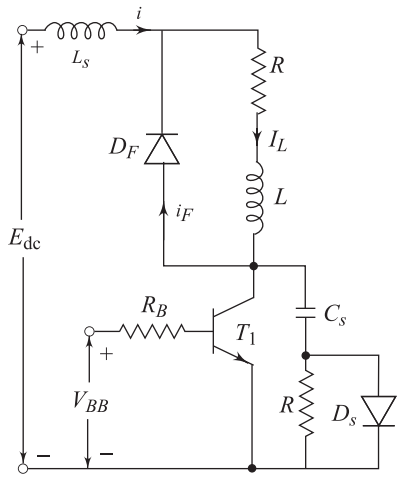


Fig. 5.26 *Transistor switch with di/dt and dv/dt protection*

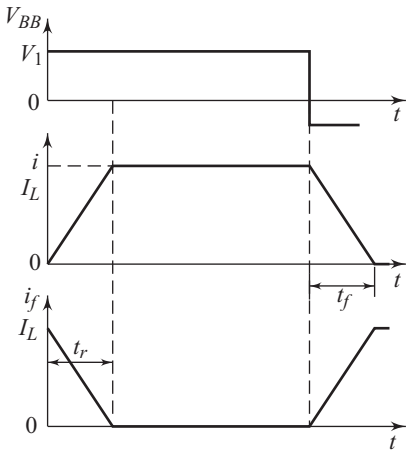


Fig. 5.27 *Associated waveforms*

During turn-on, the equivalent circuit from Fig. 5.26 is shown in Fig. 5.29. The turn-on d*i*/d*t* is given by

$$\frac{\mathrm{d}i}{\mathrm{d}t} = \frac{E_{dc}}{L_s} \tag{5.48}$$

The value of L_s is obtained by equating Eqs (5.46) and (5.48).

$$\therefore \qquad L_s = \frac{E_{dc} \cdot t_r}{I_L} \tag{5.49}$$

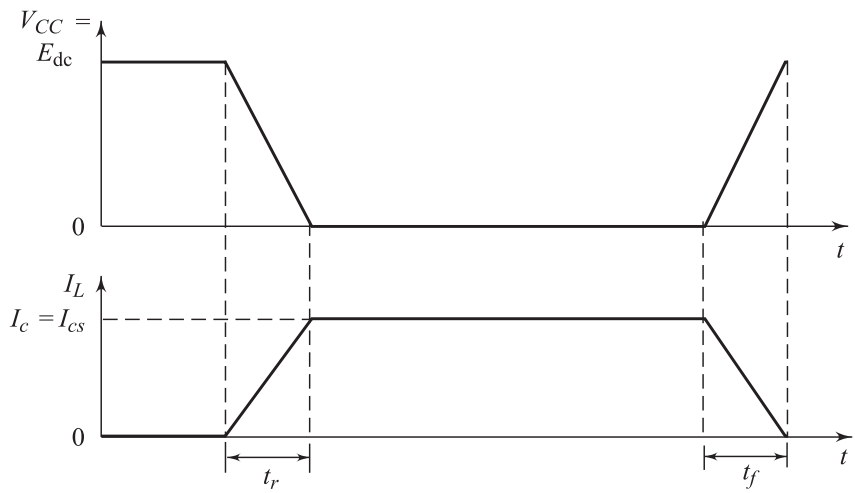


Fig. 5.28 *Voltage and current waveforms*

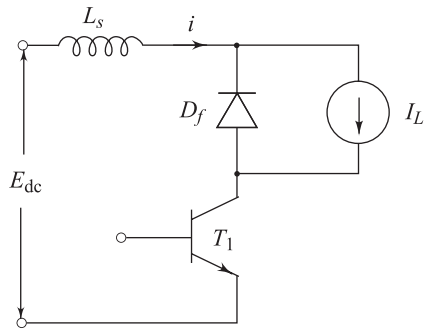


Fig. 5.29 *Equivalent circuit during turn-on*

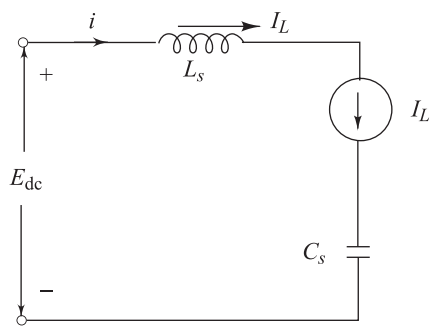


Fig. 5.30 *Equivalent circuit during turn-off*

During turn-off, the capacitor C_s will charge by the load current and the equivalent circuit is shown in Fig. (5.30). The capacitor voltage appears across the transistor and the dv/dt is

$$\frac{dv}{dt} = \frac{I_L}{C_s} \tag{5.50}$$

The required value of the snubber capacitance is obtained by equating Eqs (5.47) and (5.50)

$$\therefore \quad C_s = \frac{I_L t_f}{E_{dc}} \tag{5.51}$$

When the capacitor is charged to voltage E_{dc}, the freewheeling diode D_f will turn-on. Due to the energy stored in L_s, there will be a damped resonant circuit as shown in Fig. 5.31. The RLC circuit is normally made critically damped to avoid oscillations. For unity critical damping, Eq. (13.7) [Chapter 13] of the book yields.

$$R_s = 2\sqrt{\frac{L_s}{C_s}} \tag{5.52}$$

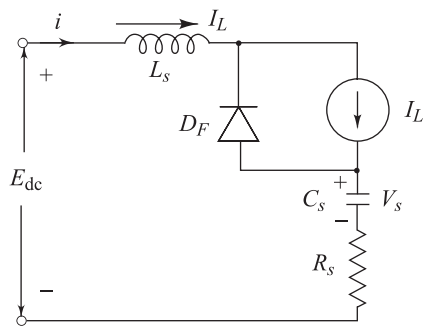


Fig. 5.31 *Damped resonant circuit*

The capacitor C_s has to discharge through the transistor and this increases the peak current rating of the transistor. The discharge through the transistor can be avoided by placing resistor R_s across C_s instead of placing R_s across D_s.

Snubber capacitor discharge current is shown in Fig. 5.32. While selecting the value of R_s, the discharge time, $R_s \cdot C_s = T_s$ should also be considered. A discharge time of one-third the switching period, T_s, is usually adequate.

$$\therefore \quad 3\,R_s C_s = T_s = \frac{1}{f_s} \quad \text{or} \quad R_s = \frac{1}{3 f_s \cdot C_s} \tag{5.53}$$

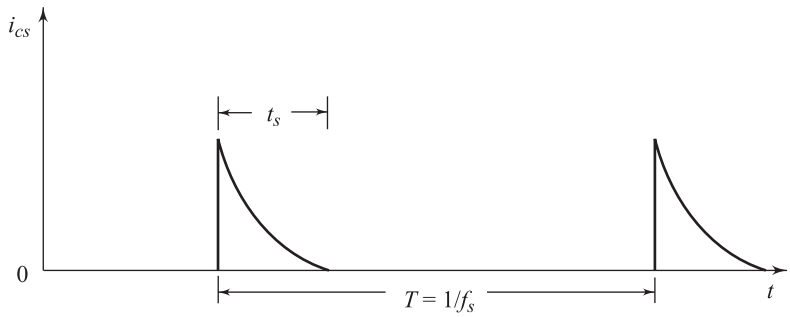


Fig. 5.32 *Discharge current of snubber capacitor*

Example 5.9 Figure 5.26 shows the circuit arrangement of a bipolar transistor which is operating as a chopper switch at a frequency of f_s = 15 kHz. The d.c. input voltage of the chopper is 240 V and the load current is 100 A. The switching times are $t_d = 0$, $t_r = 1.5$ µs and $t_f = 0.7$ µs. Calculate the values of: (a) L_s; (b) C_s; (c) R_s for critically damped condition; (d) R_s, if the discharge time is limited to one-third of switching-period; (e) R_s, if the peak discharge current is limited to 5% of load curent; and (f) power loss due to RC snubber, P_s, neglecting the effect of inductor L_s on the voltage of the snubber capacitor C_s. Assume that $V_{CE(\text{sat})} = 0$.

Solution: $I_L = 100$ A, $E_{dc} = 240$ V, $f_s = 15$ kHz, $t_r = 1.5$ µs and $t_f = 0.7$ µs

(a) From Eq. (5.49), $L_s = \dfrac{E_{dc} \cdot t_r}{I_L} = \dfrac{240 \times 1.5 \times 10^{-6}}{100} = 3.6\,\mu\text{H}.$

(b) From Eq. (5.50), $C_s = \dfrac{I_L \cdot t_f}{E_{dc}} = \dfrac{100 \times 0.7 \times 10^{-6}}{240} = 0.29\,\mu\text{F}.$

(c) From Eq. (5.51) $R_s = 2\sqrt{\dfrac{L_s}{C_s}} = 2\sqrt{\dfrac{3.6 \times 10^{-6}}{0.29 \times 10^{-6}}} = 7.05\,\Omega.$

(d) From Eq. (5.52), $R_s = \dfrac{1}{3 f_s \cdot C_s} = \dfrac{1}{3 \times 15 \times 10^3 \times 0.29 \times 10^{-6}} = 76.63\,\Omega.$

(e) It is given that the peak discharge current is limited to 5% of load current, therefore, we can write:

$$\frac{E_{dc}}{R_s} = 0.05 \times I_L$$

i.e. $\dfrac{240}{R_s} = 0.05 \times 100$ or $R_s = 48\,\Omega.$

(f) The snubber loss, neglecting the loss in diode D_s, is given by

$$P_s \cong 0.5 \times C_s \times E_{dc}^2 \times f_s \tag{5.54}$$

$$\cong 0.5 \times 0.29 \times 10^{-6} \times (240)^2 \times 15 \times 10^3 \cong 125.28\ \text{W}.$$

Example 5.10 Design a snubber network for a switching transistor which is used in a half-bridge converter for following specifications:

$$V_{CE} = 200 \text{ V}, \quad t_f = 2\ \mu\text{s}, \quad t_r = 0.5\ \mu\text{s},$$

converter working frequency = 2 kHz, $I_C = 2\ A$

Solution:

(i) *Step 1: Design of snubber capacitor C* we have the relation,

$$C = \frac{I_C\left(t_r + t_f\right)}{V_{CE}} = \frac{2\left(0.5+2\right)\times 10^{-6}}{200} = 25\ nF = 0.025\ \mu f$$

(ii) *Step 2: Design of snubber resistance R*

Let us assume that t_{on} is 40 percent of the total period (1/*f*).

$$\therefore \quad t_{on} = \frac{0.4\times 10^{-3}}{20} = 20\ \mu\text{s} \quad R = \frac{t_{on}}{3C} = \frac{20\times 10^{-6}}{3\times 0.025\times 10^{-9}} = 303\ \Omega = 300\ \Omega$$

Now,

Check the discharge current

$$I_{\text{dis}} = \frac{V_{CE}}{R} = \frac{200}{300} = 0.67 \text{ A}$$

This is greater than 25 percent of I_C, thus a new R must be calculated.

$$\therefore \qquad R = \frac{V_{CE}}{0.25 I_C} = \frac{200}{(0.25)(2)} = 400\ \Omega = 430\ \Omega$$

Now, power rating of the resistor is given by

$$p_R = \frac{1}{2}\ C\ V_{CE}^2\ f = \frac{1}{2} \times (0.025\times 10^{-6})\ (200)^2 \times 2 \times 10^3 = 1 \text{ W}$$

III GTO Gate Drive Requirement and Circuits

The gate drive requirements of the GTO can be divided into three classes.

(1) During turn-on; (2) On-state; (3) During turn-off.

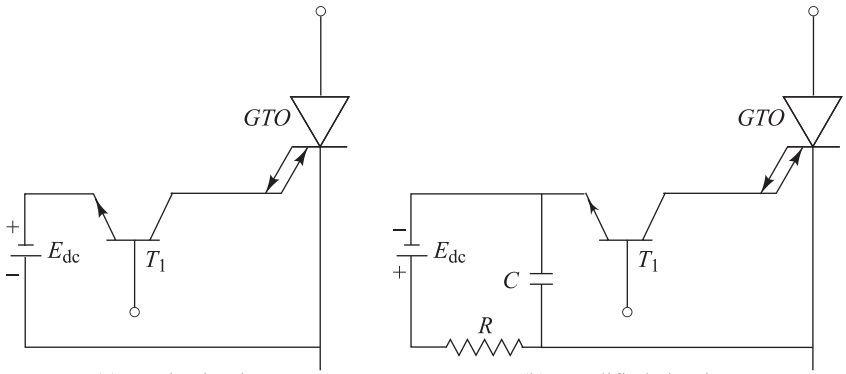
The GTO gating circuits have a great influence on performance and operation of GTO equipment. Since the turn-on process of the GTO is similar to that of the SCR, the on-gating requirements are similar to those of an SCR.

During the on-state, load current greater than the latching current must flow to maintain it in the conducting state. It is recommended that a low on-state gate current must be given during the forward on-state, to prevent any cathode island from dropping out of conduction since unlike the SCR, the GTO has a multi-cathode structure to facilitate the turn-off process.

After triggering, the load current must flow for a certain minimum duration (T_{min}) before the GTO is turned-off. This is to ensure that the junction temperature rise, which has occurred due to the turn-on power dissipation has come down before the turn-off power dissipation occurs. Moreover, the RC snubber should be so designed that the capacitor is fully discharged within T_{min}, otherwise there is a possibility of the forward off-state voltage increasing with a high dv/dt to an excessive value.

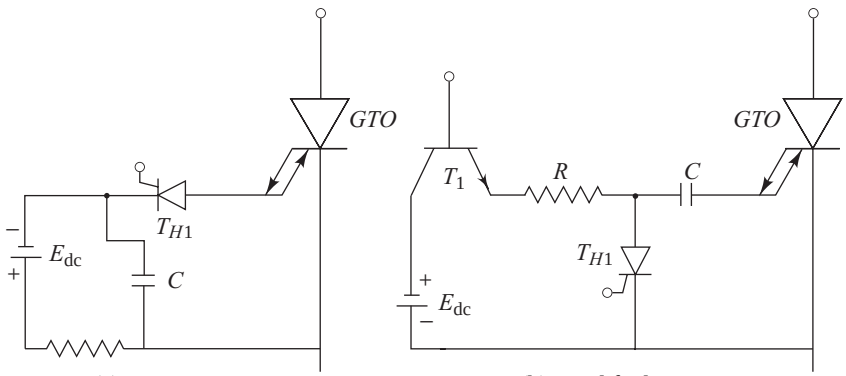
1. Various off-gating circuits The off-gating circuits are the most important for reliable operation of a GTO equipment. Various types of off-gating circuits are shown in Fig. 5.33. Here, we discuss the classification of these typical circuits in brief.

Type I: Power source voltage, E_{dc}, is chosen less than the gate-cathode breakdown voltage $V_{(BR)R}$ in Type I(a). The gate current supplied from a power source becomes nearly zero after the tail current diminishes.



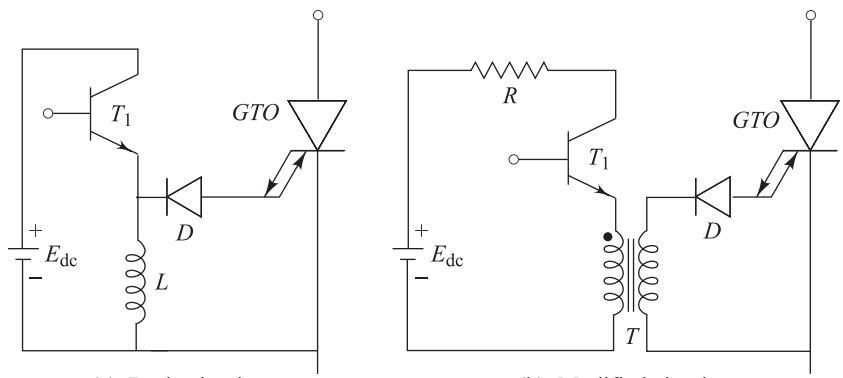
(a) Basic circuit (b) Modified circuit

(i) Type-1 circuits



(a) Basic circuit (b) Modified circuit

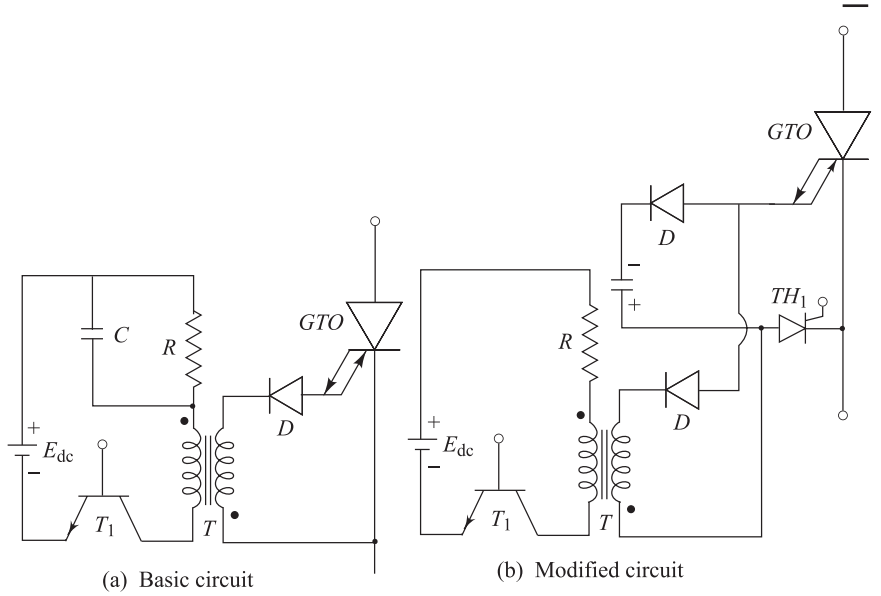
(ii) Type-II circuits



(a) Basic circuit (b) Modified circuit

(iii) Type-III circuits

Fig. 5.33 (*Contd.*)



(iv) Type-IV circuits

Fig. 5.33 *Various off-gating circuits*

The power dissipation of this type is least. But it is hardly expected that the state of rise of gate turn-off current (di_g/dt) is more than 10 A/μs and peak gate turn-off current I_{GP} is more than 100 A. On the other hand, in Type I(b), E_{dc} is chosen higher than $V_{(BR)R}$ so as to improve di_g/dt, hence current limiting resistor R is inserted. The di_g/dt increases in proportion to E_{dc}. But, higher the E_{dc} is, larger the power dissipation becomes. Because the current $(E_{dc} - V_{(BR)R})/R$ flows during the conduction of the transistor T_1 even after the gate cathode impedance has become high power loss decreases with increasing resistance, but increase in time constant RC limits its upper operating frequency.

Type II: Both Types II(a) and II(b) are designed so that the capacitor charge is sufficient to turn-off GTO. In Type II (a), resistance R should be chosen to limit the thyristor current to less than its holding current after the GTO tail current has decreased zero, therefore, the resistance must be of the order of kilo-ohm. Upper frequency becomes necessarily low. In Type II(b), a charging circuit, composed of a transistor, low resistance and a negative d.c. power source, is disconnected while the thyristor TH_1 is turned-on. Practically, capacitor charging current is effectively used as an on-gating current. But larger capacitance needs longer charging time, which restricts minimum conducting period of GTO, or needs larger charging current.

Type III: Reactor current, which has been build up due to a transistor T_1 conduction for a few ten microseconds before turning off a GTO, is transferred to the closed circuit consisting of the reactor, GTO and a diode as soon as the

transistor is switched off. The inductance must be large enough to keep the current flow against increased gate-cathode impedance for several ten microseconds.

Type IV: It is similar to a conventional on-gating circuit of thyristor, but it must have a bigger current capability. Type IV(b) is a modified circuit having two current sources, one current source which supplies a high rate of rise but short duration pulse current and the other which supplies a slow rate of rise but long duration pulse.

Since each type of circuits shown in Fig. 5.33 has merits and demerits, it is selectively used corresponding to its application's requirements or sometimes may be combined with each other.

2. Gate drive for high power GTOs Figure 5.33 shows a gating circuit suitable for high power GTOs including an on-gating, an off-gating and a negative bias circuit. On-gating circuit using pulse-transformer is quite popular to a conventional thyristor. This method is applicable to the on-gating circuit of GTOs. In Fig. 5.33, the primary winding of the transformer PT_2 is connected to a

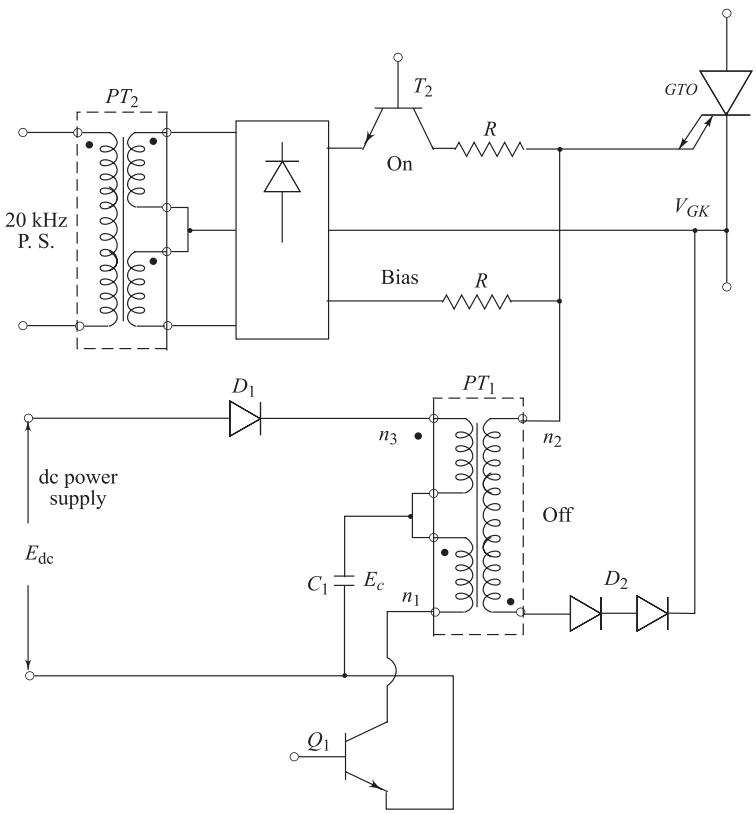


Fig. 5.34 *Gate drive for high power GTOs*

20 kHz power source. The 20 kHz power source would be readily obtainable, for example, by means of slight modification of a switching regulator on the market. Such a power source is rather preferable because d.c. voltage of each on-gating and bias circuits would result in stabilization against line voltage fluctuation. And also, the transformer PT_2 will be decreased in external dimensions. A transistor switch is provided for blocking the flow of off-gating current into the on-gating circuit. No transistor switch is used in the negative bias circuit. In a practical use, a bias current of 0.1 A will be sufficient. Because a large negative off-gating current is flowing during turn-off operation, the dv/dt capability is very high and has no relation to the bias circuit. As shown, diode D_1 is inserted between a pulse transformer PT_1 and the positive terminal of a d.c. power source. Also, capacitor C_1 is connected across the connecting point of PT_1 primary and tertiary windings and the negative terminal of the power-source.

(a) Operating principle of off-gating circuit: The various operating modes of the off-gating circuit are shown in Fig. 5.35, and the waveforms of off-gating circuit for one operating cycle are shown in Fig. 5.36. The operation of the circuit can be explained in various five operating modes as discussed below.

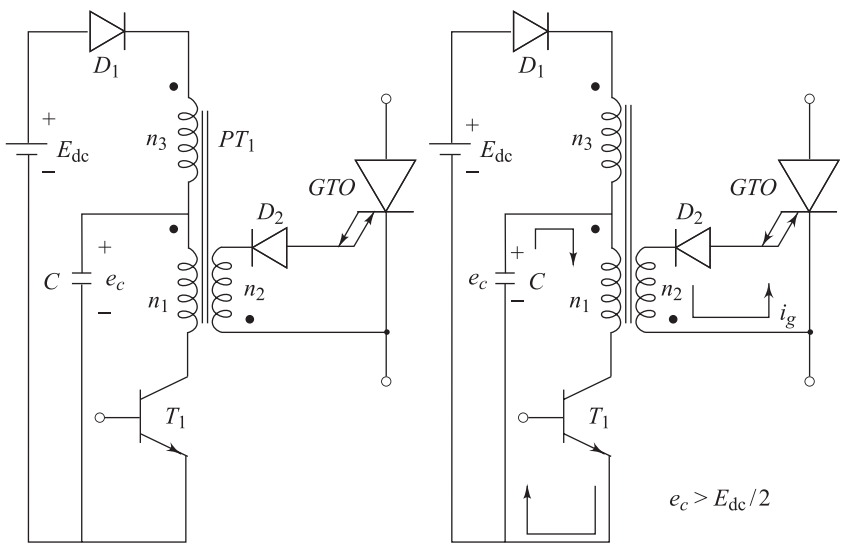


Fig. 5.35 (a) and **(b)**

***Mode 1*:** In this mode of operation, the capacitor C_1 is charged upto the voltage E_c, where E_c is higher than power some voltage E_{dc}.

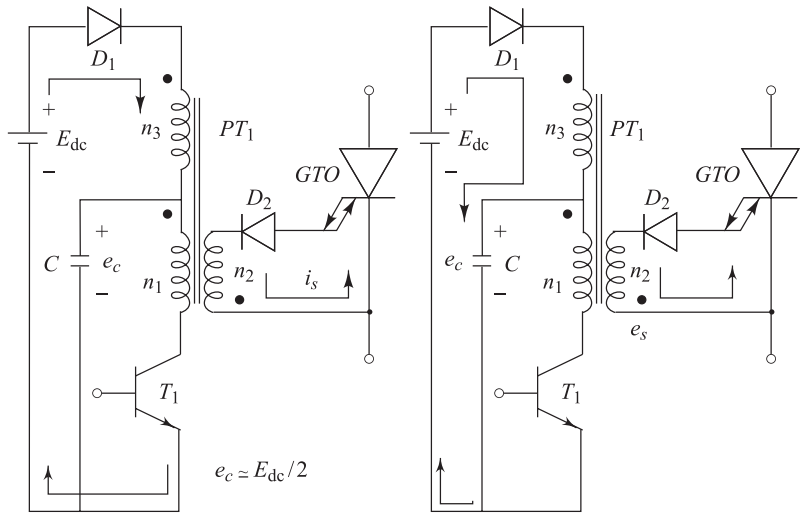
***Mode 2*:** Here, number of turns of primary and tertiary windings are equal. When the transistor T_1 is turned ON, capacitor voltage, E_C, appears across the

winding n_1, thus off-gating current i_g starts to flow. i_g and its initial rate of rise $di_g/dt|_{t=0}$ are approximately given as follows:

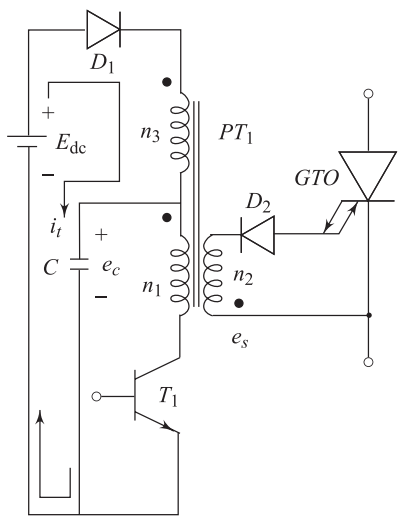
$$I_g = E_c\sqrt{C/L}\sin\left(t/n\sqrt{LC}\right) \tag{5.55}$$

and $$di_g/dt|_{t=0} = E_c/n_1 \tag{5.56}$$

where L is the total inductance reduced to terms of the secondary and $n = n_1/n_2$.



(c) Mode 3 (d) Mode 4



(e) Mode 5

Fig. 5.35 *(c), (d) and (e) Various operating modes of off-gating circuit*

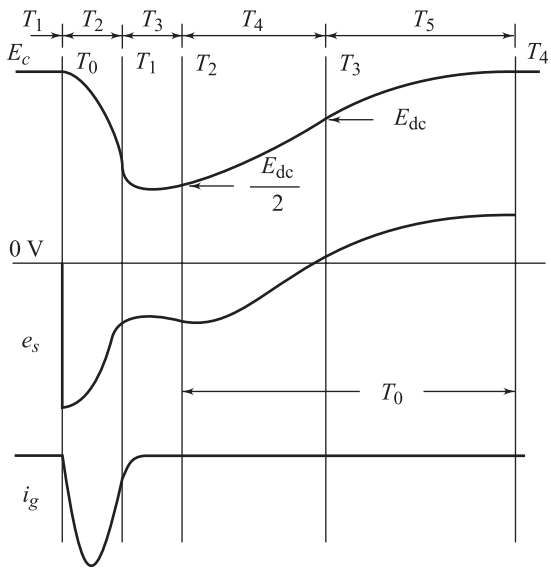


Fig. 5.36 *Waveforms of off-gating circuit for one operating cycle*

Since the voltage equal to the primary voltage induces across the tertiary winding, diode D_1 will block current flowing through the tertiary until the capacitor discharges to $E_{dc}/2$. By the end of Mode 2, the gate cathode junction has reverted to a blocking state, thus the gate-cathode impedance has become high. In case, that on-state current is zero, i_g is given by replacing E_c in Eq. (5.55) by

$(EC - n V_{(BR)R})$:

$$\therefore \qquad i_g = (EC - n V_{(BR)R}) \cdot \sqrt{C/L} \sin\left(t/n\sqrt{LC}\right) \tag{5.57}$$

EC is chosen so as to meet the requirement of the initial rate of rise of off-gating current and normally $E_c > n \cdot V_{(BR)R}$.

Mode 3: When the capacitor voltage reaches the value $E_{dc}/2$, the diode D_1 starts to conduct. E_{dc} is impressed across the primary and tertiary windings in series. The capacitor voltage holds $E_{dc}/2$ and the secondary voltage e_s is given by:

$$e_s = E_{dc}/2n \tag{5.58}$$

If e_s is chosen less than $V_{(BR)R}$, then i_g becomes nearly zero after the tail current has reduced to zero.

Modes 4 and 5: When the transistor T_1 stops conducting, the exciting current, originally flowing in the primary winding, is transferred to the tertiary. Almost all

the energy, stored in pT, is used for recharging C_1 to higher value than E_{dc}. It may be comprehensible from the fact that the capacitor will be charged up to E_{dc} even if no exciting current exists.

Practically, i_g becomes negligibly small during the modes, hence the final value E_c of the capacitor voltage can be approximately obtained by solving the following equations:

$$I_t = \{(E_{dc}/2x) \sin \omega t + I_m \cdot \cos \omega t\} \exp\left(\frac{-\omega t}{2Q}\right) \tag{5.59}$$

$$e_c = E_{dc} + \{X \cdot I_m \sin \omega t - (E_{dc}/2) \cos \omega t\} \cdot \exp(-\omega t/2Q) \tag{5.60}$$

where $X = \sqrt{L_m/C}$, $Q = X/R$, $\omega = 1/\sqrt{L_m \cdot C}$

R is the circuit loss in terms of a resistance, I_m the exciting current and L_m the exciting inductance.

The time T_0 until which capacitor C_1 has been charged, is obtained by putting Eq. (5.59) equal to zero:

$$\omega T_0 = \tan^{-1}(-2XI_m/E_{dc}) \tag{5.61}$$

where $\pi/2 < \omega T_0 < \pi$.

Substituting Eq. (5.61) to Eq. (5.60) gives E_c:

$$E_c = e_c(T_0) = \sqrt{(XI_m)^2 + (E_{dc}/2)^2} \exp\left(\frac{-\omega T_0}{2Q}\right) \tag{5.62}$$

and $XI_m = \omega(L_m \cdot I_m) = \omega \times$ constant determined by volt-second of pulse transformer.

The voltage V_s across the secondary winding is given by $-(E_{dc} - e_c)/n$. When $e_c = E_{dc}$ Mode 4 ends. During Mode 5, e_s becomes positive but diode D_2 blocks current i_g to flow in opposite direction. The rate of decay of V_s at time $t = t_3$ is so slow, and i_g is so small that the diode reverse recovery charge is negligible.

As shown in Fig. 5.34, the off-gating circuit is quite simple. The capacitor C_1 which is charged by the stored-energy of PT_1, provides a higher off-gating pulse. The features of this circuit are as follows:

(1) This circuit operates satisfactorily and power dissipation in the off-gating circuit reduces significantly.

(2) No backswing of PT_1 due to its stored energy appears because of using its energy for charging up capacitor C_1.

IV Paralleling of GTOs

Paralleling with no anode current balancers, i.e. direct paralleling, is useful in simplifying large capacitor power converters. Direct paralleling also makes it easier to replace a large current GTO with paralleled small current GTOs. For the equipment handling a large current, over several hundred amperes, a flat type GTO is used, although it is more expensive than the stud type. By replacing the

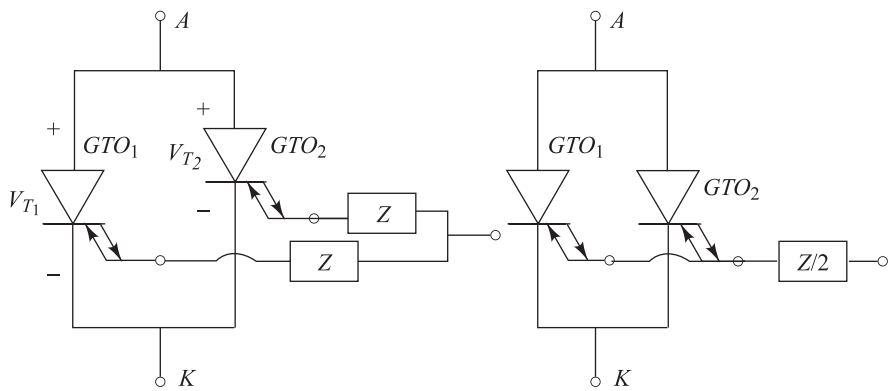
flat type GTO with the direct paralleled stud type GTO, costs of large capacity power can be reduced. In this section, steady state and transient operations for direct paralleling of GTO's has been discussed. Also, the current balancing ability of GTO's caused by the commutation of the gate current between parallel devices is described.

Current unbalance in the steady state and the transient state is generally attributed to the mismatch of the on-state voltage and the switching time. However, in case of GTO paralleling, exchange of the gate current between parallel devices also has much influence on current unbalance. In order to investigate this influence, the following two methods of gate connection are used:

(1) The external impedances are connected in series with each gate terminal, so that the gate current can be equally divided among the devices (gate-decoupling).

(2) The gate terminals are directly connected with each other, so that the gate current can be divided by the gate impedance of the device itself (gate-coupling).

Current unbalance is compared for the two methods of gate-connections in Fig. 5.37 to investigate gate interaction. External impedance is determined as shown in Fig. 5.37, so that a whole gate current can flow in the same way for both the methods.



(a) Gate decoupling (b) Gate coupling

Fig. 5.37 *Connections in direct paralleling of GTOs*

Typical switching waveforms of both devices is shown in Fig. 5.38. The current unbalance ΔI_p and ΔI_T during turn-on and steady on-state are given by

$$\Delta I_p = I_{P_1} - I_{P_2} \tag{5.63}$$

$$\Delta I_T = I_{T_1} - I_{T_2} \tag{5.64}$$

where I_P is the peak anode current during turn-on and I_T is the conducting current during the on-state.

Subscripts 1, 2 represent the number of the parallel branches, assuming the conducting current of branch 1 is larger than that of branch 2.

Current unbalance during turn-off is evaluated by the incremental current, ΔI_C in the transient state, and it is given by

$$\Delta I_C = I_{C_1} - I_{T_1} \qquad (5.65)$$

where I_{C_1} is the peak anode current during turn-off. The whole value of current unbalance during turn-off is the difference between the peak current I_{C_1} and the average on-state current. It is the sum of ΔI_C and $\Delta I_T/2$. The anode and gate currents can be measured using a current transformer. The impedance inserted in the circuit is 0.2 mΩ, which is sufficiently small enough not to produce a disturbance in the parallel operation.

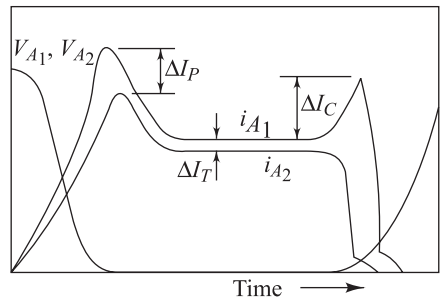


Fig. 5.38 *Switching waveforms of parallel devices*

1. *Steady on-state*

(A) On-state-operation: In the on-state, current unbalance results from the mismatch ΔV_T of the on-state voltage between parallel devices. Dependence of the on-state voltage on the gate current cannot be neglected in a GTO, unlike in a conventional thyristor. Current unbalance in the on-state is derived from not only the mismatch ΔV_T, but also the exchange of the gate current.

The on-state voltage changes linearly with small variations of the gate current and the anode current, and is given by

$$V_T = V_{TO} + R_{TT} \cdot \Delta I_T - R_{TG} \cdot \Delta I_G \qquad (5.66)$$

where V_{TO} = the initial value of the on-state voltage, $R_{TT} = \partial V_T / \partial I_T$, and $R_{TG} = -\partial V_T / \partial I_G$.

Similarly, the gate voltage changes linearly with small variations of both currents, and is given by

$$V_G = V_{GO} + R_{GT} \cdot \Delta I_T + R_{GG} \cdot \Delta I_G \qquad (5.67)$$

where V_{TO} = the initial value of the gate voltage

$R_{GT} = \partial V_G / \partial I_T$ and $R_{GG} = \partial G_V / \partial I_G$.

Figure 5.39 shows the dependence of on-state voltage V_T and gate voltage V_G on on-state current. For a device (stud type package) having a blocking voltage of 1200 V and controllable current of 200 A, it has been found that the value of R_{TT} and R_{GT} are 8 and 15 mΩ, respectively, and corresponds to the slopes of V–I current in Fig. 5.39.

The values of R_{TG} and R_{GG} correspond similarly to the slopes shown in Fig. 5.40, however, the slopes are different for the negative and positive side of the gate current. When the gate current is not supplied from the external circuit, the values of R_{TG} and T_{GG} are given by mean slope between both side, and are 13 and 23 mΩ, respectively.

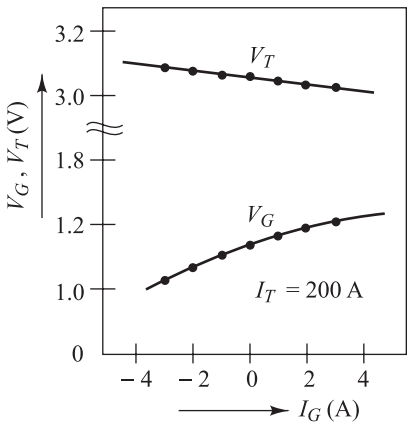


Fig. 5.39 *Dependence of on-state voltage V_T and gate voltage V_G on on-state current*

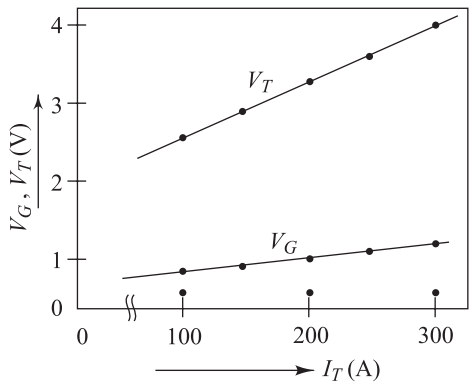


Fig. 5.40 *Dependence of on-state voltage V_T and gate voltage V_G on gate-current*

In gate decoupling, $\Delta I_G = 0$. For the on-state current, $\Delta I_T = -\Delta I_{T_2} = \Delta I_T/2$, and for the on-state voltage, $V_{T_1} = V_{T_2}$.

From Eq. (5.68), current unbalance

$$\Delta I_T = \Delta V_T / R_{TT} \tag{5.68}$$

where $\Delta V_T = V_{TO_2} - V_{TO_1}$.

In *gate coupling*, $\Delta I_{G_1} = -\Delta I_{G_2} = \Delta I_G/2$ and $V_{G_1} = V_{G_2}$. The condition with respect to V_T and I_T are the same as gate decoupling. Assuming that the mismatch ΔV_G is negligible small, $V_{G_{10}} = V_{G_{20}}$, current unbalance is given by

$$\Delta I_T = \frac{\Delta V_T}{R_{TT} + R_{GT} \cdot R_{TG} / R_{GG}} \tag{5.69}$$

(*B*) *Current unbalance*: Figure 5.39 shows the dependence of current unbalance on the mismatch of the on-state voltage. As shown, current unbalance in the gate coupling is smaller than in the gate decoupling. This is also shown in comparison between Eqs. (5.70) and (5.71).

The reduction of current unbalance is attributed to the improvement of the mismatch, ΔV_T, caused by exchange of the gate current. In gate coupling, there is nothing to prevent the exchange of the gate current, except the gate

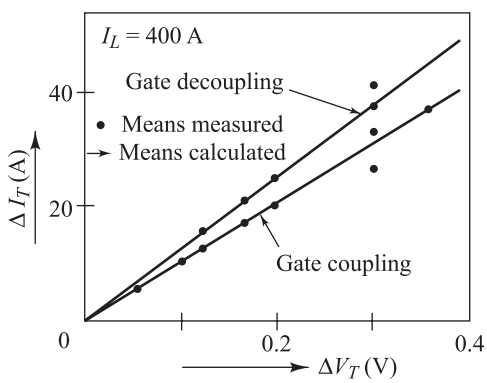


Fig. 5.41 *On-state current unbalance I_T due to the mismatch V_T of on-state voltage*

impedance of the GTO itself. Therefore, the exchange of the gate current is generated due to the difference of the gate voltage caused by the on-state current unbalance. As shown in Fig. 5.39, the gate voltage rises with the anode current, thus the device with larger anode current has a higher gate voltage, and plays the role of a gate current source. Consequently, the on-state voltage of the device increases with the negative gate current, as shown in Fig. 5.40, while the on-state voltage decreases in the device of small anode current. As a result, the net mismatch, ΔV_T, is reduced and current unbalance is improved.

The mismatch of the on-state voltage must be within 0.4 V, so that current unbalance can be limited to less than the desirable value of 40 A, which corresponds to 10% of the ratio between current unbalance of average current.

2. Turn-on

(A) Turn-on operation: The turn-on operation is measured using a resonant circuit. The load current is a half-sine waveform with a certain conducting period (say about 10 μs). First, the delay time of each device is measured under the values of the following parameters; gate-current (6 A), anode voltage (800 V), and peak anode current (250 A). Then, the combinations with various mismatch, ΔT_d of the delay time are selected and their turn-on parallel operations investigated. It has been found practically that, with the mismatch ΔT_d of 0.34 μs, in gate decoupling, current unbalance ΔI_P reaches the value of 155 A for the above parameter values, which is 30% in the ratio of incremental value to the average peak anode current. The gate current is equally divided due to the external resistor. It has also been observed that the gate voltage increases abruptly due to the gate current at first, and then increases gradually corresponding to a rate of rise of anode current. The former represents rise of the junction voltage, and the latter may be caused by inductance in the device package.

In the gate-coupling, with the same devices and circuit parameters, current unbalance is remarkably reduced in comparison to gate coupling. This improvement results from the induced voltage across the cathode wiring and the difference in gate impedance between both devices.

Cathode wiring, which connects both cathode terminals, is several centimeters in length and its inductance is very low. However, due to the large difference in the rate of rise of the conducting current, a noticeable voltage is induced across the cathode wiring.

The difference in gate current for the early stage results from the difference in gate impedance between parallel devices. A devices with a long delay time has low gate impedance, conversely, a device with a short delay time has high gate impedance.

Due to the induced voltage of the cathode wiring and the difference in gate impedance, a larger gate current flows to the device of longer delay time, while a smaller gate-current flows to the device of shorter-delay-time. As a result, the mismatch of the delay time is reduced, as well as current unbalance is improved.

(B) Current unbalance Figure 5.42 shows the dependence of current unbalance on the mismatch of the delay time. In gate-decoupling, current unbalance increases linearly with the mismatch ΔT_d. In gate coupling, current unbalance is small, and about one-tenth compared with gate decoupling. At the maximum mismatch ΔT_d of 0.34 μs, the ratio of the incremental value to the average peak current is about 3% in gate coupling. Current unbalance is sufficiently small enough not to require screening for the mismatch ΔT_d.

Figure 5.43 shows the dependence of current unbalance on the inductance L_K of cathode wiring. The difference of L_K between both devices generates a serious current unbalance. Therefore, each device must be connected with the load circuit by cathode wiring of the same-length.

In gate coupling, current balance is determined by the induced voltage of the cathode wiring and the difference in gate impedance. Therefore, it depends only slightly on the peak load current and the gate-current determined by the external circuit.

The method of gate coupling is useful in achieving the turn-on current balance in direct paralleling provided symmetrical cathode wiring is carried out.

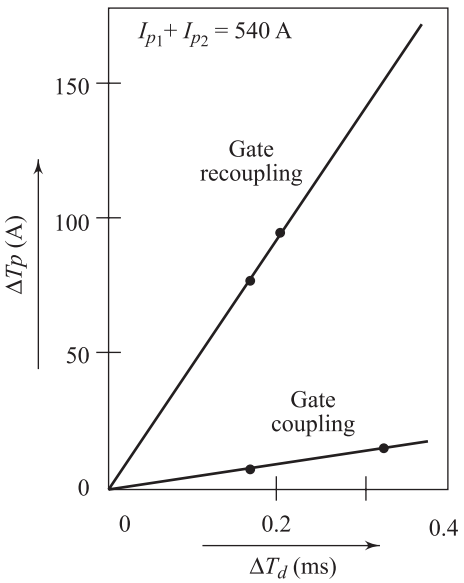


Fig. 5.42 *Relations between turn-on current unbalance ΔI_p and the delay time mismatch ΔT_d with peak load current ($I_{p1} + I_{p2}$) of 540 A*

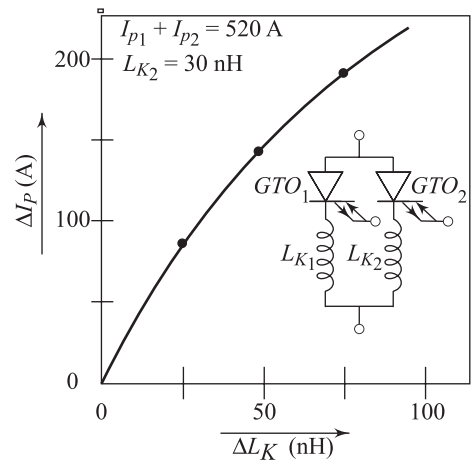


Fig. 5.43 *Dependence of turn-on current unbalance ΔI_P on the mismatch ΔL_K ($L_{K_2} - L_{K_1}$) of cathode wiring inductance*

3. Turn-off

(A) Turn-off operation: Turn-off operation is done in the clamped inductive load, using a polarized snubber, which protects the device from turn-off failure. In the parallel

operation, the mismatch of the storage time is an important parameter affecting current unbalance. The value of the storage time is slightly different between devices, and also changes with the anode current in the on-state. Therefore, the mismatch ΔT_s is given by the sum of the difference in storage time for the fixed anode current and the difference caused by current unbalance in the on-state.

The gate decoupling is carried out using the series gate inductance (of 1 μH) connected to each gate terminal. It has been observed experimentally that the gate-current is equally divided during the storage period.

When the device with the short storage time is turned off early, the anode current of the other device increases abruptly. In this case, serious current unbalance generates due to even a slight mismatch ΔT_s of less than 10% of the storage time. It is noted that, the current unbalance is remarkably reduced in comparison with gate decoupling. This results from the improvement of the mismatch ΔT_s caused by commutation of the GTO current.

The storage period of a GTO is a process during which the excess holes in the *P*-base are removed by the negative gate current, and lasts until the gate charge, or the time integrated value of the negative gate current reaches a prescribed value. Therefore, the storage time becomes short with an increase of the negative gate current, and longer with its decrease.

It has been found that, the gate current is equally divided in the early stage, however, there is a difference between both gate currents generated in the final stage of the storage period. In the device turning OFF early, the negative gate current decreases so that the storage period may be lengthened, while in the device turning-off later, the negative gate current increases so that the storage period may be shortened. As a result, the mismatch ΔT_s is improved and current unbalance is reduced.

(B) Current unbalance: Figure 5.44 shows the dependence of the incremental ΔI_c on the mismatch ΔT_s. In gate decoupling, the dependence roughly corresponds to the reverse waveforms of the anode current when the other device turns-off early. Basically, the mismatch ΔT_s must be sufficiently small enough compared with the fall time of the other device in order to reduce current unbalance.

In the gate coupling, the incremental value is remarkably small compared with gate decoupling, and is only slightly dependent on the mismatch ΔT_s. Figure 5.45 shows the dependence of turn-off incremental current ΔI_c on load current I_L. Similar to the previous figure, the value of ΔI_c in gate coupling is small compared with the gate decoupling. Also, it is hardly dependent on the controllable current, therefore, the ratio of current unbalance decreases with controllable current.

In gate coupling, current balance during turn-off is not affected by the device parameter mismatch; however, it depends significantly on the cathode wiring resistance. Figure 5.46. Shows the dependence of the incremental current ΔI_c on the mismatch of the cathode wiring resistance. The device of branch 1 has the lower on-state voltage, and the on-state current of branch 1 is 40 A more than that of branch 2, at a negligibly small resistance of the cathode wiring.

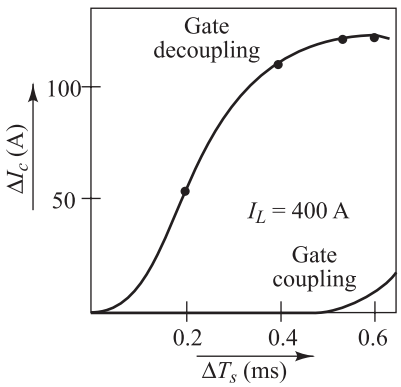


Fig. 5.44 *Turn-off incremental current ΔI_c due to the storage time mismatch ΔT_s*

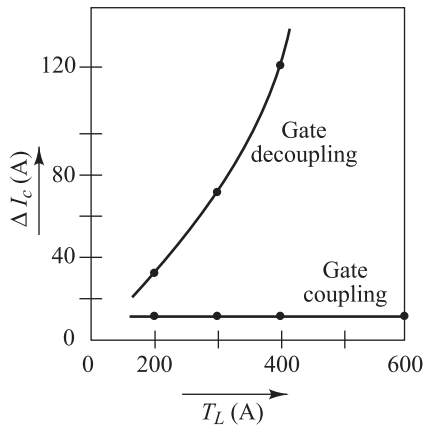


Fig. 5.45 *Dependence of turn off in incremental current ΔI_c on load current I_L*

When both cathode wiring resistances are equal, the incremental ΔI_c is nearly zero. The on-state current unbalance is reduced with an increase of the cathode wiring resistance of branch 1, however, the value of ΔI_c increases remarkably. The balance of the cathode wiring resistance is the most important point in direct paralleling of gate coupling.

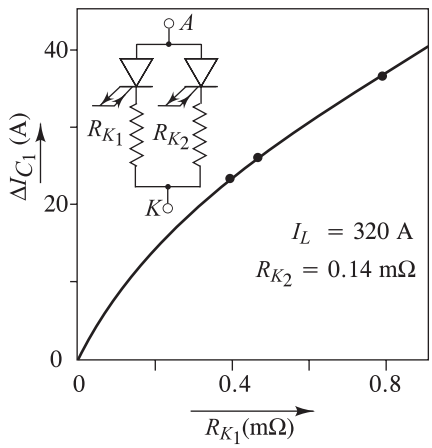


Fig. 5.46 *Dependence of turn-off incremental current ΔI_C on cathode wiring resistance*

(c) Mismatch of storage time: Figure 5.47 shows the dependence of the mismatch ΔT_s on the gate series inductance, where the end of the storage period is judged by the value of the impedance (V_A/i_A) of each device. Usually, this is defined at the time when the anode current decreases to 90% of the on-state current. However, the usual definition is not applicable for the device turning OFF later, in which the anode current increases over the on-state current during the storage period. The value of the impedance is selected so as to be consistent with the usual definition.

As shown in Fig. 5.47, the mismatch ΔT_s decreases with the gate series inductance L_{GS} connected with each gate terminal. When the value of L_{GS} is changed, the common inductance L_{GC} is also changed so that a rate of rise of the

whole negative gate current can be maintained at a fixed value. All mismatch ΔT_s values in the three different combinations are within less than 0.1 μs for the shortest gate wiring of 0.05 μH in Fig. 5.45.

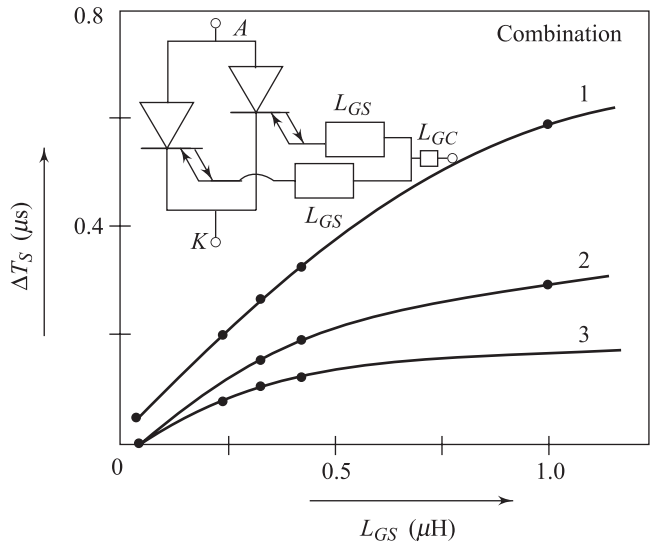


Fig. 5.47 *Dependence of the storage time mismatch ΔT_s on the gate series inductance L_G for three different combinations*

The mechanism improving the mismatch ΔT_s is as follows. Basically, it results from the time variation of the gate-impedance of the device itself. In the on-state, the gate impedance is low due to conductivity modulation of the *P*-base. The negative gate current squeezes the modulated area towards the centre of the *N*-emitter. The modulated area changes into the unmodulated area, therefore the gate impedance increases with the reduction of the modulated area. Then, the storage period ends with the disappearance of the modulated area.

In parallel operation, a device with a larger modulated area has a lower gate impedance, therefore, the modulated area is reduced faster due to the larger gate current corresponding to the gate impedance. In the other device with a smaller modulated area, it is reduced slowly. As a result, the modulated area of both devices would be squeezed in the same area, and would almost simultaneously disappear, i.e. the storage periods of both devices would end at the same time.

V FIELD-CONTROLLED THYRISTOR (FCT)

Field-controlled thyristors represent a new developed class of semiconductor devices which can be used for power switching applications. These devices have also been called field-controlled diode (FCD), and in Japan, a bipolar-static in duction thyristor (BSITH). Another term used to describe these devices is the bipolar Gridistor, because of the gridlike gate junction used in the device structure. Like conventional thyristors, these devices can block current flow for both polarities of applied anode voltage and can also conduct forward current at a high current density with a low forward voltage drop. FCDs have been shown to offer several unique features such as very high (dv/dt) capability, high radiation tolerance, and good high temperature characteristics.

1 Basic Structure and Characteristics

Figure 5.48 shows the basic field-controlled thyristor structure. The device consists of a *P-i-N* rectifier structure in which a gate junction has been introduced to control the current flow between the anode and the cathode regions. Power FCTs are made with a vertical current conduction path through the chip for the several reasons. Firstly, the internal structure of the power devices with vertical current flow paths can be designed so that electric field crowding can be minimized. The prevention of field crowding within the internal structure is extremely important for achieving nearly ideal breakdown characteristics within the limits set by the device termination. Secondly, in a vertical device design, one of the high current carrying terminals is placed at the top of the wafer and the other, at the bottom. The control electrode of these three terminal active power switching devices is also placed on the top surface for easy access during packaging. The placement of one of the large, high current carrying terminals at the bottom of the chip also results in significant reduction in chip area.

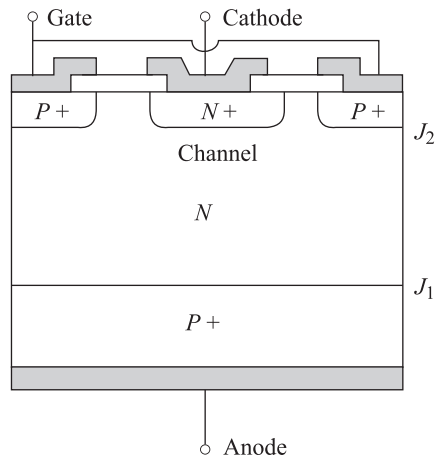
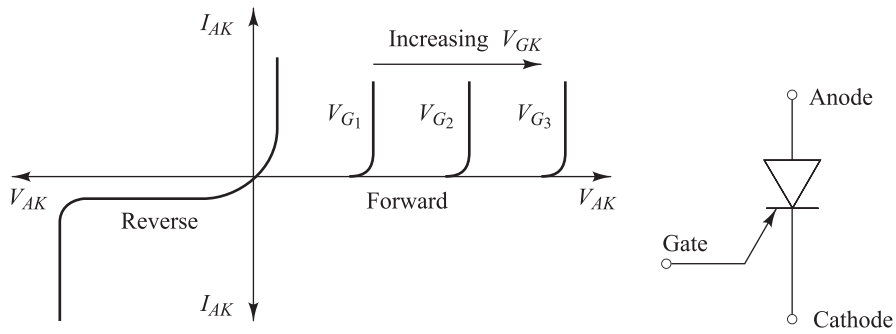


Fig. 5.48 *Field controlled-thyristor structure*

These devices are operated by grounding the cathode and applying bias voltages to the anode and gate regions with respect to the cathode. In the absence of a gate-bias, the device behaves essentially like a *P-i-N* rectifier between the anode and cathode terminals. The *I–V* characteristics of the FCT is shown in Fig. 5.49 (a).



(a) Output characteristics of FCT (b) Symbol

Fig. 5.49 *Device characteristics and circuit symbol*

With negative voltages applied to the anode, the device blocks current flow across the reverse-biased anode–base junction (J_1) producing the reverse blocking characteristics. With positive voltage applied to the anode, the *P-N* junction, J_1 becomes forward biased and the device conducts current at a high current density due to the modulation of the conductivity of the *N*-base by the carriers injected from the anode and the cathode regions. In order to control the power delivered to a load, it is also desirable to be able to block current flow for positive applied anode voltages. To obtain these forward blocking characteristics in this device, it is necessary to apply a negative bias on the gate. This reverse biases the gate junction (J_2) and causes its depletion layer to extend under the cathode. When the depletion layers of adjacent gate regions punch through under the cathode, a potential barrier is formed between the anode and the cathode. This potential barrier prevents the injection of electrons from the cathode to the anode and, thus, allows the device to block current flow. However, as the anode voltage increases, the potential barrier height decreases. This causes anode current flow to commence when the anode voltage is increased beyond a certain value for each applied gate-bias voltage. The ratio of this anode voltage to the applied gate bias is defined as the blocking gain of the device. Thus, FCTs have a normally-on characteristics and require the application of a gate voltage to maintain it in the off-state.

These devices can also be switched rapidly from the conducting mode to the forward-blocking mode (forced gate turn-off) by the application of a negative gate voltage while the anode current is flowing. During gate turn-off, sufficient gate current must be supplied by the gate drive circuit so as to remove the minority carrier stored charge in the *N*-base and to allow the gate depletion layer to extend under the cathode to pinch off the anode current flow. It has been found that turn-off times of less than one microsecond can be achieved when the peak gate-turn-off current is comparable to the anode current.

2 Gating Techniques

The FCT is fundamentally a normally-on device. It will conduct current in the absence of a gate bias voltage. To prevent forward conduction, it is necessary to supply a negative gate bias with respect to the cathode for *N*-channel devices. In this section, we will see the two different gating schemes.

1. Basic gating circuit Figure 5.50 shows the basic gating circuit for FCTs. In this circuit, the current supplied to the load by the power supply (E_L) can be controlled by gating the field controlled thyristor using switch S_1. When switch S_1 is open, the FCT is in its on-state and current is supplied to the load. When switch S_1 is closed, the gate voltage (V_G) is used to maintain the FCT in its forward blocking mode. To ensure forward blocking, it is necessary to satisfy the condition

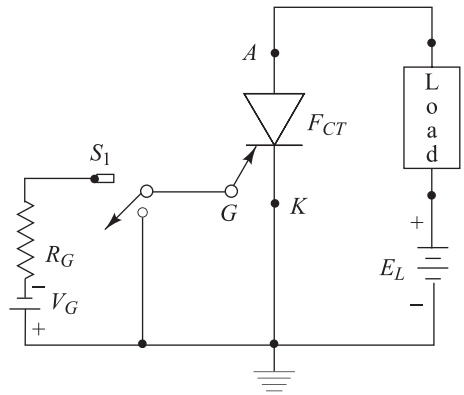


Fig. 5.50 *Basic gating circuit for FCT*

$$V_G > \frac{E_L}{G_B} \tag{5.72}$$

where G_B is the forward-blocking gain.

The turn-off speed of the FCT is controlled by the peak gate current during turn-off. This current can be controlled by the gate resistance (R_G). The gate series resistance, including that of the switch S_1, must be designed to provide adequate gate current for achieving the desired switching speed.

Several problems have been encountered with the use of this gating technique. Firstly, the devices are normally-on in the absence of a gate bias voltage and the circuit cannot ensure fail-safe start up and operation. Secondly, the devices require a substantial gate voltage (V_G) in order to operate them at large forward blocking voltages. This problem has been partially overcome by improvements in the device structure which have allowed the development of devices with high blocking gains. Thirdly, these devices require substantial gate-drive currents to switch them from the on-state to the blocking-state. Thus, although sub-microsecond turn-off times have been observed, gate turn-off current gains of less than 5 are typically necessary to achieve these high turn-off speeds. These drawbacks of the FCTs have been primarily responsible for its limited application to power switching applications.

2. Gating circuit using MOSFET The problems discussed above in the conventional gating technique for FCTs can be solved using the gating technique that utilizes a normally-on FCT and a separate normally-off three terminal device to create a composite device that exhibits normally-off characteristics. The most

desirable circuit for achieving normally-off operation is shown in Fig. 5.51. In this circuit, an *N*-channel, normally-off, MOS gated field effect transistor is used to control the current flow through the field controlled thyristor. To accomplish this, the drain (*D*) of the MOSFET is connected to the cathode (*K*) of the FCT and the source (*S*) of the MOSFET is connected to the gate (G_1) of the FCT. The current conduction through the load is then controlled by the applied bias (V_G) to the gate (G_2) of the MOSFET.

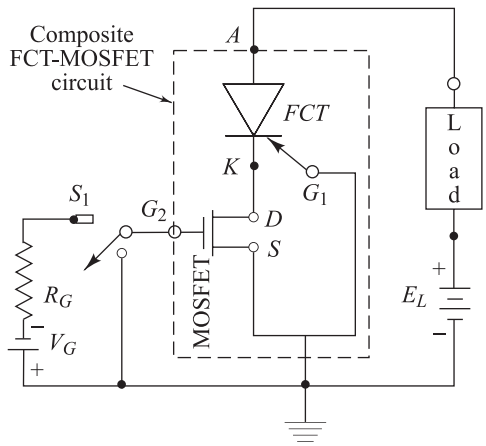


Fig. 5.51 *Gating circuit for FCT using MOSFET*

If the load voltage (E_L) is applied with the switch S_1 connecting the gate (G_2) of the MOSFET to the ground potential, the MOSFET remains in its off-state and does not allow current flow between its drain and source terminals unless the MOSFET breakdown voltage is exceeded. At the same time, the application of positive voltage (E_L) to the anode of the FCT reverse-biases its gate junction [junction J_2 in Fig. 5.49(a)]. The depletion layer of this junction then spreads under the cathode of the FCT and establishes a potential barrier between the anode and the cathode. This process shields the cathode potential from the anode potential. This can be clearly observed in Fig. 5.52 which shows a plot of the measured FCT gate-to-cathode potential (also the drain-to-source potential of the MOSFET) as a function of the applied anode voltage. It can be observed that the drain voltage of the MOSFET remains at less than 50 V for anode voltages of over 600 V. This feature is extremely important for the operation of the circuit because it allows the use of a low breakdown voltage MOSFET device for controlling the load current. Such low-voltage MOSFETs can be designed with very low on-resistance in order to maintain a small forward voltage drop in the device and to minimize the power dissipation. It has been found that the on-resistance per unit area for these unipolar devices will increase as a 2.5 power of the breakdown voltage.

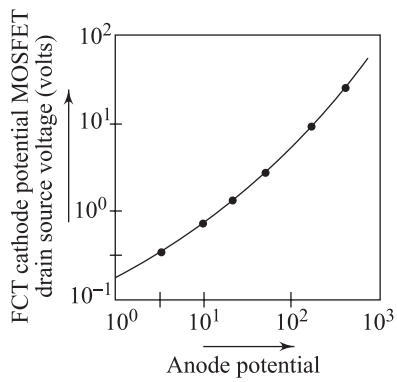


Fig. 5.52 *Variation of FCT cathode potential (also drain-to-source voltage of the MOSFET) with increasing anode voltage applied to the composite circuit*

Thus, the ability to use a low breakdown voltage MOSFET in the circuit due to the shielding of the cathode potential is extremely important for maintaining a low device forward drop and a low power dissipation. With the gate (G_2) connected to the ground potential, this gating circuit then maintains the FCT in a current blocking condition. This gating circuit, thus operates the FCT device in a normally-off mode without the need for a gate bias voltage and thus assures fail-state start up and operation.

In order to deliver current to the load, the switch S_1 is used to connect the gate (G_2) to the positive gate power supply (V_G). This positive gate bias (V_G) must exceed the threshold voltage of the MOSFET in order to switch it to the conducting state. When the MOSFET is in its conducting state, the load current can now flow through the FCT from the anode to the cathode and then via the drain of the MOSFET to the ground potential. Thus, in this circuit the full load current flows through the MOSFET. Since the forward voltage drop of the FCT is typically about 1.5 V, it is desirable to keep the forward voltage drop of the MOSFET below 0.5 V. This can be readily accomplished because the MOSFET used in this gating circuit can have a low breakdown voltage.

This gating circuit has the advantage of achieving forced gate turn-off of the anode current with a very high gate turn-off current gain. In order to turn-off the load current, the switch S_1 is used to connect the gate G_2 of the MOSFET to the ground potential. When this is done, the MOSFET switches from its conducting state to its blocking state. In order to accomplish this, a displacement current must flow to discharge the input gate capacitance of the MOSFET. Once the MOSFET turns-off, its drain potential rises. This produces a reverse-bias on the gate-juncjtion (J_2) of the FCT. The minority carriers stored in the N-base of the FCT are then removed via the gate until the FCT device supports the load voltage (E_L). The current flowing out of the gate (G_1) is equal to the anode current of the FCT until the gate junction (J_2) begins to support the anode voltage (E_L). Thus, the removal of the stored charge in the FCT occurs under conditions similar to unity current gain turn-off for the conventional circuit shown in Fig. 5.50. In this gating technique, the gate drive current required during turn-off is determined by the displacement current required for discharging the gate capacitance of the MOSFET. Since this gate current can be made small, this gate circuit offers very high gate turn-off current gains at very fast turn-off speeds.

ADDITIONAL REVIEW QUESTIONS

5.1 Draw and explain the simplified structure and collector characteristics of a power bipolar junction transistor in detail.
5.2 Explain the switching behaviour of a power transistor for a resistive load.
5.3 Discuss the switching behaviour of a power transistor for a inductive load.
5.4 Disscuss the various breakdown voltages of power BJT quoted by the manufacturer.
5.5 Explain in brief the second breakdown phenomenon in a power BJT.
5.6 What do you mean by safe operating area. Discuss the FBSOA and RBSOA for a power BJT.
5.7 Draw and explain the thermal equivalent circuit of a power BJT. Also, derive the expression for junction-temperature.
5.8 With the help of neat circuit diagrams, explain the various base drive controls in a power BJT.
5.9 Discuss the antisaturation control of BJTs in brief.
5.10 Draw and explain the power Darlington connection of two transistors. What are the disadvantages of this type of connection.
5.11 Discuss the power transistor voltage and current ratings briefly.
5.12 Briefly discuss the various power transistor snubber circuits.
5.13 Justify the following statements:
(i) It is necessary to connect an antiparallel diode across power BJT
(ii) The body of power BJT is connected to its collector terminal.
5.14 Draw the diagram of turn-off snubber used for the transistor protection and briefly explain the function of each component.
5.15 Discuss briefly the design issues of turn-off snubbers used for transistor.
5.16 Discuss the various gate drive circuits for a GTO.
5.17 Explain the operation of parallel connected GTOs.
5.18 What is the purpose of having parallel operation of GTOs? What care must be taken when paralleling the GTOs.

ADDITIONAL PROBLEMS ON BIOPLAR TRANSISTORS

5.5 For the transistor of worked Example 5.2, plot curves showing the instantaneous power during turn-on and turn-off. Hence, find the maximum instantaneous power level developed.

[*Ans* (i) Turn-on]

t (μs)	5	10	15	20	25	30	35	40
Power (W)	840	1440	1800	1920	1800	1440	840	0

(ii) Turn-off

t (μs)	5	10	15	20	25	30	35	40	45	50	55
Power (W)	586.7	1066.7	1400	1706	1866.7	1920	1866.7	1706	1440	1066.7	5 86.7

5.6 The β of the bipolar transistor in the following figure varies from 10 to 50. The load resistance is R_L = 11 Ω. The d.c. supply voltage is V_{CC} = 140 V and the

input voltage to the base circuit is V_{BB} = 10 V. If $V_{CE(sat)}$ = 1.8 V and $V_{BE(sat)}$ = 2 V, determine:

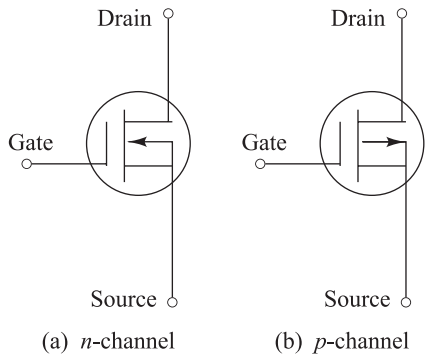


Fig. 5.6 *DE MOSFET schematic symbols*

(a) the value of R_B that will result in saturation with an overdrive factor of 6,
(b) the forced β, and
(c) the power loss in the transistor.[*Ans* (a) 1.06 Ω (b) 1.66 (c) 37.73 W]

5.7 For the power transistor, if the maximum junction temperature is T_J = 150°C, the ambient temperature is 35°C. If the thermal impedance are R_{QJC} = 0.7°C/W, R_{QCS} = 0.36°C/w, and R_{QCS} = 1.20°/W, calculate:

(a) the maximum power dissipation, and
(b) the case-temperature.

[*Ans* (a) 55.88 W. (b) 110.88°C]

5.8 The collector damping circuit of the following figure has V_{CC} = 120 V, R_C = 2.2 Ω, V_{D_1} = 2.1 V, V_{D_2} = 0.9 V, V_{BE} = 0.7 V, V_B = 14V, β = 14 and R_B = 3.3. Determine:

(a) the collector current without clamping,
(b) the collector–emitter clamping voltage V_{CE}, and
(c) the collector current with clamping

[*Ans* (a) 47.46 A (b) 1.9 V. (c) 53.27 A]

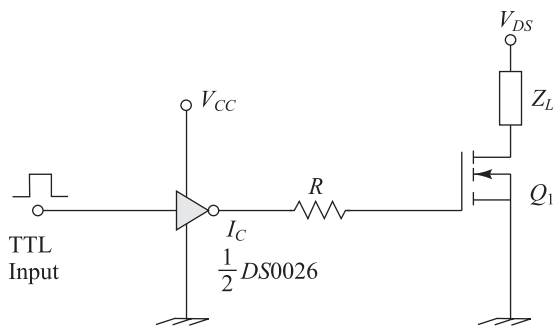


Fig. 5.8 *High current integrated buffer*

5.9 Two bipolar junction transistors are connected in parallel as shown in the following figure, and carry a total current of I_T = 20 A. The collector-emitter voltage of transistor T_1 is V_{CE_1} = 2.5 V and that of transistor T_2 is V_{CE_2} = 3 V. Compute the collector current of each transistor and difference in current sharing, if the current sharing series resistance are

(a) Re_1 = 0.3 Ω and Re_2 = 0.2 and

(b) $Re_1 = Re_2$ = 0.5 Ω.

[*Ans* (a) I_{C_1} = 9 A, I_{C_2} = 11 A, ΔI = 10% (b) I_{C_1} = 5.5 A, I_{C_2} = 9.5 A, ΔI = 5%.]

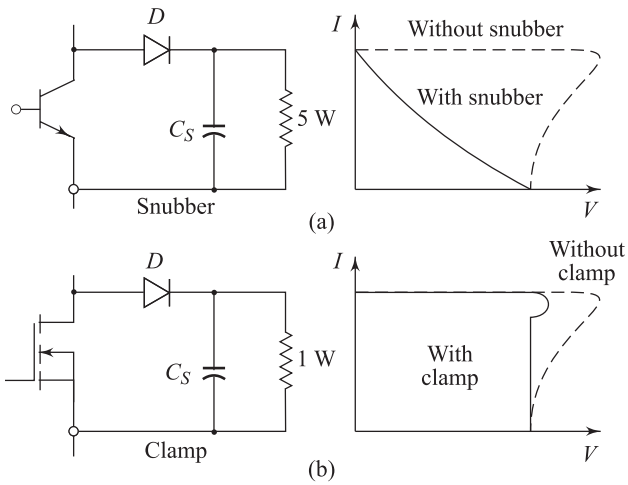


Fig. 5.9 *Comparison of snubber/clamp circuitry for* ***(a)*** *bipolar and* ***(b)*** *MOSFET*