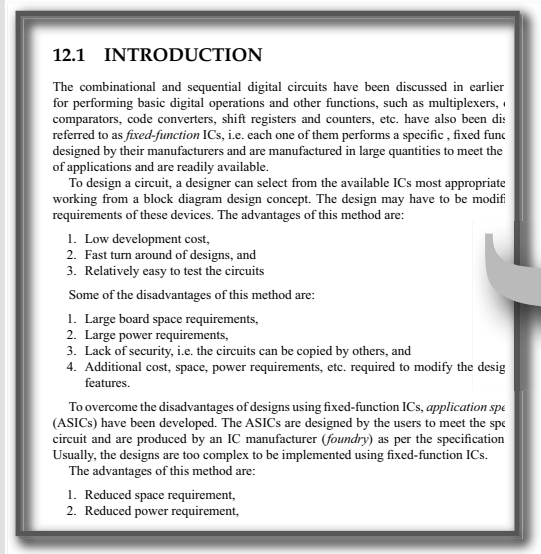
VISUAL WALKTHROUGH



12.1 INTRODUCTION

The combinational and sequential digital circuits have been discussed in earlier for performing basic digital operations and other functions, such as multiplexers, comparators, code converters, shift registers and counters, etc. have also been dis referred to as *fixed-function* ICs, i.e. each one of them performs a specific , fixed func designed by their manufacturers and are manufactured in large quantities to meet the of applications and are readily available.

To design a circuit, a designer can select from the available ICs most appropriate working from a block diagram design concept. The design may have to be modif requirements of these devices. The advantages of this method are:

1. Low development cost,
2. Fast turn around of designs, and
3. Relatively easy to test the circuits

Some of the disadvantages of this method are:

1. Large board space requirements,
2. Large power requirements,
3. Lack of security, i.e. the circuits can be copied by others, and
4. Additional cost, space, power requirements, etc. required to modify the desig features.

To overcome the disadvantages of designs using fixed-function ICs, *application spe* (ASICs) have been developed. The ASICs are designed by the users to meet the spe circuit and are produced by an IC manufacturer (*foundry*) as per the specification Usually, the designs are too complex to be implemented using fixed-function ICs.

The advantages of this method are:

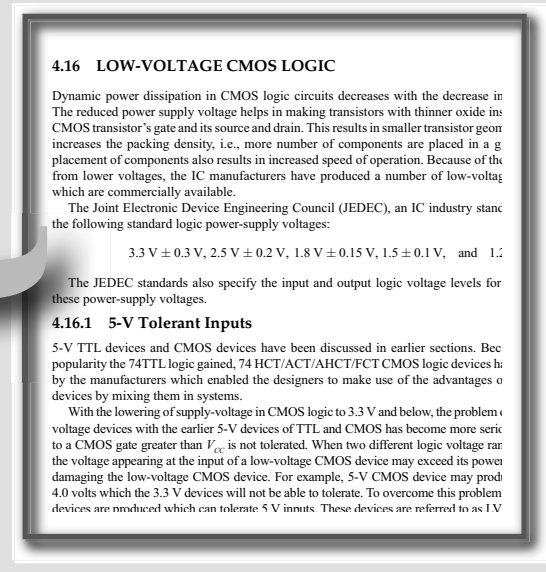
1. Reduced space requirement,
2. Reduced power requirement,

INTRODUCTION

Each chapter begins with an *Introduction* that introduces the topic giving its brief background, importance and contents of the chapter.

SECTIONS & SUB-SECTION

Each chapter has been divided into *Sections and Sub-sections* to present the chapter's subject matter in a logical progression of ideas and concepts.



4.16 LOW-VOLTAGE CMOS LOGIC

Dynamic power dissipation in CMOS logic circuits decreases with the decrease in The reduced power supply voltage helps in making transistors with thinner oxide ins CMOS transistor's gate and its source and drain. This results in smaller transistor geom increases the packing density, i.e., more number of components are placed in a g placement of components also results in increased speed of operation. Because of the from lower voltages, the IC manufacturers have produced a number of low-voltag which are commercially available.

The Joint Electronic Device Engineering Council (JEDEC), an IC industry stand the following standard logic power-supply voltages:

3.3 V ± 0.3 V, 2.5 V ± 0.2 V, 1.8 V ± 0.15 V, 1.5 ± 0.1 V, and 1.2

The JEDEC standards also specify the input and output logic voltage levels for these power-supply voltages.

4.16.1 5-V Tolerant Inputs

5-V TTL devices and CMOS devices have been discussed in earlier sections. Bec popularity the 74TTL logic gained, 74 HCT/ACT/AHCT/FCT CMOS logic devices ha by the manufacturers which enabled the designers to make use of the advantages o devices by mixing them in systems.

With the lowering of supply-voltage in CMOS logic to 3.3 V and below, the problem voltage devices with the earlier 5-V devices of TTL and CMOS has become more seric to a CMOS gate greater than V_{CC} is not tolerated. When two different logic voltage ran the voltage appearing at the input of a low-voltage CMOS device may exceed its power damaging the low-voltage CMOS device. For example, 5-V CMOS device may produ 4.0 volts which the 3.3 V devices will not be able to tolerate. To overcome this problem devices are produced which can tolerate 5 V inputs. These devices are referred to as I V

Read To Output Active Time (t_{RDX})

This is the minimum time delay between the beginning of the read pulse and the active state (from the high-impedance state).

Chip-Select To Output Valid Time (t_{CO})

This is the maximum time delay between the beginning of the chip-select pulse and at the data outputs.

Chip-Select To Output Active Time (t_{CX})

This is the minimum time delay between the beginning of the chip-select pulse and t to active state.

Output Tristate From Read (t_{OTD})

This is the maximum time delay between the end of the read pulse and the outpu impedance state.

Data Hold Time (t_{OHA})

This is the minimum time for which the valid data is available at the data outputs a The write- and read-cycle timings of a typical memory chip are given in Table 1

TECHNICAL TERMS

Important *Technical Terms* have been clearly defined for better understanding of the concepts involved.

ILLUSTRATIONS

A large number of *Illustrations*, totalling to 551, are provided at suitable locations to illustrate the concepts clearly for better understanding of the topic.

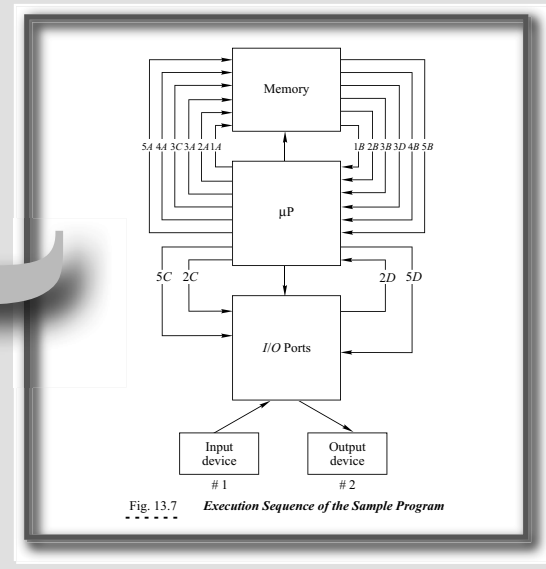


Fig. 13.7 ***Execution Sequence of the Sample Program***

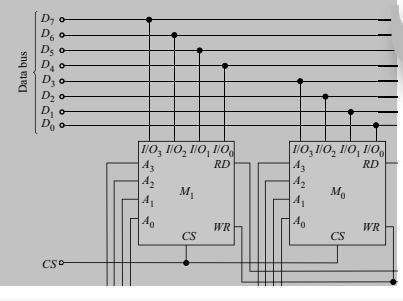
Example 11.3

Obtain a 16 × 8 memory using 16 × 4 memory ICs.

Solution

Since the word size required is $n = 8$ and the word size of the available IC is $N = 4$, the required to obtain the desired memory.

Since each chip can store 16 4-bit words and we want to store 16 8-bit words, each chip i each word. Figure 11.6 shows the relevant connections of the two chips. Here, we have ass output (I/O) lines which is common in available memory chips. In this 16×8 memory, the hig D_3, D_4) of each 8-bit word are located in memory M_1 and the lower order four bits (D_3, I memory M_0.



SOLVED EXAMPLES

***Solved Examples*, numbering 223, spread suitably through each chapter, are provided at appropriate locations, to aid in clear understanding of the text material.**

AVAILABLE ICs

Commercially *Available ICs* for each digital function is provided to help understand their functions and options available and allow a proper selection for design.

74S288 TTL PROM

The 74S288 is a 256 bit Schottky TTL PROM organised as 32 × 8 bits. Its l
Fig. 11.14. It is available in 16-pin DIP and has one enable ($\overline{G}$) input terminal whic
When the device is enabled ($\overline{G}$ LOW), the outputs ($O_0 - O_7$) represent the conten
the address input. When disabled ($\overline{G}$ HIGH), the outputs go to the OFF (high-im
available with LOWs in all locations. A HIGH may be programmed into any select
the titanium-tungsten fuse which requires 10.5 V for programming.

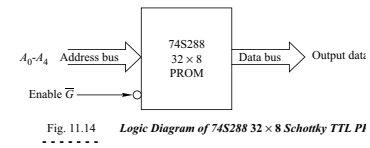


Fig. 11.14 ***Logic Diagram of 74S288 32 × 8 Schottky TTL PI***

27C010 OTP EPROM

Figure 11.15 shows the logic diagram of 27C010-1 Megabit OTP EPROM. It is CMOS read-only memory (OTP EPROM) organised as 128 K × 8 bits. It has Enable ($\overline{CE}$), Output Enable ($\overline{OE}$), and Program Store ($\overline{PGM}$).

GLOSSARY

Asynchronous sequential circuit A sequential circuit whose behaviour depen
which the input signals change. It is event driven and does not require clock pulses
Bit time Amount of time to transmit a single bit.
Bouncing Moving back and forth between two states before reaching a final stat
Bounce-elimination circuit A circuit that eliminates the effect of switch bouncin
Characteristic table A table describing operation of a FLIP-FLOP.
Chatterless switch A switch in which the bouncing effect has been eliminated.
Clear Setting the contents of a FLIP-FLOP or a circuit containing FLIP-FLOI
Clear input The input used for clearing a digital circuit.
Clock A train of pulses of usually constant frequency that synchronize the oper
sequential circuit including a microprocessor based system.
Clock cycle The interval between successive positive or negative transitions in a
Clocked FLIP-FLOP A FLIP-FLOP that responds to the data inputs only
appropriate clock signal.
Clock frequency The number of clock cycles per second.
Clocked sequential circuit The sequential circuits whose operation is synchroniz
clock pulses, between which no changes of state occur.
Counter A digital circuit that can count the number of pulses.
Data Information in digital (binary) form.
Debouncing switch Same as chatterless switch.
D-type FLIP-FLOP A FLIP-FLOP whose output follows the input when trigge
Edge-triggered FLIP-FLOP A FLIP-FLOP whose state changes on the ris
(negative) edge of a clock pulse.

GLOSSARY

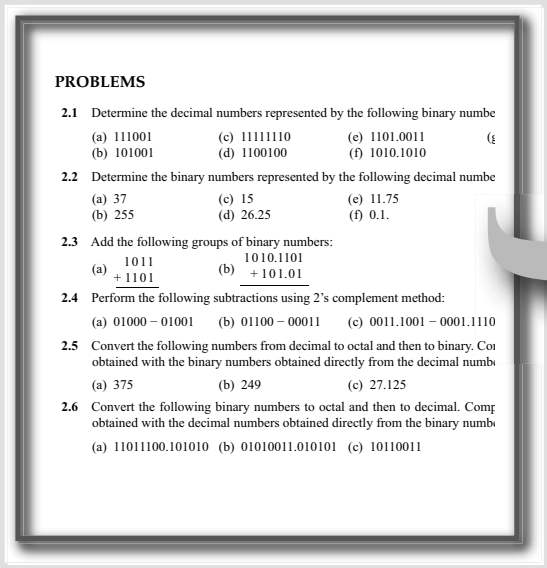
At the close of each chapter, *Glossary* of important terms, totalling to 542, is provided. It gives a list of key terms involved alongwith their definitions.

REVIEW QUESTIONS

Short answer *Review Questions* are provided at the end of each chapter in sufficient number, totalling to 293, for testing the understanding of the concepts introduced in the chapter. Their answers are available in Appendix-C.

REVIEW QUESTIONS

1.1 Ordinary electrical switch is _____ device. (analog/digital)
1.2 A train of pulses is _____ signal. (analog/digital)
1.3 The output of an AND gate is *high* if and only if all its inputs are _____
1.4 If one of the inputs to an OR gate is *high* its output will be _____
1.5 An AND gate output will always differ from an OR gate output for the same inpu
1.6 An OR gate is DISABLED by connecting one of its inputs to logic level ___
1.7 To ENABLE an OR gate, one of its inputs is connected to logic level _____
1.8 To INHIBIT (or DISABLE) an AND gate one of its inputs is connected to logi
(0/1)
1.9 To ENABLE an AND gate one of its inputs is connected to logic level _____
1.10 An AND gate is ENABLED by connecting one of its inputs to logic level ___
1.11 To DISABLE a NOR gate one of its inputs needs to be connected to logic leve
1.12 One of the inputs of an AND gate is labelled as ENABLE. This control inp
(active-low/active-high)
1.13 One of the inputs of a NOR gate is labelled as ENABLE. This control inp
(active-low/active-high)
1.14 The universal gates cannot be used as inverters. (True/False)
1.15 EXCLUSIVE-OR and EXCLUSIVE-NOR gates can be used as inverters. (Tr
1.16 An EX-OR gate can be used to compare digital signals. (True/False)
1.17 If one of the inputs of an EX-OR gate is *high*, its output will be _____
input/inverse of other input)
1.18 The number of rows in a truth table of 4 variables is _____ .
1.19 A 3-input NOR gate is required to detect the simultaneous occurrence of a
state. Its output is _____ . (active-low/active-high)
1.20 The number of 3-input NAND gates in a 14-pin IC is _____ .
1.21 The minimum member of bits required to distinguish 108 distinct objects is



PROBLEMS

2.1 Determine the decimal numbers represented by the following binary numbe

(a) 111001 (c) 11111110 (e) 1101.0011 (g
(b) 101001 (d) 1100100 (f) 1010.1010

2.2 Determine the binary numbers represented by the following decimal numbe

(a) 37 (c) 15 (e) 11.75
(b) 255 (d) 26.25 (f) 0.1.

2.3 Add the following groups of binary numbers:

(a) 1011 + 1101 (b) 1010.1101 + 101.01

2.4 Perform the following subtractions using 2's complement method:

(a) 01000 − 01001 (b) 01100 − 00011 (c) 0011.1001 − 0001.1110

2.5 Convert the following numbers from decimal to octal and then to binary. Co obtained with the binary numbers obtained directly from the decimal numb

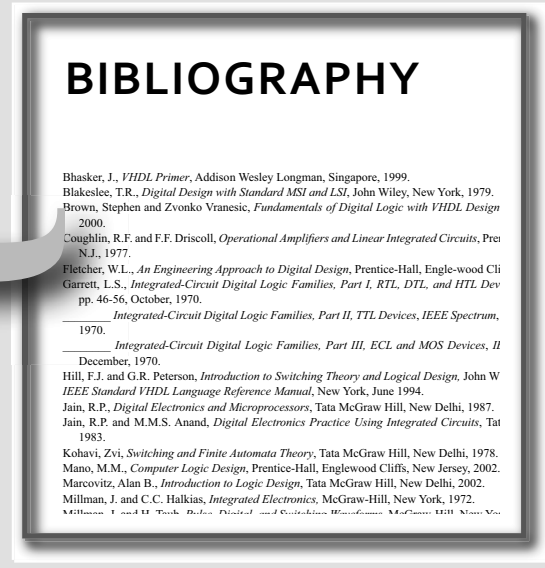
(a) 375 (b) 249 (c) 27.125

2.6 Convert the following binary numbers to octal and then to decimal. Comp obtained with the decimal numbers obtained directly from the binary numb

(a) 11011100.101010 (b) 01010011.010101 (c) 10110011

PRACTICE PROBLEMS

Each chapter contains a set of *Practice Problems*, totalling to 315, which require application of ideas and concepts discussed in the book. Answers for some of the selected Problems are provided in Appendix-D.



BIBLIOGRAPHY

Bhasker, J., *VHDL Primer*, Addison Wesley Longman, Singapore, 1999.
Blakeslee, T.R., *Digital Design with Standard MSI and LSI*, John Wiley, New York, 1979.
Brown, Stephen and Zvonko Vranesic, *Fundamentals of Digital Logic with VHDL Design* 2000.
Coughlin, R.F. and F.F. Driscoll, *Operational Amplifiers and Linear Integrated Circuits*, Pre N.J., 1977.
Fletcher, W.L., *An Engineering Approach to Digital Design*, Prentice-Hall, Engle-wood Cli
Garrett, L.S., *Integrated-Circuit Digital Logic Families, Part I, RTL, DTL, and HTL Dev* pp. 46-56, October, 1970.
_____ *Integrated-Circuit Digital Logic Families, Part II, TTL Devices*, *IEEE Spectrum*, 1970.
_____ *Integrated-Circuit Digital Logic Families, Part III, ECL and MOS Devices*, *I* December, 1970.
Hill, F.J. and G.R. Peterson, *Introduction to Switching Theory and Logical Design,* John W
IEEE Standard VHDL Language Reference Manual, New York, June 1994.
Jain, R.P., *Digital Electronics and Microprocessors*, Tata McGraw Hill, New Delhi, 1987.
Jain, R.P. and M.M.S. Anand, *Digital Electronics Practice Using Integrated Circuits*, Tat 1983.
Kohavi, Zvi, *Switching and Finite Automata Theory*, Tata McGraw Hill, New Delhi, 1978.
Mano, M.M., *Computer Logic Design*, Prentice-Hall, Englewood Cliffs, New Jersey, 2002.
Marcovitz, Alan B., *Introduction to Logic Design*, Tata McGraw Hill, New Delhi, 2002.
Millman, J. and C.C. Halkias, *Integrated Electronics,* McGraw-Hill, New York, 1972.

BIBLIOGRAPHY

***Bibliography*, provided at the end of the book, gives some useful references.**

Wakerly, John F., *Digital Design Principles and Practices*, Prentice-Hall, New Jersey, 200
Yarbrough, John M., *Digital Logic Applications and Design*, Vikas Publishing House, Nev

Websites

http://en.wikipedia.org
http://focus.ti.com
www.actel.com
www.alliancememory.com
www.altera.com
www.amd.com
www.atmel.com
www.cypress.com
www2.electronicproducts.com
www.epn-online.com
www.fairchild.com
www.futurlec.com
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ONLINE RESOURCES

***Online* webaddresses are provided for some of the prominent IC manufactures and distributors from where useful further information can be obtained about various products.**