CHAPTER 4

FIELD-EFFECT TRANSISTORS

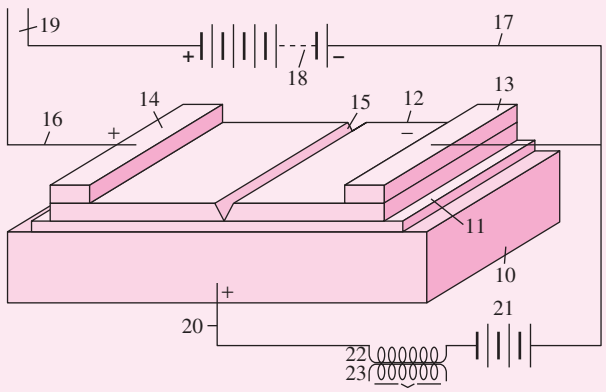
Chapter Outline

Chapter Goals

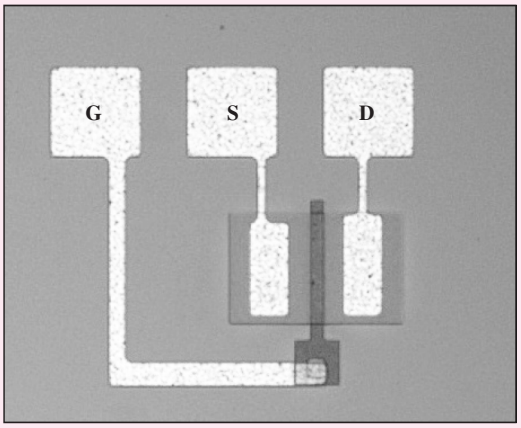
- Develop a qualitative understanding of the operation of two types of field-effect transistors — the MOSFET and the JFET
- Define and explore FET characteristics in the cutoff, triode, and saturation regions of operation
- Develop mathematical models for the current-voltage (i-v) characteristics of MOSFETs and JFETs
- Introduce the graphical representations for the output and transfer characteristic descriptions of electron devices
- Catalog and contrast the characteristics of enhancement-mode and depletion-mode FETs including NMOS and PMOS FETs and JFETs
- Learn the symbols used to represent FETs in circuit schematics
- Investigate circuits used to bias the transistors into various regions of operation
- Learn the basic structure and mask layout for MOS transistors and circuits
- Explore the concept of MOS device scaling
- Contrast three- and four-terminal device behavior
- Understand sources of capacitance in MOSFETs and JFETs
- Explore FET Modeling in SPICE

In this chapter we begin to explore the field effect transistor or FET. The FET has emerged as the dominant device in modern integrated circuits and is present in the vast majority of semiconductor circuits produced today. The ability to dramatically shrink the size of the FET device has made possible handheld computational power unimagined just 20 years ago.

As noted in Chapter 1, various versions of the field-effect device were conceived by Lilienfeld in 1928, Heil in 1935, and Shockley in 1952, well before the technology to produce such devices existed. The first successful metal-oxide-semiconductor field-effect transistors or MOSFETs were fabricated in the late 1950s, but it took nearly a decade to develop reliable commercial fabrication processes for MOS devices. Because of fabrication-related difficulties, MOSFETs with a p-type conducting region, PMOS devices, were the first to be commercially



Drawing from Lillienfeld Patent [1]



Top View of a Simple MOSFET

available in IC form, and the first microprocessors were built using PMOS processes. By the late 1960s, understanding and control of fabrication processes had improved to the point that devices with an *n*-type conducting region, NMOS transistors, could be reliably fabricated in large numbers, and NMOS rapidly supplanted PMOS technology because the improved mobility of the NMOS device translated directly into higher circuit performance. By the mid 1980s, power had become a severe problem, and the low-power characteristics of complementary MOS or CMOS devices caused a rapid shift to that technology even though it was a more complex and costly process. Today CMOS technology, which utilizes both NMOS and PMOS transistors, is the dominant technology in the electronics industry.

Chapter 4 explores the characteristics of **field-effect transistors (FETs).** The **metal-oxide-semiconductor field-effect transistor (MOSFET)** is without doubt the most commercially successful solid-state device. It is the primary component in high-density VLSI chips, including microprocessors and memories. A second type of FET, the **junction field-effect transistor (JFET),** is based on a *pn* junction structure and finds application particularly in analog and RF circuit design.

***P*-channel MOS (PMOS) transistors** were the first MOS devices to be successfully fabricated in large-scale integrated (LSI) circuits. Early microprocessor chips used PMOS technology. Greater performance was later obtained with the commercial introduction of ***n*-channel MOS (NMOS)** technology, using both enhancement-mode and ion-implanted depletion-mode devices.

This chapter discusses the qualitative and quantitative i-v behavior of MOSFETs and JFETs and investigates the differences between the various types of transistors. Techniques for biasing the transistors in various regions of operation are also presented.

Early integrated circuit chips contained only a few transistors, whereas today, the National Technology Roadmap for Semiconductors (NTRS [2]) projects the existence of chips with 1 billion transistors by the year 2010! This phenomenal increase in transistor density has been the force behind the explosive growth of the electronics industry outlined in Chapter 1 and has been driven by our ability to reduce (scale) the dimensions of the transistor without compromising its operating characteristics.

Although the bipolar junction transistor or BJT was successfully reduced to practice before the FET, the FET is conceptually easier to understand and is by far the most commercially important device. Thus, we consider it first. The BJT is discussed in detail in Chapter 5.

4.1 CHARACTERISTICS OF THE MOS CAPACITOR

An understanding of the qualitative behavior of the MOS capacitor provides a basis for understanding operation of the MOSFET. At the heart of the MOSFET is the **MOS capacitor** structure depicted in Fig. 4.1. The MOS capacitor is used to induce charge at the interface between the semiconductor and oxide. The top electrode of the MOS capacitor is formed of a low-resistivity material, typically aluminum or heavily doped polysilicon (polycrystalline silicon). We refer to this electrode as the **gate (*G*)** for reasons that become apparent shortly. A thin insulating layer, typically silicon dioxide, isolates the gate from the substrate or body — the semiconductor region that acts as the second electrode of the capacitor. Silicon dioxide is a stable, high-quality electrical insulator readily formed by thermal oxidation of the silicon substrate. The ability to form this stable high-quality insulator is one of the basic reasons that silicon is the dominant semiconductor material today. The semiconductor region may be *n*- or *p*-type, as depicted in Fig. 4.1.

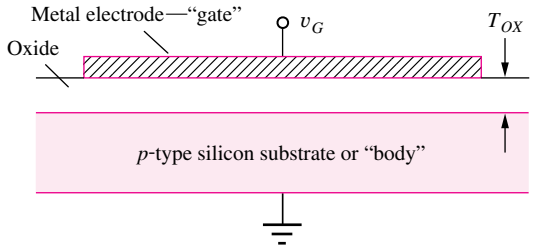


Figure 4.1 MOS capacitor structure on *p*-type silicon.

The semiconductor forming the bottom electrode of the capacitor has a substantial resistivity and a limited supply of holes and electrons. Because the semiconductor can therefore be depleted of carriers, as discussed in Chapter 2, the capacitance of this structure is a nonlinear function of voltage. Figure 4.2 shows the conditions in the region of the substrate immediately below the gate electrode for three different bias conditions: accumulation, depletion, and inversion.

4.1.1 Accumulation Region

The situation for a large negative bias on the gate with respect to the substrate is depicted in Fig. 4.2(a). The large negative charge on the metallic gate is balanced by positively charged holes attracted to the silicon-silicon dioxide interface directly below the gate. For the bias condition shown, the hole density at the surface exceeds that which is present in the original *p*-type substrate, and the surface is said to be operating in the **accumulation region** or just in **accumulation.** This majority carrier accumulation layer is extremely shallow, effectively existing as a charge sheet directly below the gate.

4.1.2 Depletion Region

Now consider the situation as the gate voltage is slowly increased. First, holes are repelled from the surface. Eventually, the hole density near the surface is reduced below the majority-carrier level set by the substrate doping level, as depicted in Fig. 4.2(b). This condition is called **depletion** and the region, the **depletion region.** The region beneath the metal electrode is depleted of free

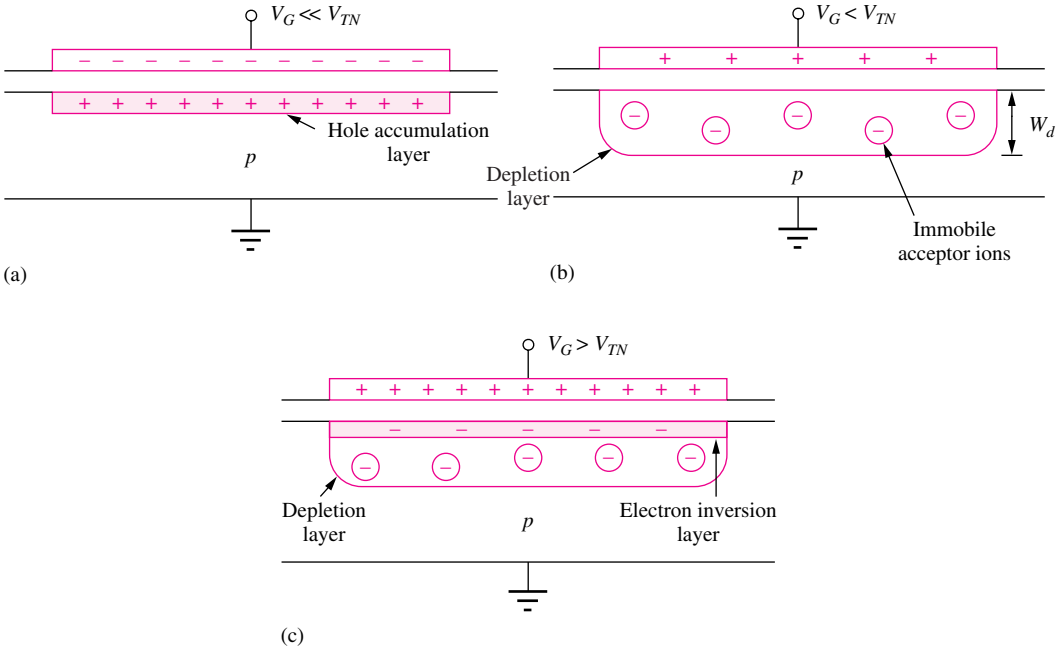


Figure 4.2 MOS capacitor operating in (a) accumulation, (b) depletion, and (c) inversion. Parameter V_{TN} in the figure is called the threshold voltage and represents the voltage required to just begin formation of the inversion layer.

carriers in much the same way as the depletion region that exists near the metallurgical junction of the *pn* junction diode. In Fig. 4.2(b), positive charge on the gate electrode is balanced by the negative charge of the ionized acceptor atoms in the depletion layer. The depletion-region width w_d can range from a fraction of a micron to tens of microns, depending on the applied voltage and substrate doping levels.

4.1.3 Inversion Region

As the voltage on the top electrode increases further, electrons are attracted to the surface. At a particular voltage level, which we will shortly define as the **threshold voltage,** the electron density at the surface exceeds the hole density. At this voltage, the surface has inverted from the *p*-type polarity of the original substrate to an *n*-type **inversion layer,** or **inversion region,** directly underneath the top plate as indicated in Fig. 4.2(c). This inversion region is an extremely shallow layer, existing as a charge sheet directly below the gate. In the MOS capacitor, the high density of electrons in the inversion layer is supplied by the electron–hole generation process within the depletion layer.

The positive charge on the gate is balanced by the combination of negative charge in the inversion layer plus negative ionic acceptor charge in the depletion layer. The voltage at which the surface inversion layer just forms plays an extremely important role in field-effect transistors and is called the **threshold voltage** V_{TN}.

Figure 4.3 depicts the variation of the capacitance of the NMOS structure with gate voltage. At voltages well below threshold, the surface is in accumulation, corresponding to Fig. 4.2(a), and the capacitance is high and determined by the **oxide thickness.** As the gate voltage increases, the surface depletion layer forms as in Fig. 4.2(b), the effective separation of the capacitor plates increases, and the capacitance decreases steadily. The total capacitance can be modeled as the series combination of the fixed oxide capacitance C''_{ox} and the voltage dependent depletion-layer

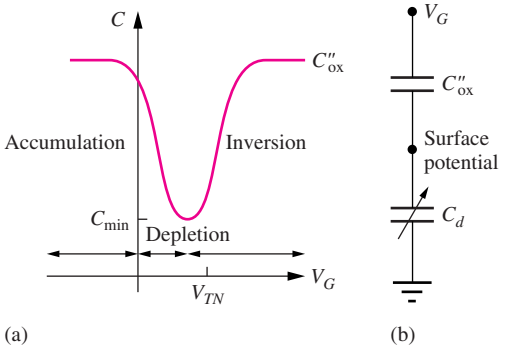


Figure 4.3 (a) Low frequency capacitance-voltage (C-V) characteristics for a MOS capacitor on a p-type substrate. (b) Series capacitance model for the C-V characteristic.

capacitance C_d, as in Fig. 4.3(b). The inversion layer forms at the surface as V_G exceeds the threshold voltage V_{TN}, as in Fig. 4.2(c), and the capacitance rapidly increases back to the value determined by the oxide layer thickness.

4.2 THE NMOS TRANSISTOR

A MOSFET is formed by adding two heavily doped n-type (n^+) diffusions to the cross section of Fig. 4.1, resulting in the structure in Fig. 4.4. The diffusions provide a supply of electrons that can readily move under the gate as well as terminals that can be used to apply a voltage and cause a current in the transistor.

Figure 4.4 shows a planar view, cross section, and circuit symbol of an ***n*-channel MOSFET,** usually called an **NMOS transistor,** or **NMOSFET.** The central region of the MOSFET is the MOS capacitor discussed in Sec. 4.1, and the top electrode of the capacitor is called the gate of the MOSFET. The two heavily doped n-type regions (n^+ regions), called the **source (*S*)** and **drain (*D*),** are formed in the p-type substrate aligned with the edge of the gate. The source and drain provide a supply of carriers so that the inversion layer can rapidly form in response to the gate voltage. The substrate of the NMOS transistor represents a fourth device terminal and is referred to synonymously as the **substrate terminal,** or the **body terminal (*B*).**

The terminal voltages and currents for the NMOS device are also defined in Fig. 4.4(b). The drain current i_D, source current i_S, gate current i_G, and body current i_B are all defined, with the positive direction of each current indicated for an NMOS transistor. The important terminal voltages are the gate-source voltage $v_{GS} = v_G - v_S$ the drain-source voltage $v_{DS} = v_D - v_S$, and the source-bulk voltage $v_{SB} = v_S - v_B$. These voltages are all positive during normal operation of the NMOSFET.

Note that the source and drain regions form pn junctions with the substrate. These two junctions are kept reverse-biased at all times to provide isolation between the junctions and the substrate as well as between adjacent MOS transistors. Thus, the bulk voltage must be less than or equal to the voltages applied to the source and drain terminals to ensure that these pn junctions are properly reverse-biased.

The semiconductor region between the source and drain regions directly below the gate is called the **channel region** of the FET, and two dimensions of critical import are defined in Fig. 4.4. ***L*** represents the **channel length,** which is measured in the direction of current in the channel. ***W*** is the **channel width,** which is measured perpendicular to the direction of current. In this and later chapters we will find that choosing the values for W and L are an important aspect of the digital and analog IC designer's task.

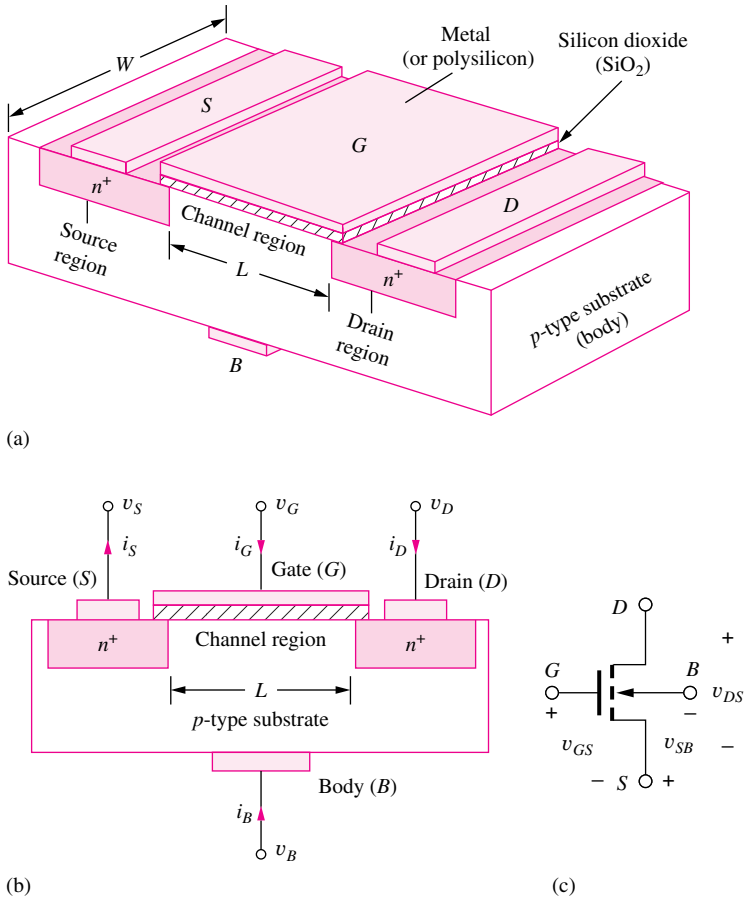


Figure 4.4 (a) NMOS transistor structure; (b) cross section; and (c) circuit symbol.

4.2.1 Qualitative *i-v* Behavior of the NMOS Transistor

Before attempting to derive an expression for the current-voltage characteristic of the NMOS transistor, let us try to develop a qualitative understanding of what we might expect by referring to Fig. 4.5. In the figure, the source, drain, and body of the NMOSFET are all grounded.

For a dc gate-source voltage, $v_{GS} = V_{GS}$, well below the threshold voltage V_{TN}, as in Fig. 4.5(a), back-to-back *pn* junctions exist between the source and drain, and only a small leakage current can flow between these two terminals. For V_{GS} near but still below threshold, a depletion region forms beneath the gate and merges with the depletion regions of the source and drain, as indicated in Fig. 4.5(b). The depletion region is devoid of free carriers, so a current still does not appear between the source and drain. Finally, however, when the gate-channel voltage exceeds the threshold voltage V_{TN}, as in Fig. 4.5(c), electrons flow in from the source and drain to form an inversion layer that connects the n^+ source region to the n^+ drain. A resistive connection, the channel, exists between the source and drain terminals.

If a positive voltage is now applied between the drain and source terminals, electrons in the channel inversion layer will drift in the electric field, creating a current in the terminals. Positive current in the NMOS transistor enters the drain terminal, travels down the channel, and exits the source terminal, as indicated by the polarities in Fig. 4.4(b). The gate terminal is insulated from the channel; thus, there is no dc gate current, and $i_G = 0$. The drain-bulk and source-bulk (and

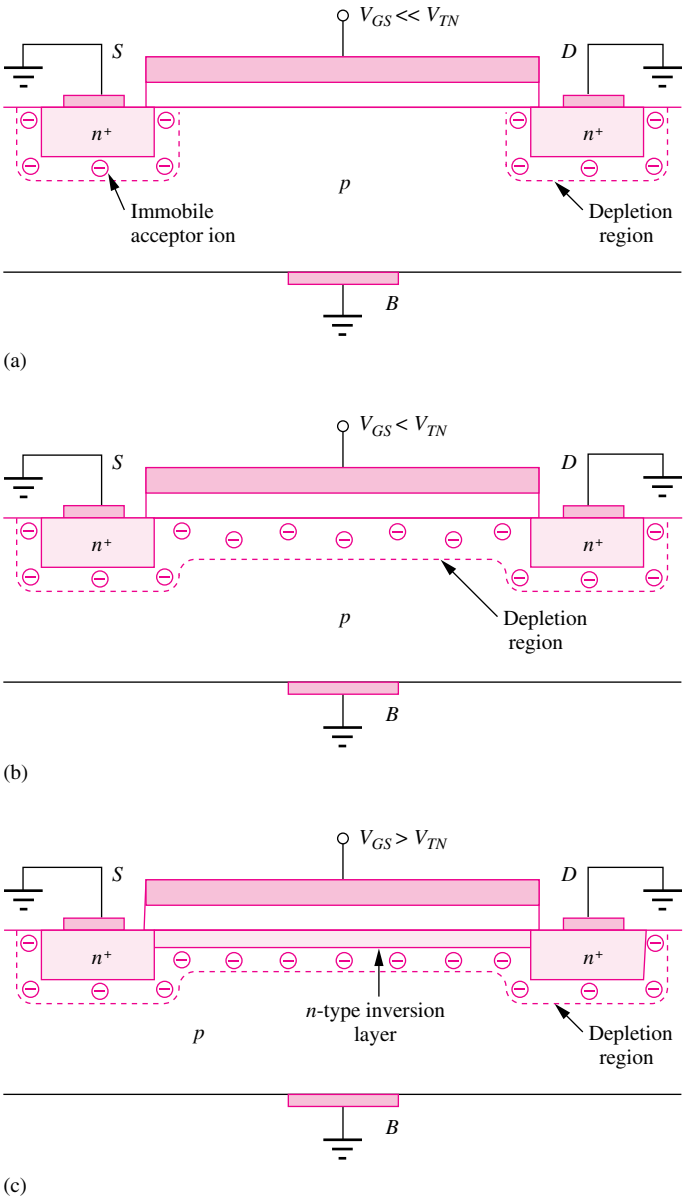


Figure 4.5 (a) $V_{GS} \ll V_{TN}$. (b) $V_{GS} < V_{TN}$. (c) $V_{GS} > V_{TN}$.

induced channel-to-bulk) pn junctions must be reverse-biased at all times to ensure that only a small reverse-bias leakage current exists in these diodes. This current is usually negligible with respect to the channel current i_D and is neglected. Thus we assume that $i_B = 0$.

In the device in Fig. 4.5, a channel must be induced by the applied gate voltage for conduction to occur. The gate voltage "enhances" the conductivity of the channel; this type of MOSFET is termed an **enhancement-mode device.** Later in this chapter we identify an additional type of MOSFET called a **depletion-mode device.** In Sec. 4.2.2, we develop a mathematical model for the current in the terminals of the NMOS device in terms of the applied voltages.

4.2.2 Triode[1] Region Characteristics of the NMOS Transistor

We saw in Sec. 4.2.1 that both i_G and i_B are zero. Therefore, the current entering the drain must be equal to the current leaving the source:

$$i_S = i_D \tag{4.1}$$

An expression for the drain current i_D can be developed by considering the transport of charge in the channel in Fig. 4.6, which is depicted for a small value of v_{DS}. The electron charge per unit length (a line charge — C/cm) at any point in the channel is given by

$$Q' = -WC''_{\text{ox}}(v_{\text{ox}} - V_{TN}) \qquad C/\text{cm for } v_{\text{ox}} \geq V_{TN} \tag{4.2}$$

where $C''_{\text{ox}} = \varepsilon_{\text{ox}}/T_{\text{ox}}$, the oxide capacitance per unit area (F/cm^2)

ε_{ox} = oxide permittivity (F/cm)

T_{ox} = oxide thickness (cm)

For silicon dioxide, $\varepsilon_{\text{ox}} = 3.9\varepsilon_{\text{o}}$, where $\varepsilon_{\text{o}} = 8.854 \times 10^{-14}$ F/cm.

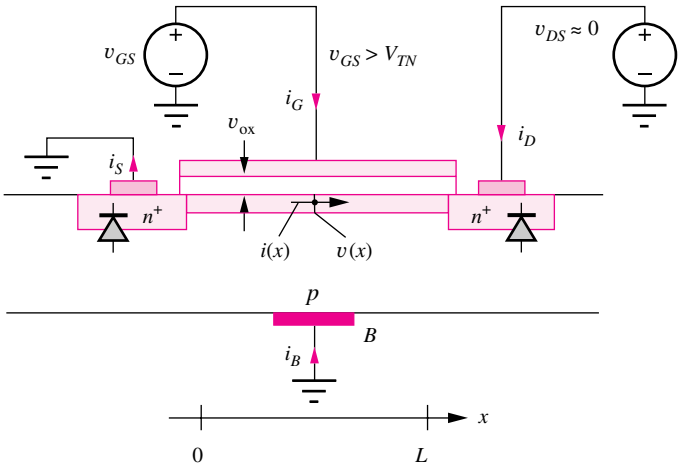


Figure 4.6 Model for determining i-v characteristics of the NMOS transistor.

The voltage v_{ox} represents the voltage across the oxide and will be a function of position in the channel:

$$v_{\text{ox}} = v_{GS} - v(x) \tag{4.3}$$

where $v(x)$ is the voltage at any point x in the channel referred to the source.

Note that v_{ox} must exceed V_{TN} for an inversion layer to exist, so Q' will be zero until $v_{\text{ox}} > V_{TN}$. At the source end of the channel, $v_{\text{ox}} = v_{GS}$, and it decreases to $v_{\text{ox}} = v_{GS} - v_{DS}$ at the drain end of the channel.

[1] This region of operation is also referred to as the "linear region." We will use triode region to avoid confusion with the concept of linear amplification introduced later in the text.

The electron drift current at any point in the channel is given by the product of the charge per unit length times the velocity v_x:

$$i(x) = Q'(x)v_x(x) \tag{4.4}$$

The charge Q' is represented by Eq. (4.2), and the velocity v_x of electrons in the channel is determined by the electron mobility and the transverse electric field in the channel:

$$i(x) = Q'v_x = [-WC''_{\text{ox}}(v_{\text{ox}} - V_{TN})](-\mu_n E_x) \tag{4.5}$$

The transverse field is equal to the negative of the spatial derivative of the voltage in the channel

$$E_x = -\frac{dv(x)}{dx} \tag{4.6}$$

Combining Eqs. (4.3) to (4.6) yields an expression for the current at any point in the channel:

$$i(x) = -\mu_n C''_{\text{ox}} W[v_{GS} - v(x) - V_{TN}]\frac{dv(x)}{dx}$$

or

$$i(x)\,dx = -\mu_n C''_{\text{ox}} W[v_{GS} - v(x) - V_{TN}]\,dv(x) \tag{4.7}$$

We know the voltages applied to the device terminals are $v(0) = 0$ and $v(L) = v_{DS}$, and we can integrate Eq. (4.7) between 0 and L:

$$\int_0^L i(x)\,dx = -\int_0^{v_{DS}} \mu_n C''_{\text{ox}} W[v_{GS} - v(x) - V_{TN}]\,dv(x) \tag{4.8}$$

Because there is no mechanism to lose current as it goes down the channel, the current must be equal to the same value i_D at every point x in the channel, $i(x) = i_D$ and Eq. (4.8) finally yields

$$i_D L = \mu_n C''_{\text{ox}} W\left(v_{GS} - V_{TN} - \frac{v_{DS}}{2}\right)v_{DS}$$

or

$$i_D = \mu_n C''_{\text{ox}} \frac{W}{L}\left(v_{GS} - V_{TN} - \frac{v_{DS}}{2}\right)v_{DS} \tag{4.9}$$

The value of $\mu_n C''_{\text{ox}}$ is fixed for a given technology and cannot be changed by the circuit designer. For circuit analysis and design purposes, Eq. (4.9) is therefore most often written as

$$i_D = K_n\left(v_{GS} - V_{TN} - \frac{v_{DS}}{2}\right)v_{DS} \tag{4.10}$$

where $K_n = K'_n W/L$ and $K'_n = \mu_n C''_{\text{ox}}$. Parameters K_n and $\boldsymbol{K'_n}$ are called **transconductance parameters** and both have units of A/V^2.

Equation (4.10) represents the classic expression for the drain-source current for the NMOS transistor in its **triode region** of operation, in which a resistive channel directly connects the source and drain. This resistive connection will exist as long as the voltage across the oxide

exceeds the threshold voltage at every point in the channel:

$$v_{GS} - v(x) \geq V_{TN} \qquad \text{for } 0 \leq x \leq L \tag{4.11}$$

The voltage in the channel is maximum at the drain end where $v(L) = v_{DS}$. Thus, Eqs. (4.9) and (4.10) are valid as long as

$$v_{GS} - v_{DS} \geq V_{TN} \qquad \text{or} \qquad v_{GS} - V_{TN} \geq v_{DS} \tag{4.12}$$

Recapitulating for the triode region,

$$i_D = K_n' \frac{W}{L}\left(v_{GS} - V_{TN} - \frac{v_{DS}}{2}\right)v_{DS} \tag{4.13}$$

for

$$v_{GS} - V_{TN} \geq v_{DS} \geq 0 \qquad \text{and} \qquad K_n' = \mu_n C_{\text{ox}}''$$

Some additional insight into the mathematical model can be gained by regrouping the terms in Eq. (4.9):

$$i_D = \left[C_{\text{ox}}'' W\left(v_{GS} - V_{TN} - \frac{v_{DS}}{2}\right)\right]\left(\mu_n \frac{v_{DS}}{L}\right) \tag{4.14}$$

For small drain-source voltages, the first term represents the average charge per unit length in the channel because the average channel voltage $v(x) = v_{DS}/2$. The second term represents the drift velocity in the channel, where the average electric field is equal to the total voltage v_{DS} across the channel divided by the channel length L.

We should note that the term *triode region* is used because the drain current of the FET depends on the drain voltage of the transistor, and this behavior is similar to that of the electronic vacuum triode that appeared many decades earlier (see Table 1.2 — Milestones in Electronics).

Note also that the quiescent operating point or Q-point of the FET is given by (I_D, v_{DS}).

EXERCISE: Calculate K_n' for a transistor with $\mu_n = 500$ cm^2/v · s and $T_{ox} = 25$ nm.

ANSWER: 69.1 μA/V^2

EXERCISE: An NMOS transistor has $K_n' = 50$ μA/V^2. What is the value of K_n if $W = 20$ μm, $L = 1$ μm? If $W = 60$ μm, $L = 3$ μm? If $W = 10$ μm, $L = 0.25$ μm?

ANSWERS: 1000 μA/V^2; 1000 μA/V^2; 2000 μA/V^2

EXERCISE: Calculate the drain current in an NMOS transistor for $V_{GS} = 0$, 1 V, 2 V, and 3 V, with $V_{DS} = 0.1$ V, if $W = 10$ μm, $L = 1$ μm, $V_{TN} = 1.5$ V, and $K_n' = 25$ μA/V^2. What is the value of K_n?

ANSWERS: 0; 0; 11.3 μA; 36.3 μA; 250 μA/V^2

4.2.3 On Resistance

The i-v characteristics in the triode region generated from Eq. (4.13) are drawn in Fig. 4.7 for the case of $V_{TN} = 1$ V and $K_n = 250\ \mu\text{A/V}^2$. The curves in Fig. 4.7 represent a portion of the common-source **output characteristics** for the NMOS device.

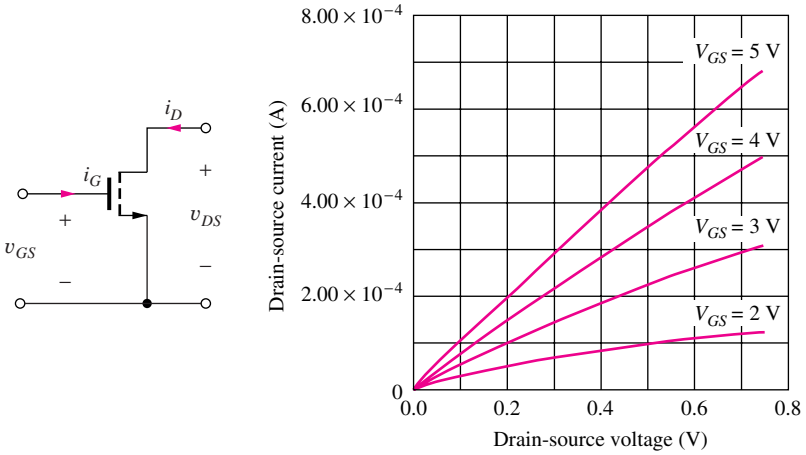


Figure 4.7 NMOS i-v characteristics in the triode region ($V_{SB} = 0$).

The output characteristics for the MOSFET are graphs of drain current i_D as a function of drain-source voltage v_{DS}. A family of curves is generated, with each curve corresponding to a different value of gate-source voltage v_{GS}. The output characteristics in Fig. 4.7 appear to be a family of nearly straight lines, hence the alternate name linear region (of operation). However, some curvature can be noted in the characteristics, particularly for $V_{GS} = 2$ V. Let us explore the triode region behavior in more detail using Eq. (4.9). For small drain-source voltages such that $v_{DS}/2 \ll v_{GS} - V_{TN}$, Eq. (4.9) can be reduced to

$$i_D \cong \mu_n C''_{\text{ox}} \frac{W}{L}(v_{GS} - V_{TN})v_{DS} \tag{4.15}$$

in which the current i_D through the MOSFET is directly proportional to the voltage v_{DS} across the MOSFET. The FET behaves much like a resistor connected between the drain and source terminals, but the resistor value can be controlled by the gate-source voltage. It has been said that this voltage-controlled resistance behavior originally gave rise to the name transistor, a contraction of "transfer-resistor."

The resistance of the FET in the triode region near the origin, called the **on-resistance R_{on}**, is defined in Eq. (4.16) and can be found by taking the derivative of Eq. (4.13):

$$R_{\text{on}} = \left[\frac{\partial i_D}{\partial v_{DS}}\bigg|_{v_{DS}\to 0}\right]^{-1}_{Q\text{-}pt} = \frac{1}{K'_n \dfrac{W}{L}(V_{GS} - V_{TN})} \tag{4.16}$$

Note that R_{on} is also equal to the ratio V_{DS}/I_D from Eq. (4.15).

Near the origin, the i-v curves are indeed straight lines. However, curvature develops as the assumption $v_{DS} \ll v_{GS} - V_{TN}$ starts to be violated. For the lowest curve in Fig. 4.7, $V_{GS} - V_{TN} = 2 - 1 = 1$ V, and we should expect linear behavior only for values of v_{DS} below 0.1 to 0.2 V. On the other hand, the curve for $V_{GS} = 5$ V exhibits quasi-linear behavior throughout most of the range of Fig. 4.7.

EXERCISE: Calculate the on-resistance of an NMOS transistor for $V_{GS} = 2$ V and $V_{GS} = 5$ V if $V_{TN} = 1$ V and $K_n = 250\ \mu A/V^2$.

ANSWERS: 4 kΩ; 1 kΩ

4.2.4 USE OF THE MOSFET AS A VOLTAGE-CONTROLLED RESISTOR

By operating the MOSFET in the triode region, we have a resistor with a value that can be controlled electronically. These resistors in turn may be used as the control element in more complicated electronic circuits. An important aspect of the utility of the MOSFET in this application comes from the fact that the control signal is well isolated from the resistor terminals.

A Voltage-Controlled Attenuator

As one example, the circuit in Fig. 4.8(a), shown conceptually in Fig. 4.8(b), represents a voltage-controlled attenuator in which the voltage transfer through the circuit can be varied electronically. The voltage "gain" is easily found by voltage division to be

$$\frac{v_O}{v_S} = \frac{R_{\text{on}}}{R_{\text{on}} + R} = \frac{1}{1 + \dfrac{R}{R_{\text{on}}}} = \frac{1}{1 + K_n R(V_{GG} - V_{TN})} \tag{4.17}$$

By adjusting the value of V_{GG}, we can change the fraction of the input signal that appears at the output. Suppose $K_n = 500\ \mu A/V^2$, $V_{TN} = 1$ V, $R = 2$ kΩ, and $V_{GG} = 1.5$ V. Then,

$$\frac{v_O}{v_S} = \frac{1}{1 + \left(500 \dfrac{\mu A}{V^2}\right)(2000\ \Omega)(1.5 - 1)\ V} = 0.667$$

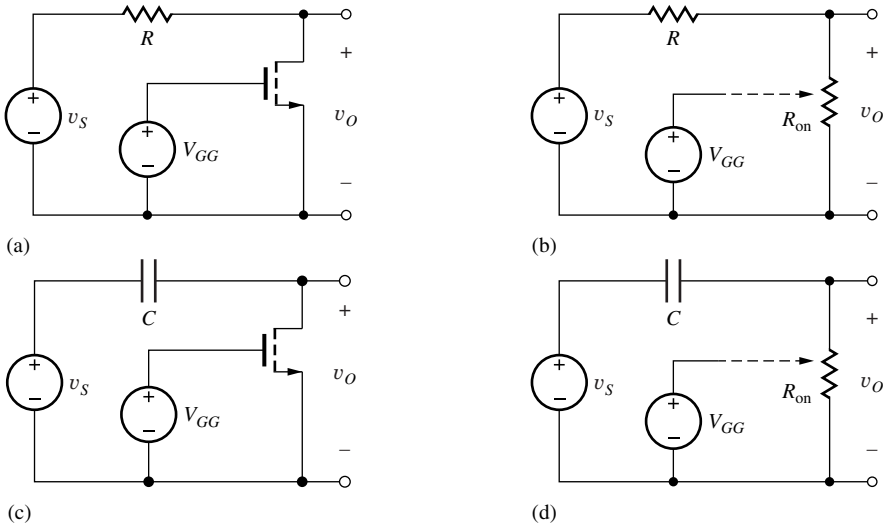


Figure 4.8 (a) Voltage-controlled attenuator circuit, (b) conceptual circuit for the attenuator explicitly indicating the voltage-controlled on-resistance, (c) voltage-controlled high-pass filter, and (d) conceptual circuit for voltage-controlled high-pass filter.

We have a minor semantics problem here. The gain through the network is less than one. This network has a gain of 0.667 or −3.52 dB, or we can say it attenuates the input signal by a factor of 1.5 or +3.52 dB.

In this application, as well as the next one, we desire the transistor to act as a resistor; therefore we must be careful not to violate the conditions required for triode region operation of the device, $v_{DS} \leq v_{GS} - V_{TN}$. In this case, the drain-source voltage equals the output voltage v_O, and the gate-source voltage is the dc bias voltage V_{GG}. Therefore proper operation requires $v_O \leq V_{GG} - V_{TN}$ to ensure that the FET remains in the triode region at all times. For the attenuator calculation here,

$$0.667 v_S \leq (1.5 - 1)\ \text{V} \qquad \text{or} \qquad v_S \leq 0.750\ \text{V}$$

EXERCISE: What is the attenuator voltage gain for $V_{GG} = 3$ V? What value of V_{GG} is required to achieve a 6-dB attenuation? A 20-dB attenuation? What are the maximum values of input voltage v_S that correspond to these three conditions?

ANSWERS: 0.333 (−9.54 dB); 2.00 V; 10.0 V; 6.00 V; 2.00 V; 90.0 V

A Voltage-Controlled High-Pass Filter

If we replace R with capacitor C, as in Fig. 4.8(c), we form a voltage controlled high-pass filter with a voltage transfer function given by

$$T(s) = \frac{\mathbf{V}_O(s)}{\mathbf{V}_S(s)} = \frac{s}{s + \omega_o} \qquad \text{where } \omega_o = \frac{1}{R_{\text{on}} C} = \frac{K_n (V_{GS} - V_{TN})}{C} \tag{4.18}$$

The **cutoff frequency** ω_o is set by the location of the pole of the RC network formed by capacitor C and the on-resistance of the FET. Here we see that the cutoff frequency is directly proportional to the gate-source voltage of the NMOS transistor. Let us calculate the cutoff frequency for $K_n = 500\ \mu\text{A/V}^2$, $V_{TN} = 1$ V, and $V_{GG} = 1.5$ V with $C = 0.02\ \mu$F:

$$f_o = \frac{500 \dfrac{\mu\text{A}}{\text{V}^2} (1.5 - 1)\ \text{V}}{2\pi (0.02\ \mu\text{F})} = 1.99\ \text{kHz}$$

At frequencies well above f_o, the magnitude of $T(s)$ approaches unity. Thus, at those frequencies the full amplitude of the input signal will appear at the output of the high-pass filter. Therefore, to satisfy triode region operation, $v_s \leq (V_{GG} - V_{TN}) = 0.5$ V

EXERCISE: What is the cutoff frequency for $V_{GG} = 5$ V? What value of V_{GG} is required to achieve a cutoff frequency of 5 kHz? What are the maximum values of input voltage v_S that correspond to these two conditions?

ANSWERS: 15.9 kHz; 2.26 V; 4.00 V; 1.26 V

4.2.5 SATURATION OF THE *i-v* CHARACTERISTICS

As discussed, Eq. (4.13) is valid as long as the resistive channel region directly connects the source to the drain. However, an unexpected phenomenon occurs in the MOSFET as the drain

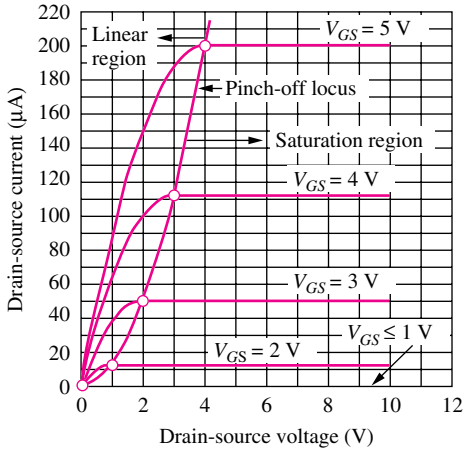


Figure 4.9 Output characteristics for an NMOS transistor with $V_{TN} = 1$ V and $K_n = 25 \times 10^{-6}$ A/V^2.

voltage increases above the triode region limit in Eq. (4.13). The current does not continue to increase, but instead saturates at a constant value. This unusual behavior is depicted in the i-v characteristics in Fig. 4.9 for several fixed gate-source voltages.

We can try to understand the origin of the current saturation by studying the device cross sections in Fig. 4.10. In Fig. 4.10(a), the MOSFET is operating in the triode region with $v_{DS} < v_{GS} - V_{TN}$, as discussed previously. In Fig. 4.10(b), the value of v_{DS} has increased to $v_{DS} = v_{GS} - V_{TN}$, for which the channel just disappears at the drain. Figure 4.10(c) shows the channel for an even larger value of v_{DS}. The channel region has disappeared, or *pinched off,* before reaching the drain end of the channel, and the resistive channel region is no longer in contact with the drain. At first glance, one may be inclined to expect that the current should become zero in the MOSFET. However, this is not the case. As depicted in Fig. 4.11, the voltage at the **pinch-off point** in the channel is always equal to

$$v_{GS} - v(x_{po}) = V_{TN} \qquad \text{or} \qquad v(x_{po}) = v_{GS} - V_{TN}$$

There is still a voltage equal to $v_{GS} - V_{TN}$ across the inverted portion of the channel, and electrons will be drifting down the channel from left to right. When the electrons reach the pinch-off point, they are injected into the depleted region between the end of the channel and the drain, and the electric field in the depletion region then sweeps these electrons on to the drain. Once the channel has reached pinch-off, the voltage drop across the inverted channel region is constant; hence, the drain current becomes constant and independent of drain-source voltage.

This region of operation of the MOSFET is often referred to as either the **saturation region** or the **pinch-off region** of operation. However, we will learn a different meaning for saturation when we discuss bipolar transistors in the next chapter. On the other hand, operation beyond pinchoff is the regime that we most often use for analog amplification, and in Part III we will use the term **active region** to refer to this region for both MOS and bipolar devices.

4.2.6 Mathematical Model in the Saturation (Pinch-Off) Region

Now let us find an expression for the MOSFET drain current in the pinched-off channel. The drain-source voltage just needed to pinch off the channel at the drain is $v_{DS} = v_{GS} - V_{TN}$, and substituting this value into Eq. (4.13) yields an expression for the NMOS current in the saturation

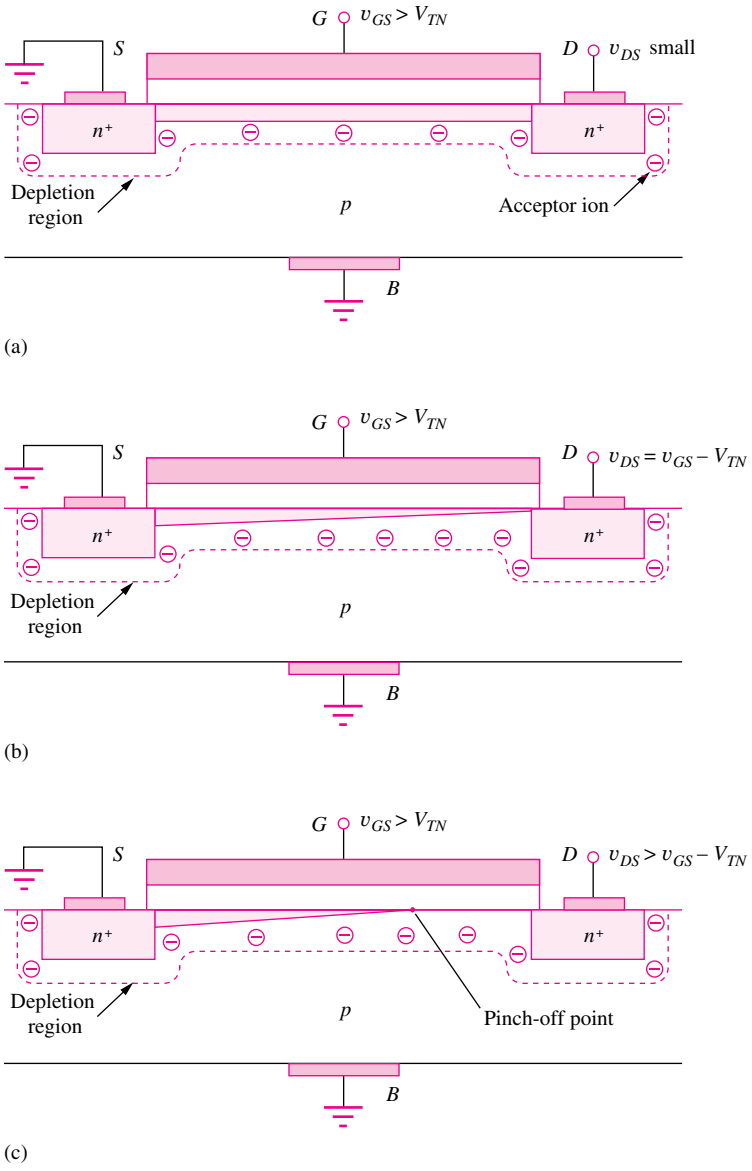


Figure 4.10 (a) MOSFET in the linear region. (b) MOSFET with channel just pinched off at the drain. (c) Channel pinch-off for $v_{DS} > v_{GS} - V_{TN}$.

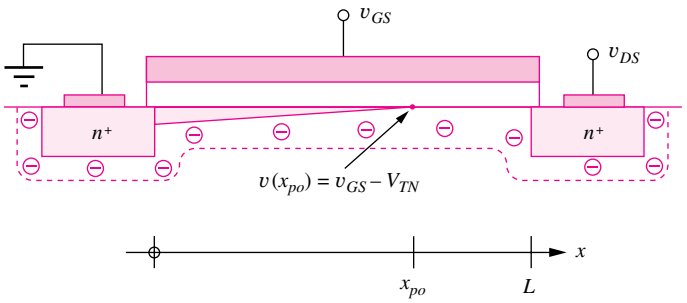


Figure 4.11 Inversion layer in the saturation region, also known as the pinch-off region.

region of operation:

$$i_D = \frac{K_n'}{2}\frac{W}{L}(v_{GS} - V_{TN})^2 \qquad \text{for } v_{DS} \geq (v_{GS} - V_{TN}) \geq 0 \tag{4.19}$$

This is the classic square-law expression for the drain-source current for the n-channel MOSFET operating in pinch-off. The current depends on the square of $v_{GS} - V_{TN}$ but is now independent of the drain-source voltage v_{DS}. Equation (4.19) is used frequently in the rest of this text. Commit it to memory!

The value of v_{DS} for which the transistor saturates is given the special name v_{DSAT} defined by

$$v_{\text{DSAT}} = v_{GS} - V_{TN} \tag{4.20}$$

and v_{DSAT} is referred to as the **saturation voltage,** or **pinch-off voltage,** of the MOSFET. Equation (4.19) can be interpreted in a manner similar to that of Eq. (4.14):

$$i_D = \left(C_{\text{ox}}'' W \frac{v_{GS} - V_{TN}}{2}\right)\left(\mu_n \frac{v_{GS} - V_{TN}}{L}\right) \tag{4.21}$$

The inverted channel region has a voltage of $v_{GS} - V_{TN}$ across it, as depicted in Fig. 4.11. Thus, the first term represents the magnitude of the average electron charge in the inversion layer, and the second term is the magnitude of the velocity of electrons in an electric field equal to $(v_{GS} - V_{TN})/L$.

An example of the overall output characteristics for an NMOS transistor with $V_{TN} = 1$ V and $K_n = 25\ \mu\text{A/V}^2$ appeared in Fig. 4.9, in which the locus of pinch-off points is determined by $v_{DS} = v_{\text{DSAT}}$. To the left of the **pinch-off locus,** the transistor is operating in the triode region, and it is operating in the saturation region for operating points to the right of the locus. For $v_{GS} \leq V_{TN} = 1$ V, the transistor is cut off, and the drain current is zero. As the gate voltage is increased in the saturation region, the curves spread out due to the square-law nature of Eq. (4.19).

Figure 4.12 gives an individual output characteristic for $V_{GS} = 3$ V, showing the behavior of the individual triode and saturation region equations. The triode region expression given in Eq. (4.13) is represented by the inverted parabola in Fig. 4.12. Note that it does not represent a valid model for the i-v behavior for $V_{DS} > V_{GS} - V_{TN} = 2$ V for this particular device. Note

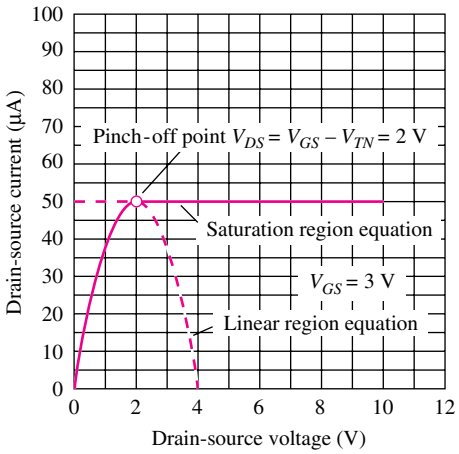


Figure 4.12 Output characteristic showing intersection of the linear region and saturation region equations at the pinch-off point.

also that the maximum drain voltage must never exceed the Zener breakdown voltage of the drain-substrate *pn* junction diode.

EXERCISE: Calculate the drain current for an NMOS transistor operating with $V_{GS} = 5$ V and $V_{DS} = 10$ V if $V_{TN} = 1$ V and $K_n = 1$ mA/V^2. What is the W/L ratio of this device if $K_n' = 40$ μA/V^2? What is W if $L = 0.35$ μm?

ANSWERS: 8.00 mA; 25/1; 8.75 μm

4.2.7 TRANSCONDUCTANCE

An important characteristic of transistors is the **transconductance** given the symbol g_m. The transconductance of the MOS devices relates the change in drain current to a change in gate-source voltage:

$$g_m = \left.\frac{di_D}{dv_{GS}}\right|_{Q\text{-}pt} \tag{4.22}$$

Taking the derivative of Eq. (4.19) and evaluating the result at the Q-point yields

$$g_m = K_n' \frac{W}{L}(V_{GS} - V_{TN}) = \frac{2I_D}{V_{GS} - V_{TN}} \tag{4.23}$$

We encounter g_m frequently in electronics, particularly during our study of analog circuit design.

EXERCISE: Find the drain current and transconductance for an NMOS transistor operating with $V_{GS} = 2.5$ V, $V_{TN} = 1$ V, and $K_n = 1$ mA/V^2.

ANSWERS: 1.13 mA; 1.5 mS

4.2.8 CHANNEL-LENGTH MODULATION

The output characteristics of the device in Fig. 4.11 indicate that the drain current is constant once the device enters the saturation region of operation. However, this is not quite true. Rather, the i-v curves have a small positive slope, as indicated in Fig. 4.13. The drain current increases slightly as the drain-source voltage increases. The increase in drain current visible in Fig. 4.13 is the result of a phenomenon called **channel-length modulation,** which can be understood by referring to Fig. 4.14, in which the channel region of the NMOS transistor is depicted for the case of $v_{DS} > v_{\text{DSAT}}$. The channel pinches off before it makes contact with the drain. Thus, the actual length of the resistive channel is given by $L = L_M - \Delta L$. As v_{DS} increases above v_{DSAT}, the length of the depleted channel region ΔL also increases, and the actual value of L decreases. Therefore, the value of L in the denominator of Eq. (4.19) actually has a slight inverse dependence on v_{DS}, leading to an increase in drain current increases as v_{DS} increases. The expression in Eq. (4.19) can be heuristically modified to include this drain-voltage dependence as

$$i_D = \frac{K_n'}{2}\frac{W}{L}(v_{GS} - V_{TN})^2(1 + \lambda v_{DS}) \tag{4.24}$$

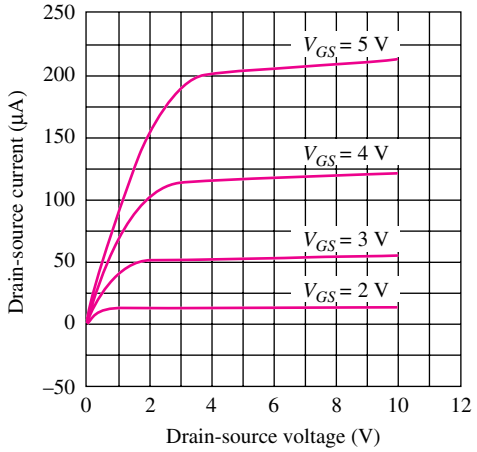


Figure 4.13 Output characteristics including the effects of channel-length modulation.

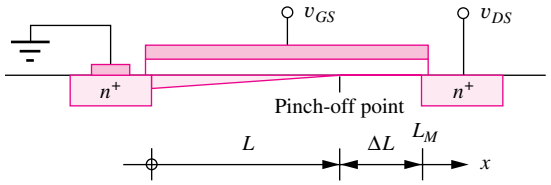


Figure 4.14 Channel-length modulation.

in which λ is called the **channel-length modulation parameter.** The value of λ is dependent on the channel length, and typical values are

$$0.001 \text{ V}^{-1} \leq \lambda \leq 0.10 \text{ V}^{-1}$$

In Fig. 4.13, λ is approximately 0.01 V^{-1}, which yields a 10 percent increase in drain current for a drain-source voltage change of 10 V.

EXERCISE: Calculate the drain current for an NMOS transistor operating with $V_{GS} = 5$ V and $V_{DS} = 10$ V if $V_{TN} = 1$ V, $K_n = 1$ mA/V^2, and $\lambda = 0.02$ V^{-1}. What is I_D for $\lambda = 0$?

ANSWERS: 9.60 mA; 8.00 mA

EXERCISE: Calculate the drain current for the NMOS transistor in Fig. 4.13 operating with $V_{GS} = 4$ V and $V_{DS} = 5$ V if $V_{TN} = 1$ V, $K_n = 25$ μA/V^2, and $\lambda = 0.01$ V^{-1}. Repeat for $V_{GS} = 5$ V and $V_{DS} = 10$ V.

ANSWERS: 118 μA; 220 μA

4.2.9 Transfer Characteristics and Depletion-Mode MOSFETs

The output characteristics in Figs. 4.7 and 4.13 represented our first look at graphical representations of the i-v characteristics of the transistor. The output characteristics plot drain current versus drain-source voltage for fixed values of the gate-source voltage. The second commonly used graphical format, called the **transfer characteristic,** plots drain current versus gate-source voltage for a fixed drain-source voltage. An example of this form of characteristic is given in Fig. 4.15 for two NMOS transistors in the pinch-off region. Up to now, we have been assuming that the threshold voltage of the NMOS transistor is positive, as in the right-hand curve in Fig. 4.15. This curve corresponds to an enhancement-mode device with $V_{TN} = +2$ V. Here we can clearly see the turn-on of the transistor as v_{GS} increases. The device is off (nonconducting) for $v_{GS} \leq V_{TN}$, and it starts to conduct as v_{GS} exceeds V_{TN}. The curvature reflects the square-law behavior of the transistor in the saturation region as described by Eq. (4.19).

However, it is also possible to fabricate NMOS transistors with values of $V_{TN} \leq 0$. These transistors are called **depletion-mode MOSFETs,** and the transfer characteristic for such a device with $V_{TN} = -2$ V is depicted in the left-hand curve in Fig. 4.15. Note that a nonzero drain current exists in the depletion-mode MOSFET for $v_{GS} = 0$; a negative value of v_{GS} is required to turn the device off.

The cross section of the structure of a depletion-mode NMOSFET is shown in Fig. 4.16. A process called *ion implantation* is used to form a built-in n-type channel in the device so that the

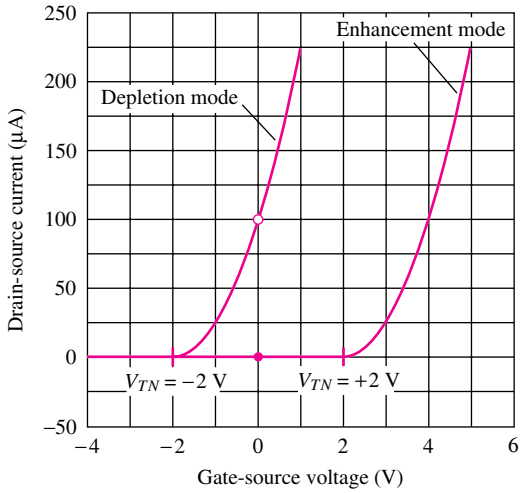


Figure 4.15 Transfer characteristics for enhancement-mode and depletion-mode NMOS transistors.

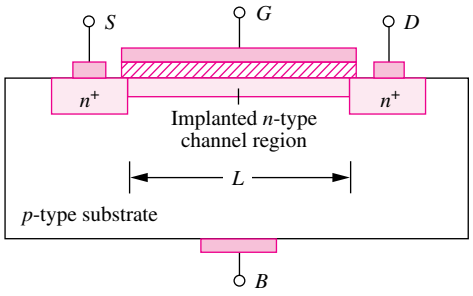


Figure 4.16 Cross section of a depletion-mode NMOS transistor.

source and drain are connected through the resistive channel region. A negative voltage must be applied to the gate to deplete the n-type channel region and eliminate the current path between the source and drain (hence the name depletion-mode device). In Chapter 6 we will see that the ion-implanted depletion-mode device played an important role in the evolution of MOS logic circuits. The addition of the depletion-mode MOSFET to NMOS technology provided substantial performance improvement, and it was a rapidly accepted change in technology in the mid 1970s.

EXERCISE: Calculate the drain current for the NMOS depletion-mode transistor in Fig. 4.15 for $V_{GS} = 0$ V if $K_n = 50\ \mu A/V^2$. Assume the transistor is in the pinch-off region. What value of V_{GS} is required to achieve the same current in the enhancement-mode transistor in the same figure?

ANSWERS: 100 μA; 4 V

EXERCISE: Calculate the drain current for the NMOS depletion-mode transistor in Fig. 4.15 for $V_{GS} = +1$ V if $K_n = 50\ \mu A/V^2$. Assume the transistor is in the pinch-off region.

ANSWER: 225 μA

4.2.10 Body Effect or Substrate Sensitivity

Thus far, it has been assumed that the source-bulk voltage v_{SB} is zero. With $v_{SB} = 0$, the MOSFET behaves as if it were a three-terminal device. However, we find many circuits, particularly in ICs, in which the bulk and source of the MOSFET must be connected to different voltages so that $v_{SB} \neq 0$. A nonzero value of v_{SB} affects the i-v characteristics of the MOSFET by changing the value of the threshold voltage. This effect is called **substrate sensitivity,** or **body effect,** and can be modeled by

$$V_{TN} = V_{TO} + \gamma\left(\sqrt{v_{SB} + 2\phi_F} - \sqrt{2\phi_F}\right) \tag{4.25}$$

where $V_{TO} =$ **zero-substrate-bias value for** V_{TN} (V)

$\gamma =$ **body-effect parameter** ($\sqrt{\text{V}}$)

$2\phi_F =$ **surface potential parameter** (V)

Parameter γ determines the intensity of the body effect, and its value is set by the relative sizes of the oxide and depletion-layer capacitances C''_{ox} and C_d in Fig. 4.3. The surface potential represents the approximate voltage across the depletion layer at the onset of inversion. For typical NMOS transistors,

$$-5\ \text{V} \leq V_{TO} \leq +5\ \text{V}$$

$$0 \leq \gamma \leq 3\sqrt{\text{V}}$$

$$0.3\ \text{V} \leq 2\phi_F \leq 1\ \text{V}$$

We use $2\phi_F = 0.6$ V throughout the rest of this text, and Eq. (4.25) will be represented as

$$V_{TN} = V_{TO} + \gamma\left(\sqrt{v_{SB} + 0.6} - \sqrt{0.6}\right) \tag{4.26}$$

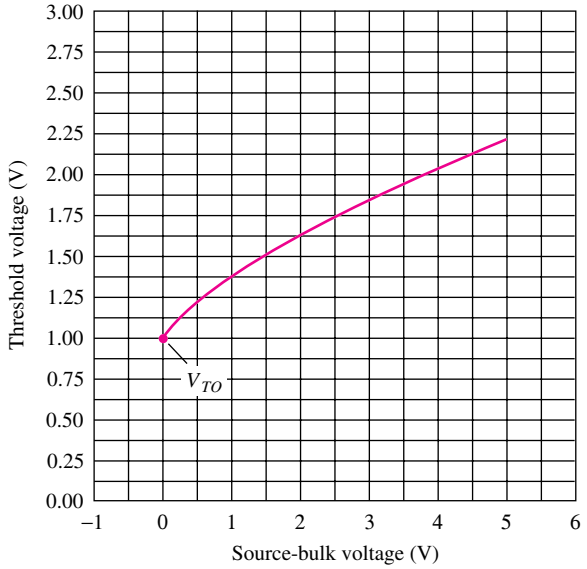
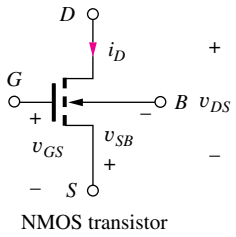


Figure 4.17 Threshold variation with source-bulk voltage for an NMOS transistor, with $V_{TO} = 1$ V, $2\phi_F = 0.6$ V and $\gamma = 0.75\sqrt{\text{V}}$.

Figure 4.17 plots an example of the threshold-voltage variation with source-bulk voltage for an NMOS transistor, with $V_{TO} = 1$ V and $\gamma = 0.75\sqrt{\text{V}}$. We see that $V_{TN} = V_{TO} = 1$ V for $v_{SB} = 0$ V, but the value of V_{TN} more than doubles for $v_{SB} = 5$ V. In Chapter 6, we will see that this behavior can have a significant impact on the design of MOS logic circuits.

NMOS TRANSISTOR MATHEMATICAL MODEL SUMMARY

Equations (4.27) through (4.31) represent the complete model for the i-v behavior of the NMOS transistor.



NMOS transistor

For all regions,

$$K_n = K_n' \frac{W}{L} \qquad K_n' = \mu_n C_{\text{ox}}'' \qquad i_G = 0 \qquad i_B = 0 \tag{4.27}$$

Cutoff region:

$$i_D = 0 \qquad \text{for } v_{GS} \leq V_{TN} \tag{4.28}$$

Triode region:

$$i_D = K_n \left(v_{GS} - V_{TN} - \frac{v_{DS}}{2} \right) v_{DS} \qquad \text{for } v_{GS} - V_{TN} \geq v_{DS} \geq 0 \tag{4.29}$$

Saturation region:

$$i_D = \frac{K_n}{2} (v_{GS} - V_{TN})^2 (1 + \lambda v_{DS}) \qquad \text{for } v_{DS} \geq (v_{GS} - V_{TN}) \geq 0 \tag{4.30}$$

Threshold voltage:

$$V_{TN} = V_{TO} + \gamma \left(\sqrt{v_{SB} + 2\phi_F} - \sqrt{2\phi_F} \right) \tag{4.31}$$

EXERCISE: Calculate the threshold voltage for the MOSFET of Fig. 4.17 for source-bulk voltages of 0 V, 1.5 V, and 3 V.

ANSWERS: 1.00 V; 1.51 V; 1.84 V

EXERCISE: What is the region of operation and drain current of an NMOS transistor having $V_{TN} = 1$ V, $K_n = 1$ mA/V^2, and $\lambda = 0.02$ V^{-1} for (a) $V_{GS} = 0$ V, $V_{DS} = 1$ V; (b) $V_{GS} = 2$ V, $V_{DS} = 0.5$ V; (c) $V_{GS} = 2$ V, $V_{DS} = 2$ V?

ANSWERS: (a) cutoff, 0 A; (b) triode, 375 μA; (c) saturation, 520 μA

4.3 PMOS TRANSISTORS

MOS transistors with p-type channels (PMOS transistors) can also easily be fabricated. In fact, as mentioned earlier, the first commercial MOS transistors and integrated circuits used PMOS devices because it was easier to control the fabrication process of the PMOS technology. The PMOS device is built by forming p-type source and drain regions in an n-type substrate, as depicted in the device cross section in Fig. 4.18.

The qualitative behavior of the transistor is essentially the same as that of an NMOS device except that the normal voltage and current polarities are reversed. The normal directions of current in the **PMOS transistor** are indicated in Fig. 4.18. A negative voltage on the gate relative to the source ($v_{GS} < 0$) is required to attract holes and create a p-type inversion layer in the channel region. To initiate conduction in the enhancement-mode PMOS transistor, the gate-source voltage must be more negative than the threshold voltage of the p-channel device, denoted by V_{TP}. To keep the source-substrate and drain-substrate junctions reverse-biased, v_{SB} and v_{DB} must also be less than zero. This requirement is satisfied by $v_{DS} \leq 0$.

An example of the output characteristics for an enhancement-mode PMOS transistor is given in Fig. 4.19. For $v_{GS} \geq V_{TP} = -1$ V, the transistor is off. For more negative values of v_{GS}, the drain current increases in magnitude. The PMOS device is in the triode region for small values of V_{DS}, and the saturation of the characteristics is apparent at larger V_{DS}. The curves look just like

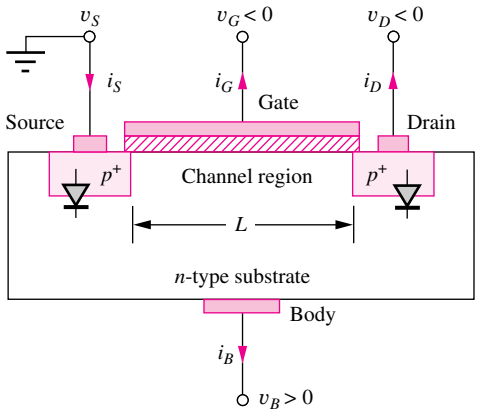


Figure 4.18 Cross section of an enhancement-mode PMOS transistor.

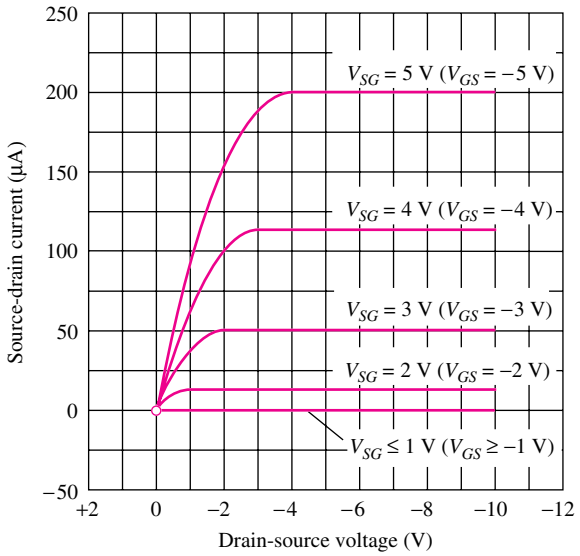


Figure 4.19 Output characteristics for a PMOS transistor with $V_{TP} = -1$ V.

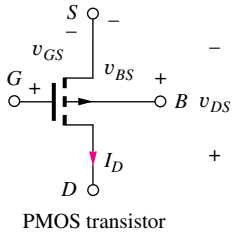
those for the NMOS device. This is a result of the choice of working with positive values for the voltages v_{SG} and v_{SD}, and of assigning the positive current direction to current exiting from the drain terminal of the PMOS transistor.

PMOS TRANSISTOR MATHEMATICAL MODEL SUMMARY

The mathematical model for the PMOS transistor is summarized below in Eqs. (4.30) through (4.34).

For all regions,

$$K_p = K_p' \frac{W}{L} \qquad K_p' = \mu_p C_{\text{ox}}'' \qquad i_G = 0 \qquad i_B = 0 \tag{4.32}$$



PMOS transistor

Cutoff region:

$$i_D = 0 \qquad \text{for } V_{GS} \geq V_{TP} \tag{4.33}$$

Triode region:

$$i_D = K_p\left(v_{GS} - V_{TP} - \frac{v_{DS}}{2}\right)v_{DS} \qquad \text{for } 0 \leq |v_{DS}| \leq |v_{GS} - V_{TP}| \tag{4.34}$$

Saturation region:

$$i_D = \frac{K_p}{2}(v_{GS} - V_{TP})^2(1 + \lambda|v_{DS}|) \qquad \text{for } |v_{DS}| \geq |v_{GS} - V_{TP}| \geq 0 \tag{4.35}$$

Threshold voltage:

$$V_{TP} = V_{TO} - \gamma\left(\sqrt{v_{BS} + 2\phi_F} - \sqrt{2\phi_F}\right) \tag{4.36}$$

For the enhancement-mode PMOS transistor, $V_{TP} < 0$. Depletion-mode PMOS devices can also be fabricated; $V_{TP} \geq 0$ for these devices.

Various authors have different ways of writing the equations that describe the PMOS transistor. Our choice attempts to avoid as many confusing minus signs as possible. The drain-current expressions for the PMOS transistor are written in similar form to those for the NMOS transistor except that the drain-current direction is reversed and the values of v_{GS} and v_{DS} are now negative quantities. Two signs must still be changed in the expressions, however. The parameter γ is normally specified as a positive value for both n- and p-channel devices, and a positive bulk-source potential will cause the PMOS threshold voltage to become more negative.

An important parametric difference appears in the expressions for K_p and K_n. In the PMOS device, the charge carriers in the channel are holes, so current is proportional to hole mobility μ_p. Hole mobility is typically only 40 percent of the electron mobility, so for a given set of voltage bias conditions, the PMOS device will conduct only 40 percent of the current of the NMOS device! Higher current capability leads to higher frequency operation in both digital and analog circuits. Thus, NMOS devices are preferred over PMOS devices in many applications.

EXERCISE: What is the region of operation and drain current of a PMOS transistor having $V_{TP} = -1$ V, $K_p = 0.4$ mA/V^2, and $\lambda = 0.02$ V^{-1} for (a) $V_{GS} = 0$ V, $V_{DS} = -1$ V; (b) $V_{GS} = -2$ V, $V_{DS} = -0.5$ V; (c) $V_{GS} = -2$ V, $V_{DS} = -2$ V?

ANSWERS: (a) cutoff, 0 A; (b) triode, 150 μA; (c) saturation, 208 μA

4.4 MOSFET CIRCUIT SYMBOLS

Standard circuit symbols for four different types of MOSFETs are given in Fig. 4.20: (a) NMOS enhancement-mode, (b) PMOS enhancement-mode, (c) NMOS depletion-mode, and (d) PMOS depletion-mode transistors. The four terminals of the MOSFET are identified as source (S), drain (D), gate (G), and bulk (B). The arrow on the **bulk terminal** indicates the polarity of the bulk-drain, bulk-source, and bulk-channel pn junction diodes; the arrow points inward for an NMOS device and outward for the PMOS transistor. Enhancement-mode devices are indicated by the dashed line in the channel region, whereas depletion-mode devices have a solid line, indicating the existence of the built-in channel. The gap between the gate and channel represents the insulating oxide region. Table 4.1 summarizes the threshold-voltage values for the four types of NMOS and PMOS transistors.

In many circuit applications, the MOSFET substrate terminal is connected to its source. The shorthand notation in Fig. 4.20(e) and 4.20(f) is often used to represent these three-terminal MOSFETs. The arrow identifies the source terminal and points in the direction of normal positive current.

To further add to the confusing array of symbols that the circuit designer must deal with, a number of additional symbols are used in other texts and reference books and in papers in technical journals. The wide diversity of symbols is unfortunate, but it is a fact of life that circuit designers

TABLE 4.1
Categories of MOS transistors

	NMOS DEVICE	PMOS DEVICE
Enhancement-mode	$V_{TN} > 0$	$V_{TP} < 0$
Depletion-mode	$V_{TN} \leq 0$	$V_{TP} \geq 0$

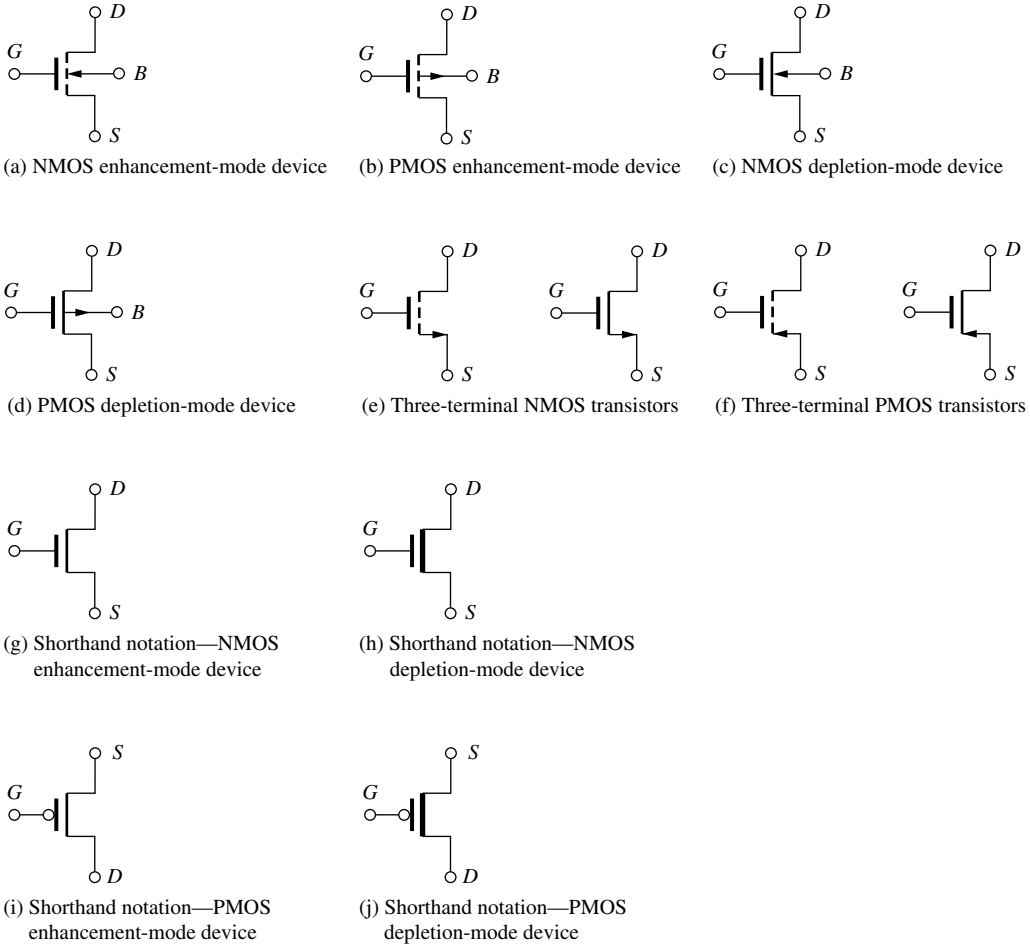


Figure 4.20 IEEE Standard MOS transistor circuit symbols.

must accept. For example, if one tires of drawing the dashed line for the enhancement-mode device as well as the substrate arrow, one arrives at the NMOS transistor symbol in Fig. 4.20(g); the channel line is then thickened to represent the NMOS depletion-mode device, as in Fig. 4.20(h). In a similar vein, the symbol in Fig. 4.20(i) represents the enhancement-mode PMOS transistor, and the corresponding depletion-mode PMOS device appears in Fig. 4.20(j). In the last two symbols, the circles represent a carry-over from logic design and are meant to indicate the logical inversion operation. We explore this more fully in Part II of this book. The symbols in Figs. 4.20(g) and (i) commonly appear in books discussing VLSI logic design.

The symmetry of MOS devices should be noted in the cross sections of Figs. 4.4 and 4.18. The terminal that is acting as the drain is actually determined by the applied potentials. Current can traverse the channel in either direction, depending on the applied voltage. For NMOS transistors, the n^+ region that is at the highest voltage will be the drain, and the one at the lowest voltage will be the source. For the PMOS transistor, the p^+ region at the lowest voltage will be the drain, and the one at the highest voltage will be the source. In later chapters, we shall see that this symmetry is highly useful in certain applications, particularly in MOS logic and dynamic random-access memory (DRAM) circuits.

DESIGN NOTE

MOS DEVICE SYMMETRY

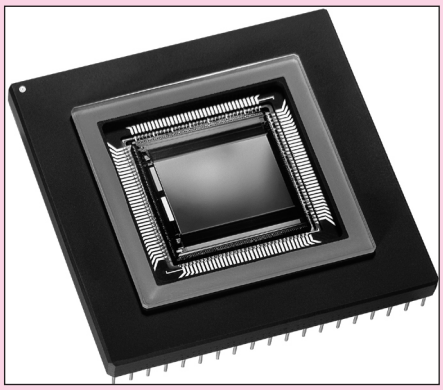
The MOS transistor terminal that is acting as the drain is actually determined by the applied potentials. Current can traverse the channel in either direction, depending on the applied voltage.

ELECTRONICS IN ACTION

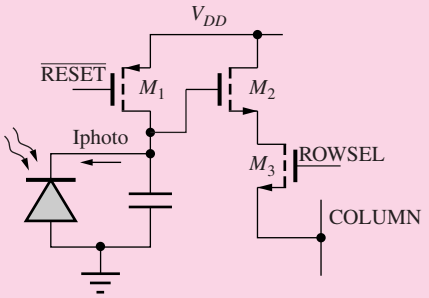
CMOS Camera on a Chip

Earlier in this text we examined the CCD image sensor widely used in astronomy. Although the CCD imager produces very high quality images, it requires an expensive specialized manufacturing process, complex control circuitry, and consumes a substantial amount of power. In the early 1990s, designers began developing techniques to integrate photo-detection circuitry onto inexpensive mainstream digital CMOS processes. In 1993, Dr. Eric Fossum's group at the Jet Propulsion Laboratory announced a CMOS digital camera on a chip. Since that time, many companies have designed camera chips that are based on mainstream CMOS processes, allowing the merging of many camera functions onto a single chip.

Pictured here is a photo of such a chip from Micron Technology.[1] The device produces full color images and has 1.3 million pixels in a 1280 × 1024 imaging array.



1.3 MegaPixel CMOS active-pixel image sensor.[1]



Typical photo diode pixel architecture.

A typical photodiode-based imaging pixel is also shown above. After asserting the $\overline{\text{RESET}}$ signal, the storage capacitor is fully charged to V_{DD} through transistor M_1. The reset signal is then removed, and light incident on the photodiode generates a photo current that discharges the capacitor. Different light intensities produce different voltages on the capacitor at the end of the light integration time. To read the stored value, the row select (ROWSEL) signal is asserted, and the capacitor voltage is driven onto the COLUMN bus via transistors M_2 and M_3.

[1] The chip pictured above is a Micron Technology MI-MV13 image sensor and is reprinted here with permission from Micron Technology, Inc.

In many designs random variations in the device characteristics will cause variations in the signal produced by each pixel for the same intensity of incident light. To correct for many of these variations, a technique known as *correlated double sampling* is used. After the signal level is read from a pixel, the pixel is reset and then read again to acquire a baseline signal. The baseline signal is subtracted from the desired signal, thereby removing the non-uniformities and noise sources which are common to both of the acquired signals.

Chips like this one are now common in digital cameras and digital camcorders. These now-common and inexpensive portable devices are enabled by the integration of analog photosensitive pixel structures with mainstream CMOS processes.

4.5 MOS TRANSISTOR FABRICATION AND LAYOUT DESIGN RULES[2]

In addition to choosing the circuit topology, the MOS integrated circuit designer must pick the values of the W/L ratios of the transistors and develop a layout for the circuit that ensures that it will achieve the performance specifications. Design of the layout of transistors and circuits in integrated form is constrained by a set of rules termed the **design rules** or **ground rules.** These rules are technology specific and specify minimum sizes, spacings and overlaps for the various shapes that define transistors. The sets of rules are different for MOS and bipolar processes, for MOS processes designed specifically for logic and memory, and even for similar processes from different companies.

4.5.1 Minimum Feature Size and Alignment Tolerance

Processes are defined around a **minimum feature size** F, which represents the width of the smallest line or space that can be reliably transferred to the surface of a wafer using a given generation of lithographic manufacturing tools. To produce a basic set of ground rules, we must also know the maximum misalignment which can occur between two mask levels during fabrication. For example, Fig. 4.21(a) shows the nominal position of a metal line aligned over a contact window (indicated by the box with and × in it). The metal overlaps the contact window by at least one **alignment tolerance** T in all directions. During the fabrication process, alignment will not be perfect, and the actual structure may exhibit misalignment in the x or y directions or both. Figures 4.21(b) through 4.21(d) show the result of one possible set of worst-case alignments of the patterns in the x, y, and both directions simultaneously. Our set of design rules assume that T is the same in both directions. Transistors designed with our ground rules will fail to operate properly if the misalignment exceeds tolerance T.

4.5.2 MOS Transistor Layout

Figure 4.22 outlines the process and mask sequence used to fabricate a basic polysilicon-gate transistor. The first mask defines the active area, or thin oxide region of the transistor, and the second mask defines the polysilicon gate of the transistor. The channel region of the transistor is actually produced by the intersection of these first two mask layers; the source and/or drain

[2] Reproduced with permission from *Introduction to Microelectronic Fabrication,* Second Edition, by Richard C. Jaeger, Prentice Hall, 2000.

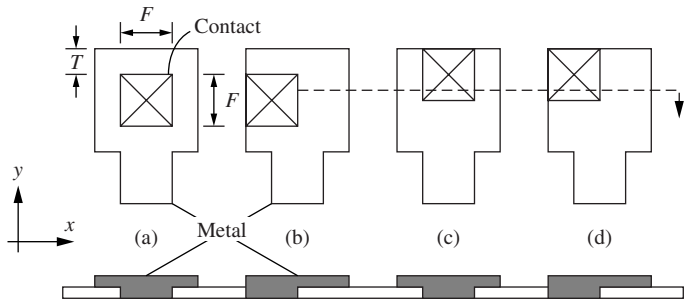


Figure 4.21 Misalignment of a metal pattern over a contact opening: (a) desired alignment, (b) one possible worst-case misalignment in the x direction, (c) one possible worst-case misalignment in the y direction, and (d) misalignment in both directions.

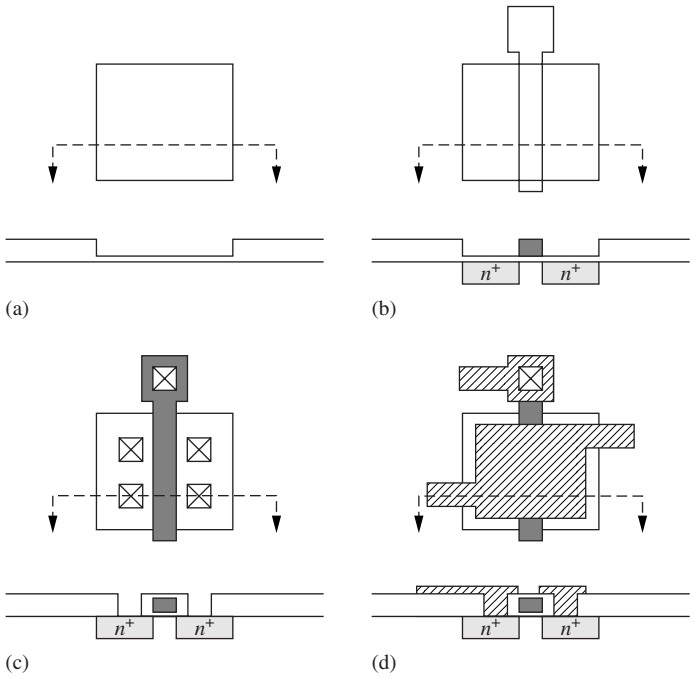


Figure 4.22 (a) Active area mask, (b) gate mask, (c) contact opening mask, and (d) metal mask.

regions are formed wherever the active layer (mask 1) is *not* covered by the gate layer (mask 2). The third and fourth masks delineate the contact openings and the metal pattern. The overall mask sequence is

Active area mask	Mask 1
Polysilicon-gate mask	Mask 2 — align to mask 1
Contact window mask	Mask 3 — align to mask 2
Metal mask	Mask 4 — align to mask 3

The alignment sequence must be specified to properly account for alignment tolerances in the ground rules. In this particular example, each mask is aligned to the one used in the preceding step, but this is not always the case.

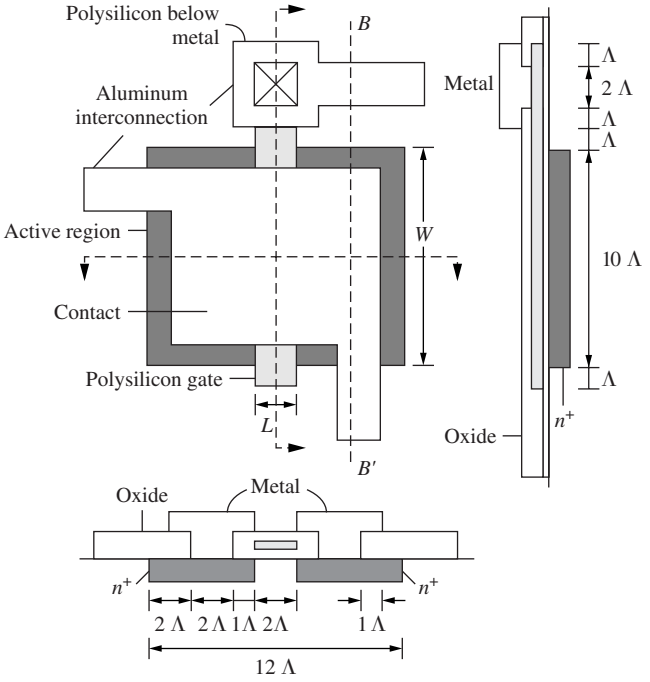


Figure 4.23 Composite top view and cross sections of a transistor with $W/L = 5/1$, demonstrating a basic set of ground rules.

We will now explore a set of design rules similar in concept to those developed by Mead and Conway [3]. These ground rules were designed to permit easy translation of a design from one generation of technology to another by simply changing the size of one parameter Λ. To achieve this goal, the rules are quite forgiving in terms of the mask-to-mask alignment tolerance.

A composite set of rules for a transistor is shown graphically in Fig. 4.23 in which the minimum feature size $F = 2\ \Lambda$ and the alignment tolerance $T = F/2 = \Lambda$. (Parameter Λ could be 1, 0.5, or 0.25 μm, for example.) Note that an alignment tolerance equal to one-half the minimum feature size is a very forgiving alignment tolerance.

For the transistor in Fig. 4.23, all linewidths and spaces must be a minimum feature size of 2 Λ. Square contacts are a minimum feature size of 2 Λ in each dimension. To ensure that the metal completely covers the contact for worst-case misalignment, a 1 Λ border of metal is required around the contact region. The polysilicon gate must overlap the edge of the active area and the contact openings by 1 Λ. However, because of the potential for tolerance accumulation during successive misalignments of masks 2 and 3, the contacts must be inside the edges of the active area by 2 Λ.

The transistor in Fig. 4.23 has a W/L ratio of $10\ \Lambda/2\ \Lambda$ or 5/1, and the total active area is $120\ \Lambda^2$. Thus the active channel region represents approximately 17 percent of the total area of the transistor. Note that the polysilicon gate defines the edges of the source and/or drain regions and results in "self-alignment" of the edges of the gate to the edges of the channel region. Self-alignment of the gate to the channel reduces the size of the transistor and minimizes the "overlap capacitances" associated with the transistor. We will explore these capacitances in more detail in Sec. 4.6.

EXERCISE: What is the active area of the transistor in Fig. 4.23 if $\Lambda = 0.5$ μm? What are the values of W and L for the transistor. What is the area of the transistor gate region? How many of these transistors could be packed together on a 1 cm × 1 cm integrated circuit die if the active areas of the individual transistors must be spaced apart by a minimum of 4 Λ?

ANSWERS: 30 μm^2; 1 μm; 5 μm; 5 μm^2; 1.79 million

4.6 CAPACITANCES IN MOS TRANSISTORS

Every electronic device has internal capacitances that limit the high-frequency performance of the particular device. In logic applications, these capacitances limit the switching speed of the circuits, and in amplifiers, the capacitances limit the frequency at which useful amplification can be obtained. Thus knowledge of the origin and modeling of these capacitances is quite important, and an introductory discussion of the capacitances of the MOS transistor appears in this section.

4.6.1 NMOS TRANSISTOR CAPACITANCES IN THE TRIODE REGION

Figure 4.24 shows the various capacitances associated with the MOS field-effect transistor operating in the triode region, in which the resistive channel region connects the source and drain. A simple model for these capacitances was presented by Meyer [4]. The total gate-channel capacitance C_{GC} is equal to the product of the **gate-channel capacitance** per unit area C''_{ox} (F/m^2) and the area of the gate:

$$C_{GC} = C''_{\text{ox}} W L \tag{4.37}$$

In the Meyer model for the triode region, C_{GC} is partitioned into two equal parts. The **gate-source capacitance** $\boldsymbol{C_{GS}}$ and the **gate-drain capacitance** $\boldsymbol{C_{GD}}$ each consist of one-half of the gate-channel capacitance plus the overlap capacitances $\boldsymbol{C_{GSO}}$ and $\boldsymbol{C_{GDO}}$ associated with the gate-source or gate-drain regions:

$$\begin{aligned} C_{GS} &= \frac{C_{GC}}{2} + C_{GSO} W = C''_{\text{ox}} \frac{WL}{2} + C_{GSO} W \\ C_{GD} &= \frac{C_{GC}}{2} + C_{GDO} W = C''_{\text{ox}} \frac{WL}{2} + C_{GDO} W \end{aligned} \tag{4.38}$$

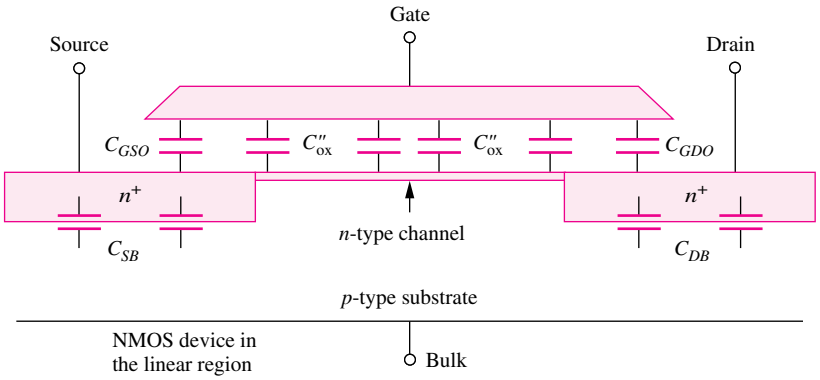


Figure 4.24 NMOS capacitances in the linear region.

The overlap capacitances arise from two sources. First, the gate is actually not perfectly aligned to the edges of the source and drain diffusion but overlaps the diffusions somewhat. In addition, fringing fields between the gate and the source and drain regions contribute to the values of C_{GSO} and C_{GDO}.

The **gate-source** and **gate-drain overlap capacitances** C_{GSO} and C_{GDO} are normally specified as oxide capacitances per unit width (F/m). Note that C_{GS} and C_{GD} each have a component that is proportional to the area of the gate and one proportional to the width of the gate.

The capacitances of the reverse-biased *pn* junctions, indicated by the **source-bulk** and **drain-bulk capacitances** C_{SB} and C_{DB}, respectively, exist between the source and drain diffusions and the substrate of the MOSFET. Each capacitance consists of a component proportional to the junction bottom area of the source (A_S) or drain (A_D) region and a component proportional to the perimeter of the source (P_S) or drain (P_D) junction region:

$$C_{SB} = C_J A_S + C_{\text{JSW}} P_S \qquad C_{DB} = C_J A_D + C_{\text{JSW}} P_D \tag{4.39}$$

Here C_J is called the junction bottom capacitance per unit area (F/m^2), and C_{JSW} is the junction sidewall capacitance per unit length. C_{SB} and C_{DB} will be present regardless of the region of operation. Note that the junction capacitances are voltage dependent [see Eq. (3.21)].

4.6.2 Capacitances in the Saturation Region

In the saturation region of operation, depicted in Fig. 4.25, the portion of the channel beyond the pinch-off point disappears. The Meyer models for the values of C_{GS} and C_{GD} become

$$C_{GS} = \frac{2}{3} C_{GC} + C_{GSO} W \qquad \text{and} \qquad C_{GD} = C_{GDO} W \tag{4.40}$$

in which C_{GS} now contains two-thirds of C_{GC}, but only the overlap capacitance contributes to C_{GD}. Now C_{GD} is directly proportional to W, whereas C_{GS} retains a component dependent on $W \times L$.

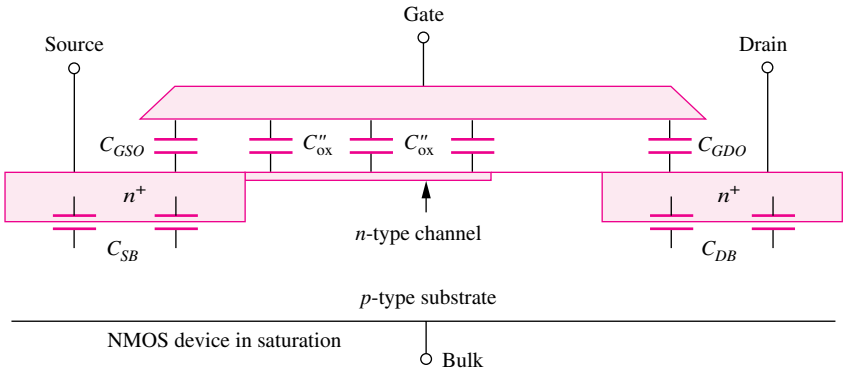


Figure 4.25 NMOS capacitances in the active region.

4.6.3 Capacitances in Cutoff

In the cutoff region of operation, depicted in Fig. 4.26, the conducting channel region is gone. The values of C_{GS} and C_{GD} now contain only the overlap capacitances:

$$C_{GS} = C_{GSO}W \qquad \text{and} \qquad C_{GD} = C_{GDO}W \tag{4.41}$$

In the cutoff region, a small capacitance $\boldsymbol{C_{GB}}$ appears between the gate and bulk terminal, as indicated in Fig. 4.26.

$$C_{GB} = C_{GBO}W \tag{4.42}$$

in which C_{GBO} is the gate-bulk **capacitance per unit width.**

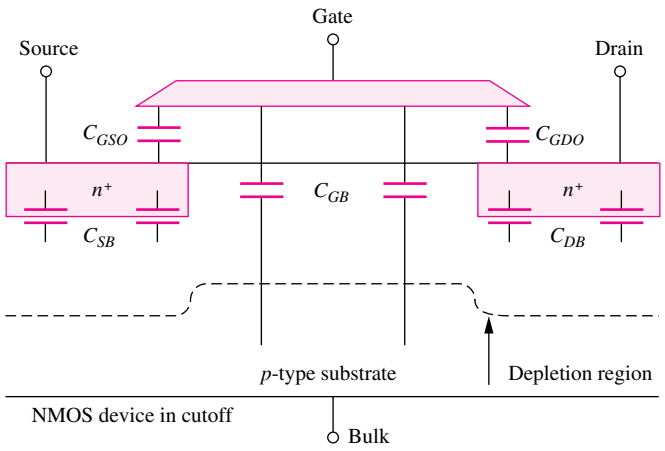


Figure 4.26 NMOS capacitances in the cutoff region.

It should be clear from Eqs. (4.38) to (4.42) that MOSFET capacitances depend on the region of operation of the transistor and are nonlinear functions of the voltages applied to the terminals of the device. In subsequent chapters we analyze the impacts of these capacitances on the behavior of digital and analog circuits. Complete models for these nonlinear capacitances are included in circuit simulation programs such as SPICE, and circuit simulation is an excellent tool for exploring the detailed impact of these capacitances on circuit performance.

Exercise: Calculate C_{GS} and C_{GD} for a transistor operating in the triode region if $C''_{ox} = 200\ \mu\text{F/m}^2$, $C_{GSO} = C_{GDO} = 300\ \text{pF/m}$, $L = 0.5\ \mu\text{m}$, and $W = 5\ \mu\text{m}$?

Answers: 2 fF; 2 fF

4.7 MOSFET Modeling in SPICE

The SPICE circuit analysis program is used to simulate more complicated circuits and to make much more detailed calculations than we can perform by hand analysis. The circuit representation for the MOSFET model that is implemented in SPICE is given in Fig. 4.27, and as we can observe,

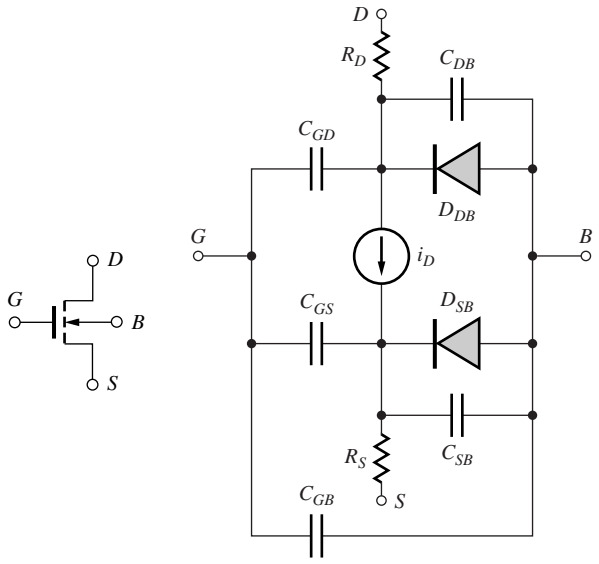


Figure 4.27 SPICE model for the NMOS transistor.

the model uses quite a number of circuits elements in an attempt to accurately represent the characteristics of a real MOSFET. For example, small resistances R_S and R_D appear in series with the external MOSFET source and drain terminals, and diodes are included between the source and drain regions and the substrate. The need for the power of the computer is clear here. It would be virtually impossible for us to use this sophisticated a model in our hand calculations.

As many as 20 different MOSFET models [5] of varying complexity are built into various versions of the SPICE simulation program, and they are denoted by "Level=Model_Number". The levels each have a unique mathematical formulation for current source i_D and for the various device capacitances. The model we have studied in this chapter is the most basic model and is referred to as the level-1 model (LEVEL=1). Largely because of a lack of standard parameter usage at the time SPICE was first written, as well as the limitations of the programming languages originally used, the parameter names that appear in the models differ from those used in this text and throughout the literature. The LEVEL=1 model is coded into SPICE using the following formulas, which are the similar to those we have already studied.

Table 4.2 contains the equivalences of the **SPICE model** parameters and our equations summarized in Sec. 4.2. Typical and default values of the SPICE model parameters can be found in Table 4.2. A similar model is used for the PMOS transistor, but the polarities of the voltages and currents, and the directions of the diodes, are reversed.

$$\text{Triode region:} \quad i_D = \text{KP}\frac{W}{L}\left(v_{GS} - \text{VT} - \frac{v_{DS}}{2}\right)v_{DS}(1 + \text{LAMBDA} \cdot v_{DS})$$

$$\text{Saturation region:} \quad i_D = \frac{\text{KP}}{2}\frac{W}{L}(v_{GS} - \text{VT})^2(1 + \text{LAMBDA} \cdot v_{DS}) \tag{4.43}$$

$$\text{Threshold voltage: VT} = \text{VTO} + \gamma\left(\sqrt{v_{SB} + \text{PHI}} - \sqrt{\text{PHI}}\right)$$

Notice that the SPICE level-1 description includes the addition of channel-length modulation to the triode region expression. Also, be sure not to confuse SPICE threshold voltage **VT** with thermal voltage V_T.

TABLE 4.2
SPICE Parameter Equivalences

PARAMETER	OUR TEXT	SPICE	DEFAULT
Transconductance	K_n or K_p	KP	20 μA/V^2
Threshold voltage	V_{TN} or V_{TP}	VT	—
Zero-bias threshold voltage	V_{TO}	VTO	1V
Surface potential	$2\phi_F$	PHI	0.6 V
Body effect	γ	GAMMA	0
Channel length modulation	λ	LAMBDA	0
Mobility	μ_n or μ_p	UO	600 cm^2/V · s
Gate-drain capacitance per unit width	C_{GDO}	CGDO	0
Gate-source capacitance per unit width	C_{GSO}	CGSO	0
Gate-bulk capacitance per unit width	C_{GBO}	CGBO	0
Junction bottom capacitance per unit area	C_J	CJ	0
Grading coefficient	MJ	MJ	0.5 V$^{0.5}$
Sidewall capacitance	C_{JSW}	CJSW	0
Sidewall grading coefficient	MJSW	MJSW	0.5 V$^{0.5}$
Oxide thickness	T_{ox}	TOX	100 nm
Junction saturation current	I_S	IS	10 fA
Built-in potential	ϕ_j	PB	0.8 V
Ohmic drain resistance	—	RD	0
Ohmic source resistance	—	RS	0

The junction capacitances are modeled in SPICE by a generalized form of the capacitance expression in Eq. (3.21)

$$C_J = \frac{\text{CJO}}{\left(1 + \dfrac{v_R}{\text{PB}}\right)^{\text{MJ}}} \quad \text{and} \quad C_{\text{JSW}} = \frac{\text{CJSWO}}{\left(1 + \dfrac{v_R}{\text{PB}}\right)^{\text{MJSW}}} \tag{4.44}$$

in which v_R is the reverse bias across the pn junction.

EXERCISE: What are the values of SPICE model parameters **KP, LAMBDA, VTO, PHI,** W, and L for a transistor with the following characteristics: $V_{TN} = 1$ V, $K_n = 150$ μA/V^2, $W = 1.5$ μm, $L = 0.25$ μm, $\lambda = 0.0133$ V^{-1}, and $2\phi_F = 0.6$ V?

ANSWERS: 150 μA/V^2; 0.0133 V^{-1}; 1 V; 0.6 V; 1.5 μm; 0.25 μm (specified in SPICE as 150U; 0.0133; 1; 0.6; 1.5U; 0.25U)

4.8 BIASING THE NMOS FIELD-EFFECT TRANSISTOR

As stated before, the MOS circuit designer has the flexibility to choose the circuit topology and W/L ratios of the devices in the circuit, and to a lesser extent, the voltages applied to the devices. As designers, we need to develop a mental catalog of useful circuit configurations, and we begin by looking at several basic circuits for biasing the MOSFET.

We have found that the MOSFET has three regions of operation: cutoff, triode, and saturation. For circuit applications, we want to establish a well-defined **quiescent operating point,** or **Q-point,** for the MOSFET in a particular region of operation. The Q-point for the MOSFET is represented by the dc values (I_D, V_{DS}) that locate the operating point on the MOSFET output characteristics. [In reality, we need the three values (I_D, V_{DS}, V_{GS}), but two are enough if we know the region of operation of the device.]

For binary logic circuits investigated in detail in Part II of this text, the transistor acts as an "on-off" switch, and the Q-point is set to be in either the cutoff region ("off") or the triode region ("on"). For analog circuits discussed in Part III, the Q-point is most often located in the saturation region, a region in which relatively high voltage, current, and/or power gain can be achieved.

For hand analysis and design of Q-points, channel-length modulation is usually ignored by assuming $\lambda = 0$. A review of Fig. 4.13 indicates that including λ changes the drain current by less than 10 percent. Generally, we do not know the values of transistor parameters to this accuracy, and the tolerances on both discrete or integrated circuit elements may be as large as 30 to 50 percent. If you explore some transistor specification sheets (see CD ROM or MCD website), you will discover parameters that have a 4 or 5 to 1 spread in values. You will also find parameters with only a minimum or maximum value specified. Thus, neglecting λ will not significantly affect the validity of our analysis. Also, many bias circuits involve feedback which further reduces the influence of λ. On the other hand, in Part III we will see that λ can play an extremely important role in limiting the voltage gain of analog amplifier circuits, and the effect of λ must often be included in the analysis of these circuits.

To analyze circuits containing MOSFETs, we must first assume a region of operation, just as we did to analyze diode circuits in Chapter 3. The bias circuits that follow will most often be used to place the transistor Q-point in the saturation region, and by examining Eq. (4.30) with $\lambda = 0$, we see that we must know the gate-source voltage V_{GS} to calculate the drain current I_D. Then, once we know I_D, we can find V_{DS} from the constraints of Kirchhoff's voltage law. Thus our most frequently used analysis approach will be to first find V_{GS} and then to use its value to find the value of I_D. I_D will then be used to calculate V_{DS}.

Menu for Bias Analysis

1. Assume a region of operation (Most often the saturation region)
2. Use circuit analysis to find V_{GS}
3. Use V_{GS} to calculate I_D, and I_D to determine V_{DS}
4. Check the validity of the operating region assumptions
5. Change assumptions and analyze again if necessary

DESIGN NOTE

SATURATION BY CONNECTION!

When making bias calculations for analysis or design, it is useful to remember that an NMOS *enhancement-mode* device that is operating with $V_{DS} = V_{GS}$ will always be in the pinch-off region. The same is true for an enhancement-mode PMOS transistor with $V_{SD} = V_{SG}$.

To demonstrate this result, it is easiest to keep the signs straight by considering an NMOS device with dc bias. For pinch-off, it is required that

$$V_{DS} \geq V_{GS} - V_{TN}$$

But if $V_{DS} = V_{GS}$, this condition becomes

$$V_{DS} \geq V_{DS} - V_{TN} \qquad \text{or} \qquad V_{TN} \geq 0$$

which is always true if V_{TN} is a positive number. $V_{TN} > 0$ corresponds to an NMOS enhancement-mode device. Thus an enhancement-mode device operating with $V_{DS} = V_{GS}$ is always in the saturation region! Similar arguments hold true for enhancement-mode PMOS devices operating with $V_{SD} = V_{SG}$.

EXAMPLE 4.1(a) **CONSTANT GATE-SOURCE VOLTAGE BIAS**

A basic bias circuit for the NMOS transistor is shown in Fig. 4.28, in which dc voltage source V_{GG} is used to establish a fixed gate-source bias for the MOSFET, source V_{DD} supplies drain current to the NMOS transistor through resistor R_D, and the value of R_D determines V_{DS}. This circuit is used to introduce a number of concepts related to biasing, but we shall find that it is not a very useful circuit in practical applications.

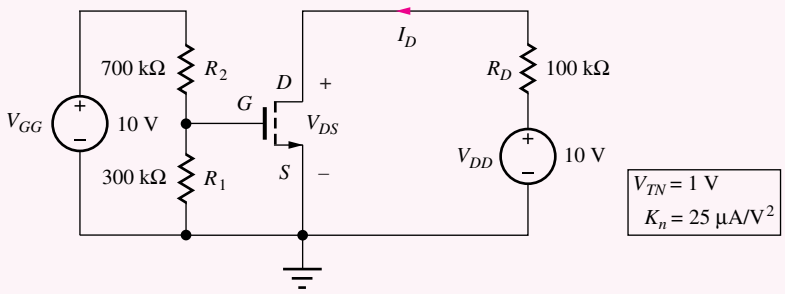


Figure 4.28 Constant gate-voltage bias using a voltage divider.

PROBLEM Find the quiescent operating point Q-point (I_D, V_{DS}) for the MOSFET in the fixed gate bias circuit in Fig. 4.28.

SOLUTION **Known Information and Given Data:** Circuit schematic in Fig. 4.28 with $V_{DD} = 10$ V, $V_{GG} = 10$ V, $R_1 = 300$ kΩ, $R_2 = 700$ kΩ, $R_D = 100$ kΩ, $V_{TN} = 1$ V, $K_n = 25\,\text{mA/V}^2$, $I_G = 0$, and $I_B = 0$

Unknowns: I_D, V_{DS}, and V_{GS}

Approach: We can find the Q-point using the mathematical model for the NMOS transistor. We must assume a region of operation, determine the Q-point, and then see if the resulting Q-point is consistent with the assumed region of operation.

Assumptions: We will assume that the MOSFET is pinched-off: $I_D = (K_n/2)(V_{GS} - V_{TN})^2$. Remember, we ignore λ in hand bias calculations. This assumption simplifies the mathematics because I_D is then modeled as being independent of V_{DS}.

Analysis: From the drain current expression and given data, we see that if we first find V_{GS}, then we can use it to find I_D. First label the variables in the circuit including I_D, V_{DS}, and V_{GS}. Then to simplify the analysis, we replace the gate-bias network consisting of V_{GG}, R_1, and R_2

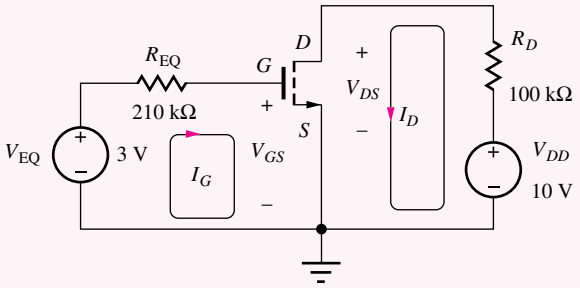


Figure 4.29 Simplified MOSFET bias circuit.

with its Thévenin equivalent circuit as in Fig. 4.29 in which

$$V_{EQ} = \frac{R_1}{R_1 + R_2} V_{GG} = 3 \text{ V} \qquad \text{and} \qquad R_{EQ} = \frac{R_1 R_2}{R_1 + R_2} = 210 \text{ k}\Omega$$

We apply Kirchhoff's voltage law (KVL) to the loop containing the gate-source terminals of the device (referred to here as the input loop):

$$V_{EQ} = I_G R_{EQ} + V_{GS} \tag{4.45}$$

But, we know that $I_G = 0$ for the MOSFET, so that $V_{GS} = V_{EQ} = 3$ V. We can now find I_D using the transistor parameters from Fig. 4.28:

$$I_D = \frac{K_n}{2}(V_{GS} - V_{TN})^2 = \frac{25 \times 10^{-6}}{2} \frac{\mu\text{A}}{\text{V}^2} (3 - 1)^2 \text{ V}^2 = 50 \, \mu\text{A}$$

To determine V_{DS} we write a loop equation including the drain-source terminals of the device (referred to here as the output loop):

$$V_{DD} = I_D R_D + V_{DS} \tag{4.46}$$

Again substituting the values from Fig. 4.29,

$$V_{DS} = 10 \text{ V} - (50 \times 10^{-6} \text{ A})(10^5 \, \Omega) = 5.00 \text{ V}$$

Check of Results: We have $V_{DS} = 5$ V and $V_{GS} - V_{TN} = 2$ V. Since V_{DS} exceeds $V_{GS} - V_{TN}$, the transistor is indeed pinched-off and in the saturation region. Thus, the Q-point is (50.0 μA, 5.00 V) with $V_{GS} = 3$ V.

Discussion: Although this circuit introduces a number of concepts related to biasing, it is not a very useful circuit in practical applications because the Q-point is very sensitive to variations in the values of the transistor parameters. If the value of V_{GS} is fixed in the drain current expression, then I_D varies in direct proportion to K_n and depends on the square of changes in V_{TN}. The bias circuits that we will explore in Exs. 4.3 and 4.7 provide a much reduced sensitivity of the Q-point to changes in device parameters and are preferred methods of biasing the transistor.

EXERCISE: Find the Q-point for the circuit in Fig. 4.29 if R_D is changed to 50 kΩ.

ANSWER: (50.0 μA, 7.50 V)

EXERCISE: Find the Q-point for the circuit in Fig. 4.29 if $R_1 = 270\,\text{k}\Omega$, $R_2 = 750\,\text{k}\Omega$, and $R_D = 100\,\text{k}\Omega$.

ANSWER: (33.9 μA, 6.61 V)

EXERCISE: Suppose that $K_n = 30\ \mu\text{A/V}^2$ instead of $25\ \mu\text{A/V}^2$ as in Ex. 4.1. What are the new values of V_{GS}, I_D, and V_{DS}?

ANSWER: (3 V, 60.0 μA, 4 V) (Note in this circuit that I_D is directly proportional to K_n.)

EXERCISE: Suppose that V_{TN} is 1.5 V instead of 1 V in Ex. 4.1. What are the new values of V_{GS}, I_D, and V_{DS}?

ANSWER: (3 V, 28.1 μA, 7.19 V) (We see that the current is also quite sensitive to the value of V_{TN}.)

EXAMPLE 4.1(b) ANALYSIS INCLUDING THE EFFECT OF CHANNEL-LENGTH MODULATION

It has been argued several times thus far that λ can be neglected in bias calculations. So, before we leave the constant gate bias circuit behind, let us repeat the bias calculation above with $\lambda = 0.02\ \text{V}^{-1}$.

PROBLEM Find the quiescent operating point Q-point for the MOSFET in the fixed gate bias circuit in Fig. 4.28 with $\lambda = 0.02\ \text{V}^{-1}$.

SOLUTION **Known Information and Given Data:** Simplified circuit schematic in Fig. 4.29 with $V_{DD} = 10\,\text{V}$, $R_D = 100\,\text{k}\Omega$, $V_{TN} = 1\,\text{V}$, $K_n = 25\,\mu\text{A/V}^2$, $\lambda = 0.02\,\text{V}^{-1}$, $I_G = 0$, $I_B = 0$, and $V_{GS} = V_{EQ} = 3\,\text{V}$.

Unknowns: I_D, V_{DS}

Approach: We can make use of the information from the previous example. For this circuit, including a nonzero value of λ does not affect the equations describing the input loop. So $V_{GS} = 3\,\text{V}$, and we can directly reevaluate the drain current expression.

Assumptions: Assume that the MOSFET is in the pinch-off region. But now

$$I_D = \frac{K_n}{2}(V_{GS} - V_{TN})^2(1 + \lambda V_{DS}).$$

Analysis: To find V_{DS}, we still have

$$V_{DS} = V_{DD} - I_D R_D$$

Combining this equation with the expression for the drain current yields

$$V_{DS} = V_{DD} - \frac{K_n R_D}{2}(V_{GS} - V_{TN})^2(1 + \lambda V_{DS})$$

and substituting the values from Fig. 4.29 yields

$$V_{DS} = 10 - \frac{(25 \times 10^{-6})(10^5)}{2}(3 - 1)^2(1 + 0.02\ V_{DS})$$

in which the units have been eliminated for simplicity. Solving for V_{DS} yields $V_{DS} = 4.55\,\text{V}$. Using this value to calculate the drain current gives

$$I_D = \frac{25 \times 10^{-6}}{2}(3-1)^2[1 + 0.02(4.55)] = 54.5\,\mu\text{A}$$

Check of Results: We see that $V_{DS} = 4.55\,\text{V}$ exceeds $V_{GS} - V_{TN} = 2\,\text{V}$ so that the transistor is indeed pinched-off. Thus, the saturation region assumption is justified. The final Q-point is (54.5 μA, 4.55 V).

Discussion: We see that the Q-point values have each changed by approximately 10 percent from (50 μA, 5 V) to (54.5 μA, 4.55 V). From a practical point of view, the tolerances on circuit element and transistor parameter values will completely swamp out these small differences. Therefore we gain little from the additional complexity of including λ in our hand calculations. Note that, although this particular calculation including λ may have seemed relatively painless, the relative ease is an artifact of this particular circuit. Including λ in calculations for other bias circuits is considerably more difficult. On the other hand, if we use a circuit analysis program to perform the calculations, we might as well include λ.

EXERCISE: Repeat the channel length modulation calculation for $\lambda = 0.01\ \text{V}^{-1}$. What are the new values of I_D and V_{DS}.

ANSWER: (52.4 μA, 4.76 V)

EXAMPLE 4.2 LOAD LINE ANALYSIS

The Q-point for the MOSFET circuit in Fig. 4.29 can also be found graphically with a load-line method very similar to the one used for analysis of diode circuits in Sec. 3.10. The graphical approach helps us visualize the operating point of the device and its location relative to the boundaries between the cutoff, triode and pinch-off regions of operation.

PROBLEM Use load line analysis to locate the Q-point for the MOSFET in the fixed gate bias circuit in Fig. 4.29.

SOLUTION **Known Information and Given Data:** Circuit schematic in Fig. 4.29 with $V_{DD} = 10\,\text{V}$, $V_{EQ} = 3\,\text{V}$, $R_{EQ} = 210\,\text{k}\Omega$, $R_D = 100\,\text{k}\Omega$, $V_{TN} = 1\,\text{V}$, $K_n = 25\,\mu\text{A/V}^2$, $I_G = 0$, and $I_B = 0$

Unknowns: Q-point = (I_D, V_{DS})

Approach: We need to find an equation for the load line, $I_D = f(V_{DS})$, so that it can be plotted on the output i-v characteristics. The Q-point can then be located on the output characteristics. Equation (4.46) represents the *load line* for this MOSFET circuit and is repeated here:

$$V_{DD} = I_D R_D + V_{DS}$$

Assumptions: We have already found $V_{GS} = 3\,\text{V}$ using the techniques in Ex. 4.1(a).

Analysis: For the values for the circuit in Fig. 4.29, the load line equation becomes

$$10 = 10^5 I_D + V_{DS}$$

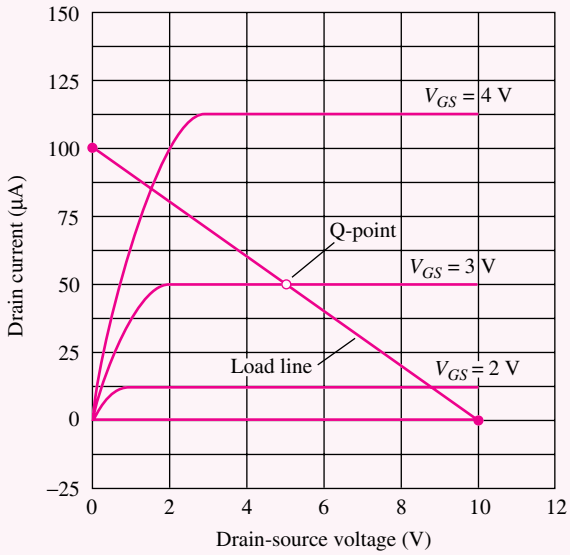


Figure 4.30 Load line for the circuit in Figs. 4.28 and 4.29.

Just as for the diode circuits in Sec. 3.10, the load line is constructed by finding two points on the line: for $V_{DS} = 0$, $I_D = 100\,\mu\text{A}$, and for $I_D = 0$, $V_{DS} = 10\,\text{V}$. The resulting line is drawn on the output characteristics of the MOSFET in Fig. 4.30. The family of NMOS curves intersects the load line at many different points (actually infinitely many since each possible gate voltage corresponds to a different curve). The gate-source voltage is the parameter that determines which of the intersection points is the actual Q-point. In this circuit, we already found $V_{GS} = 3\,\text{V}$; the Q-point is indicated by the circle in the Fig. 4.30. Reading the values from the graph yields $V_{DS} = 5\,\text{V}$ and $I_D = 50\,\mu\text{A}$.

Check of Results: This is the same Q-point that we found using our mathematical model for the MOSFET.

Discussion: From the graph, we can immediately see that the Q-point is in the saturation region of the transistor output characteristics. The Q-point is fairly well centered in the saturation region of operation, and the drain-source voltage is 1.5 V greater than that required to saturate the device.

Although we will seldom actually solve bias problems using graphical techniques, it is very useful to visualize the location of the Q-point in terms of the load line on the output characteristics as in Fig. 4.30. We can readily see if the device is operating in the triode or saturation regions as well as how far the operating point is from the boundaries between the various regions of operation.

EXERCISE: Draw the new load line and find the Q-point if R_D is changed to 66.7 kΩ.

ANSWER: (50 μA, 6.7 V)

EXAMPLE 4.3 FOUR-RESISTOR BIASING

The circuit in Fig. 4.28 provides a fixed gate-source bias voltage to the transistor. Theoretically, this works fine. However, in practice the values of K_n, V_{TN}, and λ for the MOSFET will not be known with high precision. In addition, we must be concerned about resistor and power supply tolerances (you may wish to review Sec. 1.8) as well as component value drift with both time and temperature in an actual circuit.

The most general and important bias method that we will encounter is the **four-resistor bias** circuit in Fig. 4.31(a). The addition of the fourth resistor R_S helps stabilize the MOSFET Q-point in the face of many types of circuit parameter variations. This bias circuit is actually a form of *feedback circuit,* which will be studied in great detail in Chapters 12 and 18. Also observe that a single voltage source V_{DD} is now used to supply both the gate-bias voltage and the drain current.

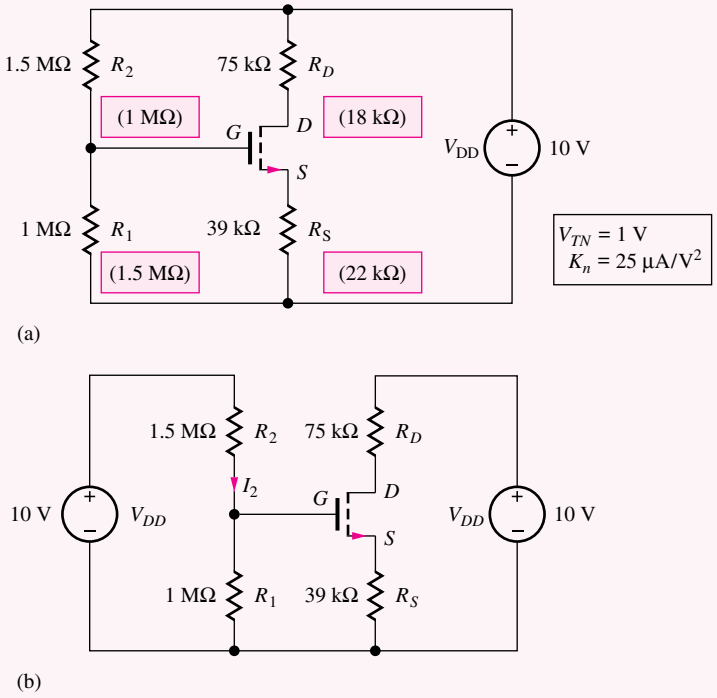


Figure 4.31 (a) Four-resistor bias network for a MOSFET. (b) Equivalent circuit with replicated sources. The shaded values in part (a) are used in Ex. 4.4.

PROBLEM Find the Q-point = (I_D, V_{DS}) for the MOSFET in the four resistor bias circuit in Fig. 4.31.

SOLUTION **Known Information and Given Data:** Circuit schematic in Fig. 4.31 with $V_{DD} = 10$ V, $R_1 = 1\,\text{M}\Omega$, $R_2 = 1.5\,\text{M}\Omega$, $R_D = 75\,\text{k}\Omega$, $R_S = 39\,\text{k}\Omega$, $K_n = 25\,\mu\text{A/V}^2$, and $V_{TN} = 1$ V.

Unknowns: Q-point = (I_D, V_{DS}), V_{GS}, and region of operation

Approach: We can find the Q-point using the mathematical model for the NMOS transistor. We assume a region of operation, determine the Q-point, and check to see if the resulting Q-point is consistent with the assumed region of operation.

Assumptions: The first step in our Q-point analysis of the equivalent circuit in Fig. 4.31 is to assume that the transistor is saturated (remember to use $\lambda = 0$):

$$I_D = \frac{K_n}{2}(V_{GS} - V_{TN})^2 \tag{4.47}$$

Also, $I_G = 0 = I_B$. Using the $\lambda = 0$ assumption simplifies the mathematics because I_D is then modeled as being independent of V_{DS}. (The four-resistor bias circuit is most often used to place the transistor in the saturation region of operation for use as an amplifier for analog signals.)

Analysis: To find I_D, the gate-source voltage must be determined, and we begin by simplifying the circuit. In the equivalent circuit in Fig. 4.31(b), the voltage source V_{DD} has been split into two equal-valued sources, and we recognize that the gate-bias voltage is determined by V_{EQ} and R_{EQ}, exactly as in Figs. 4.28 and 4.29. After the Thévenin transformation is applied to this circuit, the resulting equivalent circuit is given in Fig. 4.32 in which the variables have been clearly labeled. This is the final circuit to be analyzed.

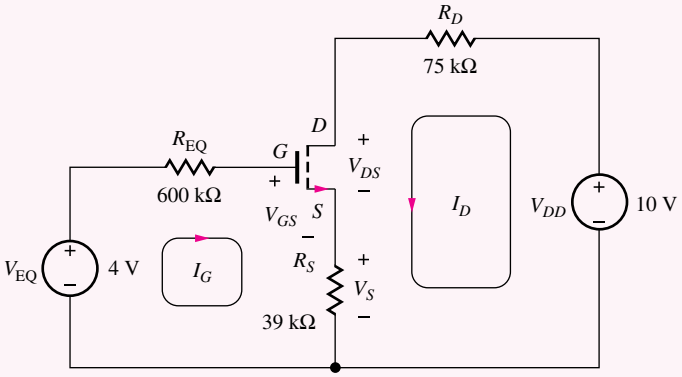


Figure 4.32 Equivalent circuit for the four-resistor bias network.

Detailed analysis begins by writing the input loop equation containing V_{GS}:

$$V_{EQ} = I_G R_{EQ} + V_{GS} + (I_G + I_D)R_S \qquad \text{or} \qquad V_{EQ} = V_{GS} + I_D R_S \tag{4.48}$$

because we know that $I_G = 0$. Substituting Eq. (4.47) into Eq. (4.48) yields

$$V_{EQ} = V_{GS} + \frac{K_n R_s}{2}(V_{GS} - V_{TN})^2 \tag{4.49}$$

and we have a quadratic equation to solve for V_{GS}. For the values in Fig. 4.32 with $V_{TN} = 1\,\text{V}$ and $K_n = 25\,\mu\text{A/V}^2$,

$$4 = V_{GS} + \frac{(25 \times 10^{-6})(3.9 \times 10^4)}{2}(V_{GS} - 1)^2$$

and

$$V_{GS}^2 + 0.05\,V_{GS} - 7.21 = 0 \qquad \text{for which} \qquad V_{GS} = -2.71\,\text{V}, +2.66\,\text{V}$$

For $V_{GS} = -2.71\,\text{V}$, the MOSFET would be cut off because $V_{GS} < V_{TN}$. Therefore, $V_{GS} = +2.66\,\text{V}$ must be the answer we seek, and $I_D = 34.4\,\mu\text{A}$ is found using Eq. (4.47).

The second part of the Q-point, V_{DS}, can now be determined by writing the "output" loop equation including the drain-source terminals of the device:

$$V_{DD} = I_D R_D + V_{DS} + (I_G + I_D)R_S \qquad \text{or} \qquad V_{DD} = I_D(R_D + R_S) + V_{DS} \tag{4.50}$$

Eq. (4.50) has been simplified since we know that $I_G = 0$. Substituting the values from the circuit gives

$$10\,\text{V} = (34.4\,\mu\text{A})(75\,\text{k}\Omega + 39\,\text{k}\Omega) + V_{DS} \qquad \text{or} \qquad V_{DS} = 6.08\,\text{V}$$

Check of Results: Checking the saturation region assumption, we have

$$V_{DS} = 6.08\,\text{V},\ V_{GS} - V_{TN} = 1.66\,\text{V} \qquad \text{and} \qquad V_{DS} > (V_{GS} - V_{TN}) \quad \checkmark$$

The saturation region assumption is consistent with the resulting Q-point: (34.4 μA, 6.08 V) with $V_{GS} = 2.66$ V.

Discussion: The four-resistor bias circuit is one of the best for biasing transistors in discrete circuits. The bias point is well stabilized with respect to device parameter variations and temperature changes. The four-resistor bias circuit is most often used to place the transistor in the saturation region of operation for use as an amplifier for analog signals, and as mentioned at the beginning of this example, the bias circuit in Fig. 4.31 represents a type of feedback circuit that uses negative feedback to stabilize the operating point. The operation of this feedback mechanism can be viewed in the following manner. Suppose for some reason that I_D begins to increase. Equation (4.48) indicates that an increase in I_D must be accompanied by a decrease in V_{GS} since V_{EQ} is fixed. But, this decrease in V_{GS} will tend to restore I_D back to its original value [see Eq. (4.47)]. This is negative feedback in action!

Note that this circuit uses the three-terminal representation for the MOSFET, in which it is assumed that the bulk terminal is tied to the source. If the bulk terminal is instead grounded, the analysis becomes more complex because the threshold voltage is then a function of the voltage developed at the source terminal of the device. This case will be investigated in more detail in Ex. 4.5. Let us now use the computer to explore the impact of neglecting λ in our hand analysis.

Computer-Aided Analysis: If we use SPICE to simulate the circuit using a LEVEL = 1 model and the parameters from our hand analysis (KP = 25 μA/V^2 and VTO = 1 V), we get exactly the same Q-point (34.4 μA, 6.08 V). If we add LAMBDA = 0.02 V^{-1}, SPICE yields a new Q-point of (35.9 μA, 5.91 V). The Q-point values change by less than 5 percent, a value that is well below our uncertainty in the device parameter and resistor values in a real situation.

EXERCISE: Suppose K_n increases to 30 μA/V^2 for the transistor in Fig. 4.32. What is the new Q-point for the circuit?

ANSWER: (36.8 μA, 5.81 V)

EXERCISE: Suppose V_{TN} changes from 1 V to 1.5 V for the MOSFET in Fig. 4.32. What is the new Q-point for the circuit?

ANSWER: (26.7 μA, 6.96 V)

EXERCISE: Find the Q-point in the circuit in Fig. 4.31 if R_S is changed to 62 kΩ.

ANSWER: (25.2 μA, 6.55 V)

DESIGN EXAMPLE 4.4

FOUR-RESISTOR BIAS REDESIGN

Let us redesign the four-resistor bias network in Ex. 4.3 to increase the current while keeping V_{DS} approximately the same; the new Q-point will be (100 μA, 6 V).

PROBLEM Find the new values of R_S and R_D that will change the Q-point to (100 μA, 6 V).

SOLUTION **Known Information and Given Data:** Simplified circuit schematic in Fig. 4.32 with $V_{EQ} = 4\,\text{V}$, $R_{EQ} = 600\,\text{k}\Omega$, $K_n = 25\,\mu\text{A/V}^2$, $V_{TN} = 1\,\text{V}$, $I_G = 0$, $I_B = 0$, $I_D = 100\,\mu\text{A}$, and $V_{DS} = 6\,\text{V}$

Unknowns: V_{GS}, R_S, and R_D

Approach: The source and drain currents are controlled by the input loop and the value of R_S, which will be changed to achieve the desired value of I_D. The drain-source voltage can then be adjusted by changing the value of R_D.

Assumptions: Use the MOSFET saturation region model with $\lambda = 0$:

$$I_D = \frac{K_n}{2}(V_{GS} - V_{TN})^2$$

Analysis: Equation (4.48) can be rearranged to find the required value of R_S:

$$R_S = \frac{V_{EQ} - V_{GS}}{I_D} = \frac{V_S}{I_D} \tag{4.51}$$

but we must first find the new value of V_{GS}. (I_D is changed so V_{GS} must change.)

The gate-source voltage V_{GS} needed to establish $I_D = 100\,\mu\text{A}$ is found by rearranging the saturation region expression for the NMOS drain current, Eq. (4.30), with $\lambda = 0$:

$$V_{GS} = V_{TN} + \sqrt{\frac{2I_{DS}}{K_n}} = 1\,\text{V} + \sqrt{\frac{2(100\,\mu\text{A})}{25\,\frac{\mu\text{A}}{\text{V}^2}}} = 3.83\,\text{V} \tag{4.52}$$

Note that the positive root is used here since V_{GS} must exceed V_{TN} for conduction. Substituting this value in Eq. (4.52) yields

$$R_S = \frac{4\,\text{V} - 3.83\,\text{V}}{100\,\mu\text{A}} = \frac{0.17\,\text{V}}{100\,\mu\text{A}} = 1.7\,\text{k}\Omega$$

By rearranging the second expression in Eq. (4.50), we see that the sum of R_D and R_S in the bias network of Fig. 4.32 is determined by the desired Q-point values:

$$R_D + R_S = \frac{V_{DD} - V_{DS}}{I_D} = \frac{10\,\text{V} - 6\,\text{V}}{100\,\mu\text{A}} = 40\,\text{k}\Omega$$

and

$$R_D = (40 - 1.7)\,\text{k}\Omega = 38.3\,\text{k}\Omega$$

From Appendix A, the nearest standard 5 percent resistor values are $R_S = 1.6$ or $1.8\,\text{k}\Omega$ and $R_D = 39\,\text{k}\Omega$. Here we choose $R_S = 1.8\,\text{k}\Omega$ which will yield a drain current that is slightly lower than the design value, but, in the absence of any addition information, $1.6\,\text{k}\Omega$ would be an equally valid choice.

Since R_D and R_S are not exactly what we calculated, the values of V_{GS}, I_D, and V_{DS} will vary slightly from the design values. Using the approach in Ex. 4.3, the Q-point is found to be (99.5 μA, 5.95 V) with $V_{GS} = 3.82$ V.

Check of Results: For this design, we now have

$$V_{DS} = 5.95\,\text{V} \qquad V_{GS} - V_{TN} = 2.82\,\text{V} \qquad \text{and} \qquad V_{DS} > (V_{GS} - V_{TN}) \quad \checkmark$$

The saturation region assumption is consistent with the solution.

Discussion: Note that although the value of R_S is 6 percent larger than the calculated value, I_D changed by less than 0.5 percent. Once again we see the effects of feedback in action!

Although $R_S = 1.8\,\text{k}\Omega$ represents a reasonable value of resistance, the voltage developed at the source of the MOSFET — only 0.17 V — is quite small and will be highly sensitive to changes in V_{DD}, V_{TN}, R_1, and R_2. If we pick a larger value of V_{EQ}, a greater value of V_S will appear across R_S, and the circuit design will be far less dependent on the device parameters. (See Prob. 4.91.)

So let us increase V_{EQ} from 4 to 6 V, which will directly increase V_S by 2 V — see Eq. (4.51). The new value of R_S is

$$R_S = \frac{6\,\text{V} - 3.83\,\text{V}}{100\,\mu\text{A}} = \frac{2.17\,\text{V}}{100\,\mu\text{A}} = 21.7\,\text{k}\Omega$$

and

$$R_D = (40 - 21.2)\,\text{k}\Omega = 18.3\,\text{k}\Omega$$

From Appendix A, the nearest standard 5 percent resistor values are now $R_S = 22\,\text{k}\Omega$ and $R_D = 18\,\text{k}\Omega$.

The values of R_1 and R_2 must be modified to set V_{EQ} to 6 V. If we simply interchange the values of R_1 and R_2 in Fig. 4.31, we will have $V_{EQ} = 6$ V, with R_{EQ} remaining 600 kΩ. Our final design values, $R_1 = 1.5\,\text{M}\Omega$, $R_2 = 1\,\text{M}\Omega$, $R_S = 22\,\text{k}\Omega$, and $R_D = 18\,\text{k}\Omega$, are indicated by the shaded numbers in parentheses in Fig. 4.31(a).

EXERCISE: Show that the actual Q-point in the circuit in Fig. 4.31 for $R_1 = 1.5\,\text{M}\Omega$, $R_2 = 1\,\text{M}\Omega$, $R_S = 1.7\,\text{k}\Omega$, and $R_D = 39\,\text{k}\Omega$ is (99.5 μA, 5.95 V)

EXERCISE: Find the Q-point in the circuit in Fig. 4.31 for $R_1 = 1.5\,\text{M}\Omega$, $R_2 = 1\,\text{k}\Omega$, $R_S = 22\,\text{k}\Omega$, and $R_D = 18\,\text{k}\Omega$.

ANSWER: (99.1 μA, 6.04 V)

EXERCISE: Redesign the values of R_1 and R_2 to set the bias current to 2 μA while maintaining $V_{EQ} = 6$ V. What is the value of R_{EQ}?

ANSWER: 3 MΩ, 2 MΩ, 1.2 MΩ

DESIGN NOTE

GATE VOLTAGE DIVIDER DESIGN

Resistors R_1 and R_2 in Fig. 4.31 are required to set the value of V_{EQ}, but the current in the resistors does not contribute directly to operation of the transistor. Thus we would like to minimize the current "lost" through R_1 and R_2. The sum $(R_1 + R_2)$ sets the current in the gate bias resistors. As a rule of thumb, $R_1 + R_2$ is usually chosen to limit the current to no more than a few percent of the value of the drain current. In Fig. 4.31, the value of current I_2 is 4 percent of the drain current:

$$I_2 = \frac{10\,\text{V}}{1\,\text{M}\Omega + 1.5\,\text{M}\Omega} = 4\,\mu\text{A}$$

EXAMPLE 4.5

ANALYSIS INCLUDING BODY EFFECT

The NMOS transistor in Fig. 4.32 was connected as a three-terminal device. This example explores how the Q-point is altered when the substrate is connected as shown in Fig. 4.33.

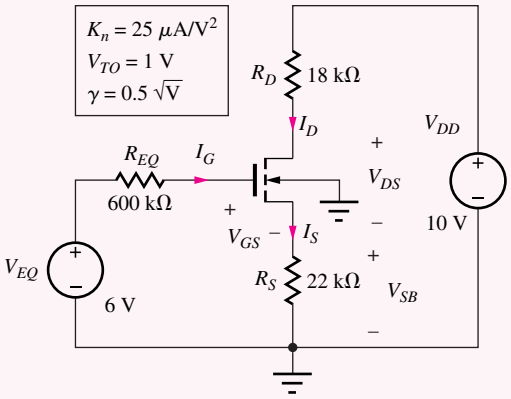


Figure 4.33 MOSFET with redesigned bias circuit.

PROBLEM Find the Q-point $= (I_D, V_{DS})$ for the MOSFET in the four-resistor bias circuit in Fig. 4.33 including the influence of body effect on the transistor threshold.

SOLUTION **Known Information and Given Data:** The circuit schematic in Fig. 4.33 with $V_{EQ} = 6\,\text{V}$, $R_{EQ} = 600\,\text{k}\Omega$, $R_S = 22\,\text{k}\Omega$, $R_D = 18\,\text{k}\Omega$, $K_n = 25\,\mu\text{A/V}^2$, $V_{TO} = 1\,\text{V}$, and $\gamma = 0.5\,\text{V}^{-1}$

Unknowns: I_D, V_{DS}, V_{GS}, V_{BS}, V_{TN}, and region of operation

Approach: In this case, the source-bulk voltage, $V_{SB} = I_S R_S = I_D R_S$, is no longer zero, and we must solve the following set of equations:

$$\begin{aligned} V_{GS} &= V_{EQ} - I_D R_S \\ V_{SB} &= I_D R_S \\ V_{TN} &= V_{TO} + \gamma\left(\sqrt{V_{SB}} + 2\phi_F - \sqrt{2\phi_F}\right) \\ I_D &= \frac{K_n}{2}(V_{GS} - V_{TN})^2 \end{aligned} \tag{4.53}$$

Although it may be possible to solve these equations analytically, it will be more expedient to find the Q-point by iteration using the computer with a spreadsheet, MATLAB®, MATHCAD®, or with a calculator.

Assumptions: Saturation region operation with $I_G = 0$, $I_B = 0$, and $2\phi_F = 0.6\,\text{V}$

Analysis: Using the assumptions and values in Fig. 4.33, Eq. set (4.53) becomes

$$\begin{aligned} V_{GS} &= 6 - 22{,}000 I_D \\ V_{SB} &= 22{,}000 I_D \\ V_{TN} &= 1 + 0.5\left(\sqrt{V_{SB} + 0.6} - \sqrt{0.6}\right) \\ I'_D &= \frac{25 \times 10^{-6}}{2}(V_{GS} - V_{TN})^2 \end{aligned} \tag{4.54}$$

and the drain-source voltage is found from

$$V_{DS} = V_{DD} - I_D(R_D + R_S) = 10 - 40{,}000 I_D \tag{4.55}$$

The expressions in Eq. (4.54) have been arranged in a logical order for an iterative solution:

1. Estimate the value of I_D.
2. Use I_D to calculate the values of V_{GS} and V_{SB}.
3. Calculate the resulting value of V_{TN} using V_{SB}.
4. Calculate I'_D using the results of steps 1 to 3, and compare to the original estimate for I_D.
5. If the calculated value of I'_D is not equal to the original estimate for I_D, then go back to step 1.

In this case, no specific method for choosing the improved estimate for I_D is provided (although the problem could be structured to use Newton's method), but it is easy to converge to the solution after a few trials, using the power of the computer to do the calculations. (Note that the SPICE circuit analysis program can also do the job for us.)

Table 4.3 shows the results of using a spreadsheet to iteratively find the solution to Eqs. (4.54) and (4.55) by trial and error. The first iteration sequence used by the author is shown; it

TABLE 4.3
Four-Resistor Bias Iteration

I_D	$I_D R_S$	V_{GS}	V_{TN}	I'_D	V_{DS}
1.000E-04	2.200	3.800	1.449	6.907E-05	6.000
9.000E-05	1.980	4.020	1.416	8.477E-05	6.400
8.000E-05	1.760	4.240	1.381	1.022E-04	6.800
8.100E-05	1.782	4.218	1.384	1.004E-04	6.760
8.200E-05	1.804	4.196	1.388	9.856E-05	6.720
8.300E-04	1.826	4.174	1.391	9.678E-05	6.680
8.400E-05	1.848	4.152	1.395	9.501E-05	6.640
8.500E-05	1.870	4.130	1.399	9.326E-05	6.600
8.600E-05	1.892	4.108	1.402	9.153E-05	6.560
8.700E-05	1.914	4.086	1.405	8.981E-05	6.520
8.800E-05	1.936	4.064	1.409	8.812E-05	6.480
8.805E-05	1.937	4.063	1.409	8.803E-05	6.478
8.804E-05	1.937	4.063	1.409	8.805E-05	6.478

converges to a drain current of 88.0 μA and drain-source voltage of 6.48 V. Care must be exercised to be sure that the spreadsheet equations are properly formulated to account for all regions of operation. In particular, $I_D = 0$ if $V_{GS} < V_{TN}$.

Check of Results: For this design, we now have

$$V_{DS} = 6.48 \text{ V}, V_{GS} - V_{TN} = 2.56 \text{ V} \qquad \text{and} \qquad V_{DS} > (V_{GS} - V_{TN}) \quad ✔$$

The saturation region assumption is consistent with the solution, and the Q-point is (88.0 μA, 6.48 V).

Discussion: Now that the analysis is complete, we see that the presence of body effect in the circuit has caused the threshold voltage to increase from 1 V to 1.41 V and the drain current to decrease by approximately 12 percent from 100 μA to 88 μA.

EXERCISE: Find the new drain current in the circuit in Fig. 4.32 if $\gamma = 0.75\sqrt{\text{V}}$.

ANSWER: 79.2 μA

DESIGN EXAMPLE 4.6

BIAS REDESIGN TO COMPENSATE FOR BODY EFFECT

The increase in threshold voltage of the MOSFET in Ex. 4.5 due to body effect has caused the drain current to be smaller than the original design value from Ex. 4.4. Let us change the design values for R_S and R_D to restore the Q-point to the original value.

PROBLEM Find the new values of R_S and R_D required to restore the Q-point to the original value of (100 μA, 6 V).

SOLUTION **Known Information and Given Data:** The circuit schematic in Fig. 4.33 with $V_{EQ} = 6$ V, $R_{EQ} = 600$ kΩ, $K_n = 25$ μA/V^2, $V_{TO} = 1$ V, $\gamma = 0.5$ V^{-1}, $I_D = 100$ μA, and $V_{DS} = 6$ V

Unknowns: V_{GS}, V_{BS}, V_{TN}, and region of operation

Approach: We have $I_S = I_D = 100$ μA. To find R_S, we must find the voltage across R_S. From the circuit we have

$$V_{EQ} - V_{GS} - V_S = 0 \qquad \text{or} \qquad V_{SB} = V_{EQ} - V_{GS} \tag{4.56}$$

However, V_{GS} is a function of V_{TN} and V_{TN} depends on V_{SB}.

$$V_{GS} = V_{TN} + \sqrt{\frac{2I_D}{K_n}} \qquad \text{and} \qquad V_{TN} = V_{TO} + \gamma\left(\sqrt{V_{SB} + 2\phi_F} - \sqrt{2\phi_F}\right)$$

We need a simultaneous solution to these equations.

Assumptions: Saturation region operation with $I_G = 0$, $I_B = 0$, and $2\phi_F = 0.6$ V.

Analysis: Since $V_{SB} = V_S$ and $V_{EQ} = 6$ V, the source-bulk voltage given by Eq. (4.56) is

$$V_{SB} = 6 - V_{GS}$$

The value of V_{GS} required to set $I_D = 100\ \mu A$ is

$$V_{GS} = V_{TN} + \sqrt{\frac{2I_D}{K_n}} = V_{TN} + \sqrt{\frac{2(100\ \mu A)}{25\frac{\mu A}{V^2}}} = V_{TN} + 2.83\ V \tag{4.57}$$

Combining Eqs. (4.56) and (4.57) and adding the expression for V_{TN} from Eq. (4.54) gives

$$6 - \left[1 + 0.5\left(\sqrt{V_{SB} + 0.6} - \sqrt{0.6}\right) + 2.83\right] - V_{SB} = 0 \tag{4.58}$$

Rearranging and collecting terms in Eq. (4.50) yields a quadratic equation for V_{SB}:

$$V_{SB}^2 - 5.37V_{SB} + 6.40 = 0 \qquad \text{or} \qquad V_{SB} = 1.79\ V, 3.58\ V$$

The second value of V_{SB} is too large [$(V_{SB} + V_{GS}) = (2.83 + 3.58)$ V which exceeds $V_{EQ} = 6$ V], so $V_{SB} = 1.79$ V is selected as the valid answer. The new values of R_S and R_D required to bias the circuit to the Q-point of (100 μA, 6 V) are

$$R_S = \frac{V_{SB}}{I_D} = \frac{1.79\ V}{100\ \mu A} = 17.9\ k\Omega \qquad \text{and} \qquad R_D = 40\ k\Omega - R_S = 22.1\ k\Omega$$

From Appendix A, the nearest standard 5 percent resistor values are $R_S = 18\ k\Omega$ and $R_D = 22\ k\Omega$.

Check of Results: Here again V_{DS} exceeds $(V_{GS} - V_{TN})$, 6 V > 2.83 V, so the transistor is pinched off as assumed in the design.

Discussion: Including the body effect in the analysis resulted in a 39 percent increase in threshold voltage ($V_{TN} = 1.39$ V) and required a significant change in the values of R_S and R_D to restore the operating point to the desired design value. We need to be aware of and be ready to account for body effect in many circuits.

EXERCISE: Find the new values of R_S and R_D needed to achieve the Q-point of (100 μA, 6 V) in Fig. 4.33 if $\gamma = 0.75\sqrt{V}$.

ANSWERS: 16.3 kΩ, 23.7 kΩ; nearest 5 percent values: 16 kΩ, 24 kΩ ($V_{SB} = 1.63$ V)

EXAMPLE 4.7 TWO-RESISTOR FEEDBACK BIAS

Another example of a feedback bias circuit is given in Fig. 4.34. This circuit requires only two resistors. R_D determines both the drain current and the drain-source voltage of the transistor. Resistor R_G provides a dc connection between the gate and drain, and also serves to isolate the two terminals when signals are applied (as will occur in analog amplifier applications for example).

PROBLEM Find the Q-point (I_D, V_{DS}) for the MOSFET in the two-resistor bias circuit of Fig. 4.34.

SOLUTION **Known Information and Given Data:** The circuit schematic in Fig. 4.34 with $V_{DD} = 3.3$ V, $R_D = 10\ k\Omega$, $R_G = 2\ M\Omega$, $K_n = 260\ \mu A/V^2$, and $V_{TN} = 1$ V

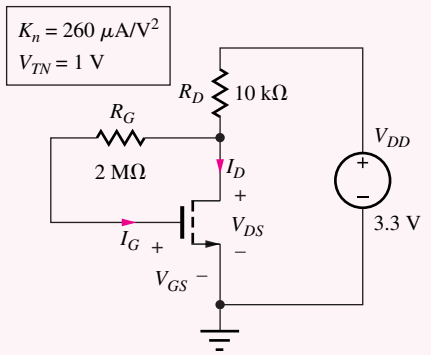


Figure 4.34 Two-resistor bias circuit.

Unknowns: I_D, V_{DS}, and V_{GS}

Assumptions: $I_G = 0, I_B = 0$. Note that the region of operation is actually known. For $I_G = 0$, there is no voltage drop across resistor R_G, and $V_{GS} = V_{DS}$. Since the transistor is an enhancement-mode device ($V_{TN} > 0$) it is pinched-off and in the saturation region — remember the Design Note in Sec. 4.8!

Approach: First find the value of V_{GS}; use V_{GS} to find I_D; use I_D to find V_{DS}.

Analysis: Writing the input loop equation for the value of V_{GS} yields

$$V_{GS} = V_{DS} - I_G R_G \qquad \text{or} \qquad V_{DS} = V_{GS} \text{ since } I_G = 0 \tag{4.59}$$

Next, writing the output loop equation including V_{DS}:

$$V_{DS} = V_{DD} - (I_D + I_G)R_D = V_{DD} - I_D R_D \tag{4.60}$$

Inserting saturation region Eq. (4.30) with $\lambda = 0$ into Eq. (4.60) yields

$$V_{GS} = V_{DD} - \frac{K_n R_D}{2}(\mathrm{V}_{GS} - \mathrm{V}_{TN})^2 \tag{4.61}$$

Substituting the values from the circuit in Fig. 4.28 gives

$$V_{GS} = 3.3 - \frac{(2.6 \times 10^{-4})(10^4)}{2}(\mathrm{V}_{GS} - 1)^2$$

and

$$V_{GS} = -0.769 \text{ V}, +2.00 \text{ V}$$

Since $V_{TN} = 1$ V, $I_D = 0$ for the negative value of V_{GS}, and the answer must be $V_{GS} = 2.00$ V for which

$$I_D = 130\ \mu\text{A} \qquad \text{and} \qquad V_{DS} = 2.00 \text{ V}.$$

Check of Results: Since $V_{DS} = 2.00$ V and $V_{GS} - V_{TN} = 1$ V, the transistor is in the saturation region. The final Q-point is (130 μA, 2.00 V).

Evaluation and Discussion: The two-resistor bias circuit in Fig. 4.34 is another example of a circuit that uses negative feedback to stabilize the operating point. The negative feedback mechanism can be viewed in the following manner. Suppose for some reason that I_D begins to increase. An increase in I_D will cause a decrease in V_{DS} and hence a decrease in V_{GS} since $V_{GS} = V_{DS}$. The decrease in V_{GS} will cause I_D to decrease back toward its original value.

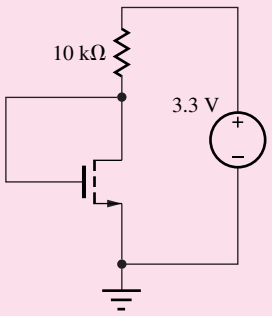
Computer-Aided Analysis: SPICE simulation with the LEVEL = 1 model gives precisely the same Q-point. Be sure to set KP = 2.6×10^{-4} A/V^2 and VTO = 1 V. If we add LAMBDA = 0.02 V^{-1}, the Q-point changes to (131 μA, 1.99 V), negligible shifts.

EXERCISE: Find the Q-point of the NMOS transistor in Fig. 4.34 if $V_{TN} = 1$ V and $K_n = 200\ \mu A/V^2$.

ANSWER: (120 μA, 2.10 V) Note the small change in Q-point caused by the 15 percent change in K_n. This is a result of feedback.

EXERCISE: Find the Q-point of the NMOS transistor in this circuit if $V_{TN} = 1$ V and $K_n = 200\ \mu A/V^2$.

ANSWER: (120 μA, 2.10 V)



EXAMPLE 4.8 ANALYSIS OF AN NMOS TRANSISTOR BIASED IN THE TRIODE REGION

In all the previous circuit examples, we assumed and confirmed that the transistors were operating in the saturation region. But, what if our assumption for the region of operation is wrong? The circuit in Fig. 4.35 provides a simple example of such a circuit.

PROBLEM Determine the Q-point for the NMOSFET in Fig. 4.35.

SOLUTION **Known Information and Given Data:** The circuit schematic in Fig. 4.35 with $V_{DD} = 4$ V, $R_D = 1.6$ kΩ, $K_n = 250\ \mu A/V^2$, and $V_{TN} = 1$ V

Unknowns: I_D, V_{DS}, V_{GS}

Approach: To find the Q-point using the mathematical model for the NMOS transistor, we will find V_{GS}, use it to find I_D and V_{DS} and then see if the resulting Q-point is consistent with the assumed region of operation.

Assumptions: $I_G = 0$ and $I_B = 0$. Assume that the transistor is operating in the saturation region as we have done in the past examples.

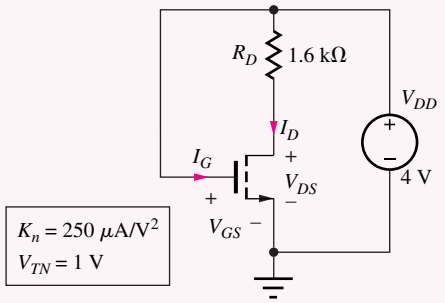


Figure 4.35 Bias circuit for example 4.8.

Analysis: In this circuit we immediately see that $V_{GS} = V_{DD} = 4$ V. Therefore, the MOSFET current is given by

$$I_D = \frac{250}{2}\frac{\mu A}{V^2}(4-1)^2 = 1.13 \text{ mA}$$

Writing the output-loop equation for V_{DS} in terms of I_D gives

$$4 = 1600\ I_D + V_{DS} \tag{4.62}$$

and we find $V_{DS} = 2.19$ V using $I_D = 1.13$ mA.

Assumption Check: We have $V_{DS} = 2.19$ V. However, $V_{GS} - V_{TN} = 4 - 1 = 3$ V. Because $V_{GS} - V_{TN} > V_{DS}$ (3 V > 2.19 V), the assumption of saturation region operation is incorrect, and we must try again.

Analysis — Second Iteration: Substituting the triode region expression into Eq. (4.62) yields

$$4 - V_{DS} = 1600K_n\left(V_{GS} - V_{TN} - \frac{V_{DS}}{2}\right)V_{DS}$$

or

$$4 - V_{DS} = 1600\left(250\frac{\mu A}{V^2}\right)\left(4 - 1 - \frac{V_{DS}}{2}\right)V_{DS} \tag{4.63}$$

After rearrangement we have

$$V_{DS}^2 - 11V_{DS} + 20 = 0$$

Finding the roots of the quadratic equation yields two possibilities:

$$V_{DS} = 8.7 \text{ V}, 2.3 \text{ V}$$

The first voltage, 8.7 V, exceeds the magnitude of the power supply voltage and is not a possible result. So $V_{DS} = 2.3$ V, and

$$I_D = 250\frac{\mu A}{V^2}\left(4 \text{ V} - 1 \text{ V} - \frac{2.3 \text{ V}}{2}\right)(2.3 \text{ V}) = 1.06 \text{ mA}$$

Check of Results: Checking the region of operation:

$$V_{GS} - V_{TN} = 4 \text{ V} - 1\text{V} = 3 \text{ V} \qquad \text{and} \qquad V_{GS} - V_{TN} > V_{DS} \quad \checkmark$$

The triode region is correct and the Q-point is (1.06 mA, 2.3 V).

Evaluation and Discussion: We have now found a Q-point consistent with the assumptions. We can use the value of I_D to double check our answer for V_{DS} from the quadratic equation: $V_{DS} = 4 - 1600I_D = 2.30$ V.

In this case, we found that the circuit is biased in the triode region. However, the two and four resistor bias circuits of the previous examples are most often used to bias the transistor in the saturation region of operation for use as an amplifier.

EXERCISE: Find the values of I_D and V_{DS} in the circuit in Fig. 4.28 if $R_D = 1.8$ MΩ?

ANSWER: (5.49 μA, 0.113 V)

Examples 4.1 through 4.8 of bias circuits represent but a few of the many possible ways to bias an NMOS transistor. Nevertheless, the examples have demonstrated the techniques that we need to analyze most of the circuits we will encounter. The four-resistor and two-resistor bias circuits are most often encountered in discrete design, whereas current mirrors, introduced in Sec. 4.10, find extensive application in integrated circuit design.

4.9 BIASING THE PMOS FIELD-EFFECT TRANSISTOR

CMOS technology, which uses a combination of NMOS and PMOS transistors, is the dominant IC technology in use today, and it is thus very important to know how to bias both types of devices. PMOS bias techniques mirror those used in the previous NMOS bias examples. In the circuits that follow, you will observe that the source of the PMOS transistor will be consistently drawn at the top of the device since the source of the PMOS device is normally connected to a potential that is higher than the drain. This is in contrast to the NMOS transistor in which the drain is connected to a more positive voltage than the source. The PMOS model equations were summarized in Sec. 4.3. Remember that the drain current I_D is positive when coming out of the drain terminal of the PMOS device, and the values of V_{GS} and V_{DS} will be negative.

EXAMPLE 4.9 FOUR-RESISTOR BIAS FOR THE PMOS FET

The four-resistor bias circuit in Fig. 4.36 functions in a manner similar to that used for the NMOS device in Ex. 4.3. In the circuit in Fig. 4.36(a), a single voltage source V_{DD} is used to supply both the gate-bias voltage and the source-drain current. R_1 and R_2 form the gate voltage divider circuit. R_S sets the source/drain current, and R_D determines the source-drain voltage.

PROBLEM Find the quiescent operating point Q-point (I_D, V_{DS}) for the PMOS transistor in the four resistor bias circuit in Fig. 4.36.

SOLUTION **Known Information and Given Data:** Circuit schematic in Fig. 4.36 with $V_{DD} = 10$ V, $R_1 = 1$ MΩ, $R_2 = 1.5$ MΩ, $R_D = 75$ kΩ, $R_S = 39$ kΩ, $K_P = 25$ μA/V^2, $V_{TP} = 1$ V, and $I_G = 0$

Unknowns: I_D, V_{DS}, V_{GS}, and the region of operation

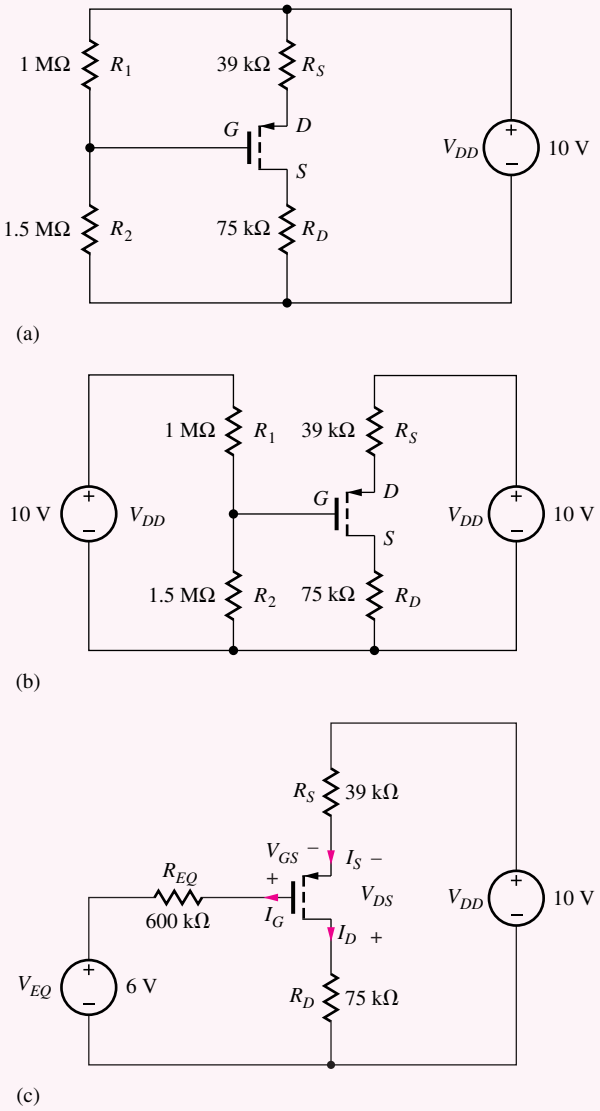


Figure 4.36 Four-resistor bias for a PMOS transistor.

Approach: We can find the Q-point using the mathematical model for the PMOS transistor. We assume a region of operation, determine the Q-point, and check to see if the Q-point is consistent with the assumed region of operation. First find the value of V_{GS}; use V_{GS} to find I_D; use I_D to find V_{DS}.

Assumptions: Assume that the transistor is operating in the saturation region (Once again, remember to use $\lambda = 0$)

$$I_D = \frac{K_p}{2}(V_{GS} - V_{TP})^2 \tag{4.64}$$

Analysis: We begin by simplifying the circuit. In the equivalent circuit in Fig. 4.36(b), the voltage source has been split into two equal-valued sources, and in Fig. 4.36(c), the gate-bias

circuit is replaced by its Thévenin equivalent

$$V_{EQ} = 10\text{ V}\frac{1.5\text{ M}\Omega}{1\text{ M}\Omega + 1.5\text{ M}\Omega} = 6\text{ V} \qquad \text{and} \qquad R_{EQ} = 1\text{ M}\Omega \| 1.5\text{ M}\Omega = 600\text{ k}\Omega$$

Figure 4.36(c) represents the final circuit to be analyzed (be sure to label the variables). Note that this circuit uses the three-terminal representation for the MOSFET, in which it is assumed that the bulk terminal is tied to the source. If the bulk terminal were connected to V_{DD}, the analysis would be similar to that used in Ex. 4.5 because the threshold voltage would then be a function of the voltage developed at the source terminal of the device.

To find I_D, the gate-source voltage must be determined, and we write the input loop equation containing V_{GS}:

$$V_{DD} = I_S R_S - V_{GS} + I_G R_G + V_{EQ} \tag{4.65}$$

Because we know that $I_G = 0$ and therefore $I_S = I_D$, Eq. (4.65) can be reduced to

$$V_{DD} - V_{EQ} = I_D R_S - V_{GS} \tag{4.66}$$

Substituting Eq. (4.64) into Eq. (4.66) yields

$$V_{DD} - V_{EQ} = \frac{K_p R_S}{2}(V_{GS} - V_{TP})^2 - V_{GS} \tag{4.67}$$

and we again have a quadratic equation to solve for V_{GS}. For the values in Fig. 4.36 with $V_{TP} = -1$ V and $K_p = 25\ \mu\text{A/V}^2$,

$$10 - 6 = \frac{(25 \times 10^{-6})(3.9 \times 10^4)}{2}(V_{GS} + 1)^2 - V_{GS}$$

and

$$V_{GS}^2 - 0.051 V_{GS} - 7.21 = 0 \qquad \text{for which } V_{SG} = +2.71\text{ V}, -2.66\text{ V}$$

For $V_{GS} = +2.71$ V, the PMOS FET would be cut off because $V_{GS} > V_{TP}$ $(= -1\text{ V})$. Therefore, $V_{GS} = -2.66$ V must be the answer we seek, and I_D is found using Eq. (4.64):

$$I_D = \frac{25 \times 10^{-6}}{2}(-2.66 + 1)^2 = 34.4\ \mu\text{A}$$

The second part of the Q-point, V_{DS}, can now be determined by writing a loop equation including the source-drain terminals of the device:

$$V_{DD} = I_S R_S - V_{DS} + I_D R_D \qquad \text{or} \qquad V_{DD} = I_D(R_S + R_D) - V_{DS} \tag{4.68}$$

Eq. (4.68) has been simplified since we know that $I_S = I_D$. Substituting the values from the circuit gives

$$10\text{ V} = (34.4\ \mu\text{A})(39\text{ k}\Omega + 75\text{ k}\Omega) - V_{DS} \qquad \text{or} \qquad V_{DS} = -6.08\text{ V}$$

Check of Results: We have

$$V_{DS} = -6.08\text{ V} \qquad \text{and} \qquad V_{GS} - V_{TP} = -2.66\text{ V} + 1\text{ V} = -1.66\text{ V}$$

and $|V_{DS}| > |V_{GS} - V_{TP}|$. Therefore the saturation region assumption is consistent with the resulting Q-point (34.4 μA, −6.08 V) with $V_{GS} = -2.66$ V.

Evaluation and Discussion: As mentioned in Ex. 4.3, the bias circuit in Fig. 4.36 uses negative feedback to stabilize the operating point. Suppose I_D begins to increase. Since V_{EQ} is fixed, an increase in I_D will cause a decrease in the magnitude of V_{GS} [see Eq. (4.66)], and this decrease will tend to restore I_D back to its original value.

EXERCISE: Find the Q-point in the circuit in Fig. 4.36 if R_S is changed to 62 kΩ.

ANSWER: (25.4 μA, −6.52 V)

EXERCISE: (a) Use SPICE to find the Q-point in the circuit in Fig. 4.36. (b) Repeat if R_S is changed to 62 kΩ. (c) Repeat parts (a) and (b) with $\lambda = 0.02$. (*Suggestion:* Insert an ammeter to measure I_D and a voltmeter to measure V_{DS}.)

ANSWERS: (a) (34.4 μA, −6.08 V); (b) (25.4 μA, −6.52 V); (c) (35.9 μA, −5.91 V), (26.3 μA, −6.39 V)

EXAMPLE 4.10 TWO-RESISTOR BIAS FOR THE PMOS TRANSISTOR

The circuit in Fig. 4.37 applies the two-resistor bias technique of Ex. 4.7 to the PMOS transistor. R_D determines both the drain current and the source-drain voltage of the transistor. Resistor R_G provides a dc connection between the gate and drain, and also serves to isolate the two terminals when signals are applied.

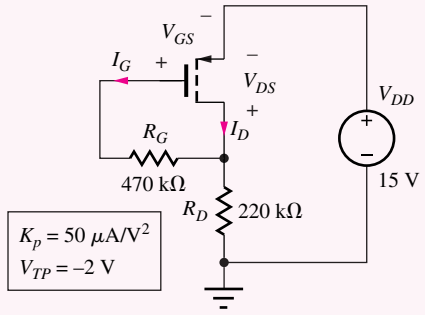


Figure 4.37 Two-resistor bias for a PMOS transistor.

PROBLEM Find the Q-point (I_D, V_{DS}) for the PMOS FET in the two resistor bias circuit of Fig. 4.37.

SOLUTION **Known Information and Given Data:** The circuit schematic in Fig. 4.37 with $V_{DD} = 15$ V, $R_D = 220$ kΩ, $R_G = 470$ kΩ, $K_P = 50$ μA/V^2, and $V_{TP} = -2$ V

Unknowns: I_D, V_{DS}, and V_{GS}

Approach: First find the value of V_{GS}; use V_{GS} to find I_D; use I_D to find V_{DS}.

Assumptions: $I_G = 0$. Note that the region of operation is actually known. For $I_G = 0$, there is no voltage drop across resistor R_G, and $V_{GS} = V_{DS}$. Since the transistor is an enhancement-mode device ($V_{TP} < 0$) , it is automatically operating in the saturation region — remember the Design Note in Sec. 4.8!

Analysis: Writing loop equations for V_{GS} and V_{DS} yields

$$\begin{aligned} V_{GS} + (470\,\text{k}\Omega)I_G + V_{DS} &= 0 \\ 15\,\text{V} + V_{DS} - (220\,\text{k}\Omega)I_D &= 0 \end{aligned} \tag{4.69}$$

Because $I_G = 0$, $V_{DS} = V_{GS}$, and the enhancement-mode transistor is "saturated by connection." Using Eq. (4.35) with $\lambda = 0$ and the transistor parameters from the figure, the second expression in Eq. (4.69) yields

$$15\,\text{V} + V_{GS} - (220\,\text{k}\Omega)\frac{50\,\mu\text{A}}{2\,\text{V}^2}(V_{GS} + 2)^2 = 0$$

and

$$V_{GS} = -0.369\,\text{V}, -3.45\,\text{V}$$

Because $V_{TP} = -2$ V, $V_{GS} = -0.369$ V is not sufficient to turn on the PMOS transistor, so the answer must be $V_{GS} = -3.45$ V, which gives

$$I_D = 52.5\mu\text{A} \qquad \text{and} \qquad V_{DS} = -3.45\,\text{V}$$

Check of Results: Although we know that $V_{DS} = V_{GS}$, let us double check the voltages for practice: $V_{GS} - V_{TP} = -1.45$ V, and so it is true that $|V_{DS}| > |V_{GS} - V_{TP}|$. The assumption of saturation region operation is correct, and the final Q-point is $(I_D, V_{DS}) = (52.5\ \mu\text{A}, -3.45\ \text{V})$.

Evaluation and Discussion: The two-resistor bias circuit in Fig. 4.37 is another example of a circuit that uses negative feedback to stabilize the operating point. The negative feedback mechanism can be viewed in the following manner. Suppose for some reason that I_D begins to increase. An increase in I_D will cause a decrease in the magnitude of V_{DS} and hence a decrease in the size of V_{GS} since $V_{GS} = V_{DS}$. This decrease will cause I_D to decrease back toward its original value.

EXERCISE: Find the Q-point of the PMOS transistor in Fig. 4.37 if $V_{TP} = -1$ V and $K_P = 250\ \mu\text{A/V}^2$.

ANSWER: (60.5 μA, −1.70 V) Note the relatively small shift in I_D for large changes in K_P and V_{TP} — another example of the stabilizing effect of feedback.

EXERCISE: Use SPICE to find the Q-point in the circuit in Fig. 4.37

4.10 CURRENT SOURCES AND THE MOS CURRENT MIRROR

Current sources are widely used to establish transistor operating points in integrated circuits, and an important application of the MOSFET (as well as other electronic devices) is as an electronic current source. The i-v characteristic for an ideal current source is shown in Fig. 4.38, in which an ideal source provides a constant 50-μA output current regardless of the polarity of the voltage across the source.

The output characteristic of an NMOS transistor with a fixed gate-source bias $V_{GS} = 3$ V is also given in Fig. 4.38. If the value of V_{DD} is chosen to be larger than the value needed to pinch off the MOSFET [in this case, $V_{DD} \geq (V_{GS} - V_{TN}) = 3 - 1 = 2$ V], then the FET drain current will also be constant at 50 μA. For $V_{DD} \geq 2$ V, the MOSFET represents an **electronic current source** with a 50-μA output current.

Figure 4.39 shows an NMOS transistor biased with a fixed 3-V dc source. This simple two-terminal MOSFET circuit will behave as an electronic current source as long as the external

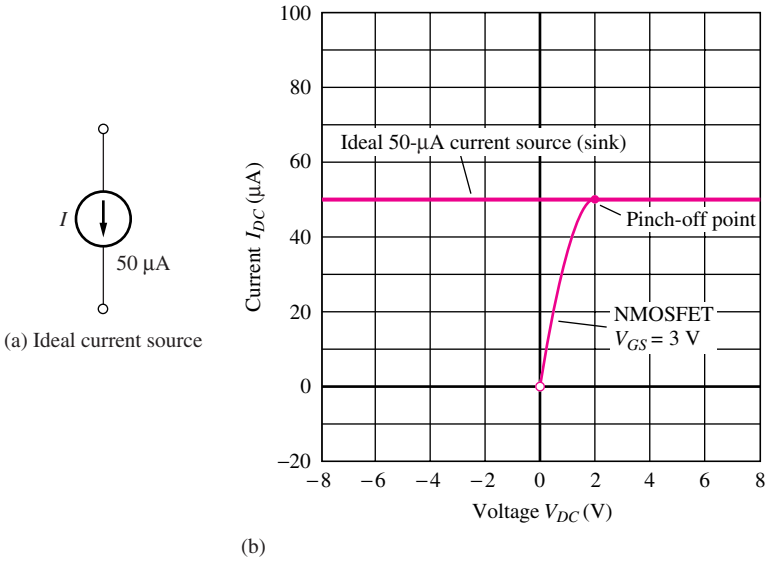


Figure 4.38 Output characteristics for an ideal current source and the MOSFET current source.

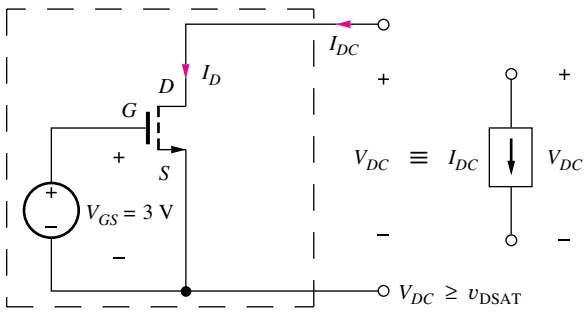


Figure 4.39 NMOS transistor as an electronic current source.

voltage V_{DC} exceeds 2 V. This MOSFET circuit behaves similar to an ideal current source with

$$I_{DC} = I_D = 50\ \mu\text{A}$$

but over a more limited range of terminal voltage. The fixed gate-source bias voltage in Fig. 4.39 could be derived from a larger voltage source V_{GG} using a resistive divider similar to that in Fig. 4.28. However, such a circuit would suffer from the problems associated with fixed gate-source bias described in Ex. 4.1. The clever current mirror circuit to be described below derives the required gate-source bias voltage from a second transistor.

The rectangular current source symbol in Fig. 4.39 will be used in this text to identify the electronic current source and to differentiate it from the ideal **current source,** which will be represented by the standard circular current source symbol in Fig. 4.38(a).

EXERCISE: A current source with $I_{DC} = 25\ \mu$A is needed, and an NMOS transistor is available with $K_n = 25\ \mu\text{A/V}^2$ and $V_{TN} = 1$ V. What is the required value of V_{GS}? What is the minimum value of V_{DS} needed for current source behavior?

ANSWERS: 2.41 V; 1.41 V

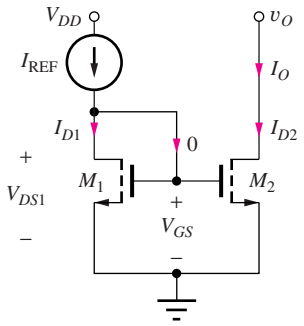


Figure 4.40 NMOS current mirror.

The current mirror circuit represents a fundamental building block in electronic circuit design. Not only is it heavily used in analog applications, but it appears routinely in digital circuit design as well. We will encounter it throughout the text. Figure 4.40 shows the circuit for a basic NMOS current mirror in which MOSFETs M_1 and M_2 are assumed to be *matched devices,* that is, they have identical parameter values (V_{TN}, K_n', λ) and W/L. A reference current I_{REF} provides operating bias to the current mirror, and the output current is represented by current I_O. The basic circuit is designed to have $I_O = I_{REF}$; that is, the output current mirrors the reference current — hence, the name "current mirror." Here the output current I_O originates in an external circuit and goes through transistor M_2 to ground, and circuit source is sometimes referred to as a **current sink** rather than a current source.

4.10.1 DC Analysis of the NMOS Current Mirror

Analysis of the NMOS current mirror begins by recognizing that the gate currents of both MOSFETs are zero. Therefore, reference current I_{REF} must flow into the drain of M_1, which is forced to operate in the saturation region by the circuit connection since $V_{DS1} = V_{GS1} = V_{GS}$. V_{GS} is forced to be equal to the value required for $I_{D1} = I_{REF}$:

$$I_{REF} = \frac{K_n}{2}(V_{GS1} - V_{TN})^2(1 + \lambda V_{DS1}) \tag{4.70}$$

Output current I_O is equal to the dc drain current of M_2,

$$I_O = \frac{K_n}{2}(V_{GS2} - V_{TN})^2(1 + \lambda V_{DS2}) \tag{4.71}$$

but the circuit connection forces $V_{GS2} = V_{GS1}$. Assuming matched devices and substituting $(V_{GS2} - V_{TN})^2$ from Eq. (4.71) into Eq. (4.70) yields

$$I_O = I_{REF} = \frac{(1 + \lambda V_{DS2})}{(1 + \lambda V_{DS1})} \cong I_{REF} \tag{4.72}$$

For equal values of V_{DS}, the output current is identical to the reference current (that is, the output current precisely mirrors the reference current). Unfortunately in most circuit applications, $V_{DS2} \neq V_{DS1}$, and a slight mismatch exists between the output current and the reference current, as demonstrated in Ex. 4.11.

EXAMPLE 4.11 NMOS CURRENT MIRROR ANALYSIS

In this example we will calculate the output current of the current mirror including the effect of mismatch in the drain-source voltages of the transistors.

PROBLEM Calculate the output current for the MOS current mirror in Fig. 4.40 if $\lambda = 0.0133\ \text{V}^{-1}$, $V_O = 12\ \text{V}$, $V_{TN} = 1\ \text{V}$, $K_n = 150\ \mu\text{A/V}^2$, and $I_{\text{REF}} = 50\ \mu\text{A}$.

SOLUTION **Known Information and Given Data:** Current mirror topology in Fig. 4.40, $I_{\text{REF}} = 50\,\mu\text{A}$, $V_O = 12\ \text{V}$, $V_{TN} = 1\ \text{V}$, $K_n = 150\ \mu\text{A/V}^2$, and $\lambda = 0.0133\ \text{V}^{-1}$

Unknowns: V_{GS}, V_{DS1}, I_O

Approach: To evaluate Eq. (4.72), we must find V_{DS1} and V_{DS2}.

Assumptions: The transistors are identical and both are pinched-off.

Analysis: From the circuit we have the value of $V_{DS2} = V_O$, but must find the value of V_{DS1} by rearranging Eq. (4.70).

$$V_{DS1} = V_{GS1} = V_{TN} + \sqrt{\frac{2I_{\text{REF}}}{K_n(1 + \lambda V_{DS1})}}$$

If we try to simplify this equation, we unfortunately end up with a cubic expression. Therefore it is more expedient to use our calculator's built-in solver or to use "trial-and-error" to find V_{DS1} from

$$V_{DS1} = 1\ \text{V} + \sqrt{\frac{2(50\ \mu\text{A})}{150\dfrac{\mu\text{A}}{\text{V}^2}\left(1 + \dfrac{0.0133}{\text{V}}V_{DS1}\right)}}$$

The result is $V_{DS1} = 1.81\ \text{V}$. Substituting this value and $V_{DS2} = 12\ \text{V}$ in Eq. (4.72) yields:

$$I_O = (50\ \mu\text{A})\frac{\left(1 + \dfrac{0.0133}{\text{V}}(12\ \text{V})\right)}{\left(1 + \dfrac{0.0133}{\text{V}}(1.81\ \text{V})\right)} = 56.6\ \mu\text{A}$$

Check of Results: M_1 is saturated by connection. For M_2, $V_{GS2} - V_{TN} = 0.81\ \text{V}$ and $V_{DS2} = 12\ \text{V}$. Therefore, M_2 is also pinched-off. The output current is similar to the input current so our calculations appear correct.

Discussion: The ideal output current for the current mirror would be 50 μA. However, the actual currents are mismatched by approximately 13 percent due to the nonzero value of λ and the differing values of the drain-source voltages. The current mirror is an extremely important circuit configuration in integrated circuit design. The flexibility of the circuit is greatly increased by the ability to change the mirror ratio as described in the next section, and techniques for minimizing errors in the mirror ratio are discussed in detail in Chapter 16.

Computer Aided Analysis: Simulation of the circuit in Ex. 4.11 confirms our hand calculations.

EXERCISE: Based on the numbers in Ex. 4.11, what is the minimum value of the drain voltage required to maintain M_2 pinched-off in Fig. 4.40? What is the output current for this value of V_O? What is the value of I_O for $V_O = 5$ V?

ANSWERS: 0.810 V; 49.4 μA; 52.1 μA

EXERCISE: What is the output current in Ex. 4.11 if $V_O = 10$ V?

ANSWER: 55.3 μA

EXERCISE: What will be the new values of V_{DS1} and the output current in Ex. 4.11 if $\lambda = 0.02/\text{V}$?

ANSWER: 1.80 V, 59.8 μA

EXERCISE: What will be the new values of V_{DS1} and output current in Ex. 4.11 if $I_{\text{REF}} = 100$ μA?

ANSWER: 2.14 V, 113 μA

4.10.2 CHANGING THE MOS MIRROR RATIO

The utility of the current mirror is greatly increased if the **mirror ratio** can be changed from unity. For the MOS current mirror, the ratio can easily be modified by changing the W/L ratios of the two transistors forming the mirror. In Fig. 4.41 for example, M_2 has five times the width of M_1, and, as we will often see, the circuit is operating from a single negative power supply.

Remembering that $K_n = K_n'(W/L)$ for the MOSFET, the K_n values for the two transistors are given by

$$K_{n1} = K_n' \left(\frac{W}{L}\right)_1 = 2K_n' \qquad \text{and} \qquad K_{n2} = K_n' \left(\frac{W}{L}\right)_2 = 10K_n' \tag{4.73}$$

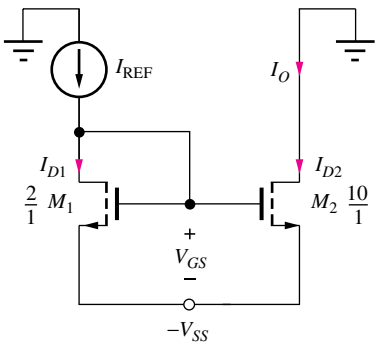


Figure 4.41 MOS current mirror with unequal (W/L) ratios.

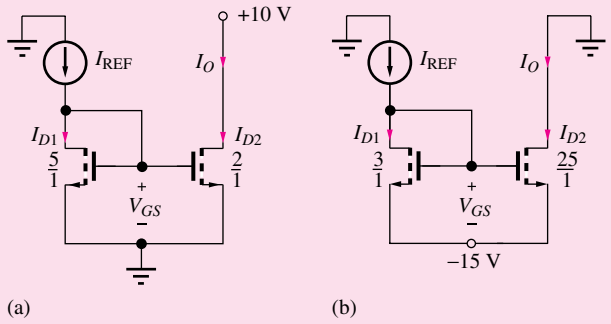
Substituting these two different values of K_n in Eqs. (4.70) and (4.71) yields

$$I_O = I_{\text{REF}} \frac{(W/L)_2}{(W/L)_1} \frac{(1 + \lambda V_{DS2})}{(1 + \lambda V_{DS1})} = 5I_{\text{REF}} \frac{(1 + \lambda V_{DS2})}{1 + \lambda V_{DS1}} \tag{4.74}$$

For the particular values in Fig. 4.41, the nominal output current is $I_O = 5I_{\text{REF}}$, ignoring the differences due to drain-source voltage mismatch. However, any difference in the two values of V_{DS} will again create a deviation from the ideal mirror ratio.

Note again the use of the negative power supply in Fig. 4.41(b). Operating the current source between ground and a negative supply is quite common, particularly in amplifier design. Circuit operation is the same; the supply voltages are just shifted.

EXERCISE: (a) Calculate the mirror ratio I_O/I_{REF} for the MOS current mirrors in the figure for $\lambda = 0$. (b) For $\lambda = 0.02\ \text{V}^{-1}$ if $V_{TN} = 1$ V, $K_n' = 25\ \mu\text{A/V}^2$, and $I_{\text{REF}} = 50\ \mu\text{A}$?



ANSWERS: 0.400, 8.33; 0.462, 10.4

4.10.3 Output Resistance of the Current Mirror

The output current of an ideal current source is totally independent of the voltage appearing across the source terminals. However, our current mirror represents an electronic approximation of the ideal current source, and its output current is not completely independent of the terminal voltage across the source. First of all, we know that there must be sufficient voltage across the output transistor to keep the device pinched off, but even in the active region, there will be small changes in output current as v_{DS} varies since a real transistor has a nonzero value for λ.

Now let us investigate the behavior of the circuit for small changes in v_O. The output current of the source will vary directly with v_{DS}. Thus the current source appears to have a resistive component associated with it. This resistance is called the **output resistance** R_o of the source and can be defined as

$$R_o = \left(\frac{\partial i_O}{\partial v_O} \bigg|_{\text{Q-pt}} \right)^{-1} \tag{4.75}$$

The current mirror output current i_O is given by Eq. (4.71) with $v_{DS2} = v_O$

$$i_O = \frac{K_n}{2} (v_{GS} - V_{TN})^2 (1 + \lambda v_O) \tag{4.76}$$

and taking the derivative of this expression as defined in Eq. (4.75):

$$\left.\frac{\partial i_O}{\partial v_O}\right|_{\text{Q-pt}} = \lambda\frac{K_n}{2}(V_{GS} - V_{TN})^2$$

Using Eq. (4.76), we observe that

$$\frac{K_n}{2}(V_{GS} - V_{TN})^2 = \frac{I_O}{1 + \lambda V_O}$$

so that R_o can be written as

$$R_o = \left(\lambda\frac{I_O}{1 + \lambda V_O}\right)^{-1} = \frac{1 + \lambda V_O}{\lambda I_O} \cong \frac{1}{\lambda I_O} \tag{4.77}$$

Using Eq. (4.77), the output resistance of the current source in Ex. 4.11 would be

$$R_o = \frac{1 + 0.0133(12)}{0.0133(56.6)}\frac{\text{V}}{\mu\text{A}} = 1.54\ \text{M}\Omega$$

which is a reasonably high value, but far from the infinite value associated with an ideal current source. The value of R_o calculated using Eqs. (4.75) to (4.77) is valid only for small changes in current near the Q-point. For this reason, R_o is called the **small-signal output resistance** of this circuit. We explore small-signal modeling of circuits in great detail in Part III.

Note that λ and the Q-point current determine R_o. We will find that λ is very important in setting the output resistance of most MOS circuits.

EXERCISE: Calculate the output resistance for the two current mirrors in the (b) part of the exercise at the end of 4.10.2.

ANSWERS: 3 MΩ, 125 kΩ

4.10.4 CURRENT MIRROR LAYOUT

Design of the circuit topology, choice of the W/L ratios, and final layout of the circuit are important parts of the IC designer's job. Figure 4.42(a) presents one possible layout of a simple current mirror designed for $I_O = 1.5I_{\text{REF}}$ based on the ground rules from Sec. 4.5. Two transistors are drawn with a common gate electrode that is also connected by the aluminum level to the drain of the first transistor. Reference current I_{REF} would be injected into this node. The two source regions are connected together, and output current I_O is taken from the drain of the second transistor. The W/L ratio of M_2 is 1.5 times that of reference transistor M_1:

$$\left(\frac{W}{L}\right)_1 = \frac{5\ \mu\text{m}}{1\ \mu\text{m}} = \frac{5}{1} \qquad \text{and} \qquad \left(\frac{W}{L}\right)_2 = \frac{7.5\ \mu\text{m}}{1\ \mu\text{m}} = \frac{7.5}{1}$$

In Fig. 4.42(b) the source regions have been merged together. Note that transistor matching may not be as good as in Fig. 4.42(a) because the effective number of source contacts/unit length is different for the reference and output transistors.

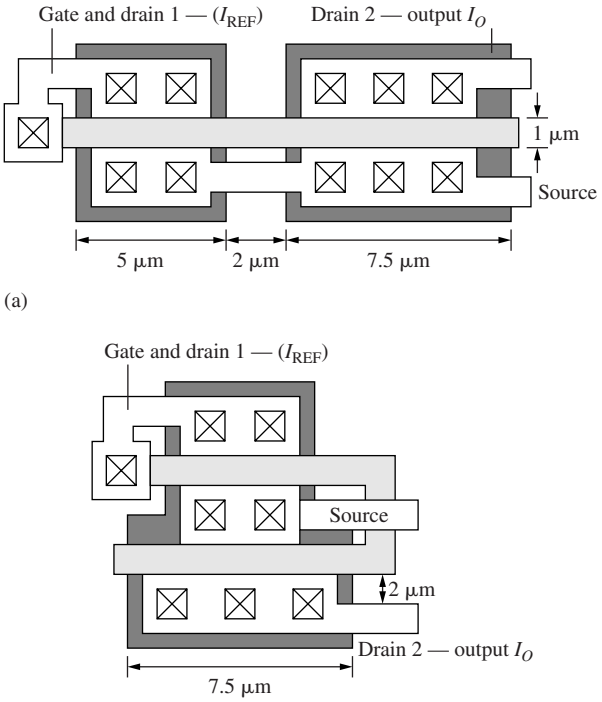


Figure 4.42 (a) Layout for NMOS current mirror with 1.5:1 mirror ratio. (b) Alternate layout with merged source regions.

4.10.5 Multiple Current Mirrors

A typical application encountered in circuit design is the need for multiple current sources and/or sinks to provide bias current to various segments of a more complex circuit. Multiple currents can be generated using a compound current mirror similar to that in Fig. 4.43(a). In this particular case, three different currents are generated from one reference current, and both the NMOS and PMOS current mirrors operate from the same reference current. The line drawn through the gate of transistor M_2 indicates a common connection of the three gate terminals of transistors M_1, M_2, and M_3.

The same reference current I_{REF} appears in both reference transistor M_4 of the upper PMOS current mirror and reference transistor M_1 of the lower NMOS current mirrors. Voltage V_{GSN} appears across the gate-source terminals of M_1, M_2, and M_3 and so the drain currents of transistors M_2 and M_3 are scaled replicas of the reference current in M_1. To understand the basic design, let us assume $\lambda = 0$:

$$I_{D2} = I_{REF}\frac{(W/L)_2}{(W/L)_1} = 25\ \mu A\frac{10/1}{5/1} = 50\ \mu A$$

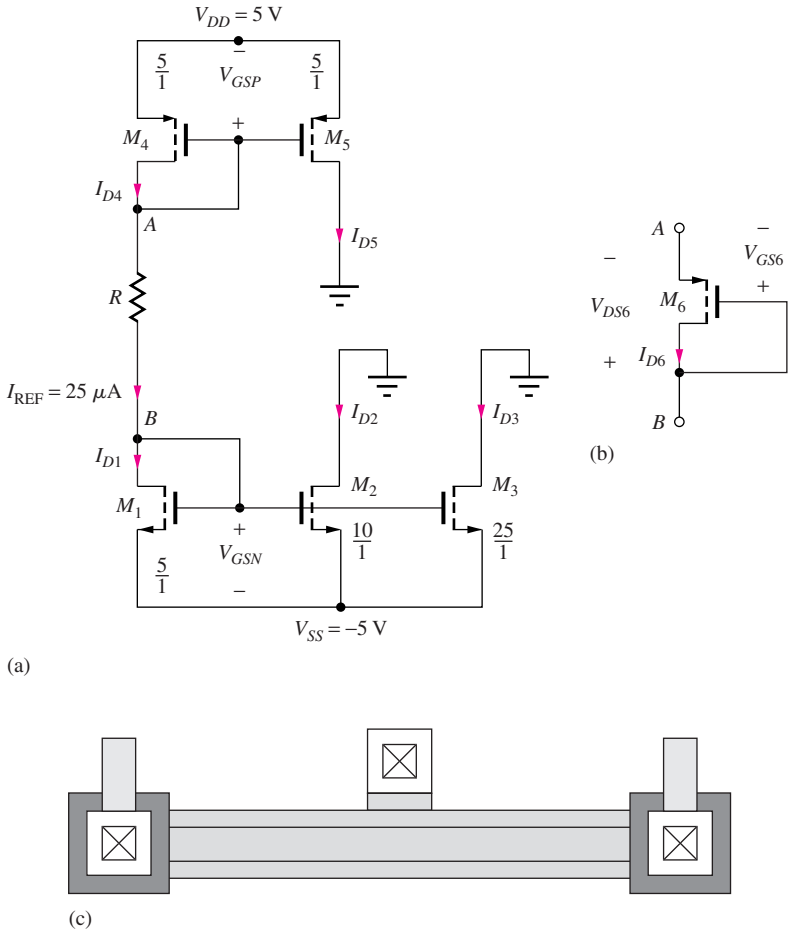


Figure 4.43 (a) Multiple currents sources generated from one reference current. For this circuit, $K_n' = 25\ \mu A/V^2$, $K_p' = 10\ \mu A/V^2$, $V_{TN} = +1$ V, $V_{TP} = -1$ V. (b) Resistor replacement, and (c) layout of a 1/13.6 device.

and

$$I_{D3} = I_{REF}\frac{(W/L)_3}{(W/L)_1} = 25\ \mu A\frac{25/1}{5/1} = 125\ \mu A$$

Similarly, voltage V_{GSP} appears across the gate-source terminals of M_4 and M_5, and therefore the drain current of transistor M_5 is a scaled replica of the reference current in M_4:

$$I_{D5} = I_{REF}\frac{(W/L)_5}{(W/L)_4} = 25\ \mu A\frac{5/1}{5/1} = 25\ \mu A$$

Let us choose the value of resistor R to set the reference current to 25 μA:

$$R = \frac{10 + V_{GSP} - V_{GSN}}{I_{REF}} \tag{4.78}$$

V_{GSP} and V_{GSN} are determined from the drain current expressions for saturated PMOS and NMOS devices:

$$V_{GSP} = V_{TP} - \sqrt{\frac{2I_D}{K_p}} = (-1\text{ V}) - \sqrt{\frac{2(25\ \mu\text{A})}{\left(20\frac{\mu\text{A}}{\text{V}^2}\right)\left(\frac{5}{1}\right)}} = -1.71\text{ V}$$

and

$$V_{GSN} = V_{TN} + \sqrt{\frac{2I_D}{K_n}} = 1\text{ V} + \sqrt{\frac{2(25\ \mu\text{A})}{\left(50\frac{\mu\text{A}}{V^2}\right)\left(\frac{5}{1}\right)}} = 1.45\text{ V} \tag{4.79}$$

Substituting these values into Eq. (4.78) gives the value of R:

$$R = \frac{10 - 1.71 - 1.45}{25}\frac{\text{V}}{\mu\text{A}} = \frac{6.84\text{ V}}{25\ \mu\text{A}} = 274\text{ k}\Omega$$

This value for R could be realized by a discrete resistor. For example, 270 kΩ represents a standard 5 percent resistor value from the resistor table in Appendix A. However, this value is too large to be easily realized in integrated circuit form, a problem that is discussed in more detail at the end of Sec. 6.6.

A better solution in an integrated circuit is to replace resistor R with an additional transistor M_6 as indicated in Fig. 4.43(b). Let us use a PMOS device (a PMOS device will require less area than an NMOS device because of its lower mobility). To replace the resistor, the transistor is connected as a two-terminal device with its gate connected to its drain and inserted in place of the resistor between terminals A and B in the circuit.

In this case, we need to complete the design by finding the W/L ratio of the transistor. We know that the source-gate voltage across the transistor is $V_{GS} = -6.84$ V and the drain current must be 25 μA. Remember also that the transistor is "saturated by connection" since it is an enhancement-mode transistor! Therefore,

$$I_D = \frac{K_p'}{2}\left(\frac{W}{L}\right)(V_{GS} - V_{TP})^2$$

$$25 \times 10^{-6} = \frac{20 \times 10^{-6}}{2}\left(\frac{W}{L}\right)(-6.84 + 1)^2 \rightarrow \left(\frac{W}{L}\right) = \frac{1}{13.6}$$

A PMOS transistor with a W/L ratio of $1/13.6$ will set the reference current to 25 μA. Note that this result design differs from those of the transistors that we have encountered thus far since the length of M_6 is larger than its width. However, this is not a problem; we can design such a device with little difficulty [see Fig. 4.43(c)].

EXERCISE: Suppose an NMOS transistor were used to set the reference current in the example above instead of the PMOS transistor. What would be the W/L ratio of the NMOS device? Does it indeed require more area?

ANSWER: 1/34.1; $(W \times L)_N = 34.1$, which is much greater than $(W \times L)_P = 13.6$

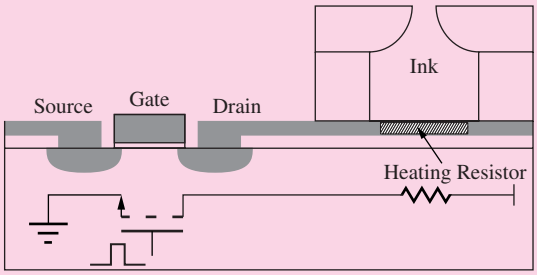
EXERCISE: What are the three drain currents in the circuit in Fig. 4.43(a) if $\lambda = 0.015\ V^{-1}$ for both transistors. What are the output resistances of the three current sources?

ANSWERS: 26.9 μA, 53.8 μA; 134 μA; 2.67 MΩ, 1.33 MΩ, 533 kΩ.

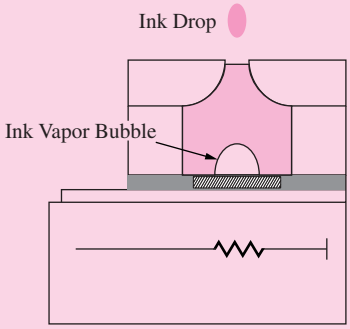
ELECTRONICS IN ACTION

Thermal Inkjet Printers

Inkjet printers have moved from a few niche applications in the 1960s to a widespread, mainstream consumer presence. Thermal inkjet technology was invented in 1979 at Hewlett-Packard Laboratories. Since that time, inkjet technology has evolved to the point where modern thermal inkjet printers deliver 10–20 picoliter droplets at rates of several KHz. Integration of the ink handling structures with microelectronics has been an important component of this evolution. Early versions of thermal inkjet printers had drive electronics that were separate from the ink delivery devices. Through the use of MEMS (micro-electro-mechanical system) technology, it has been possible to combine MOS transistors onto the same substrate with the ink handling structures.

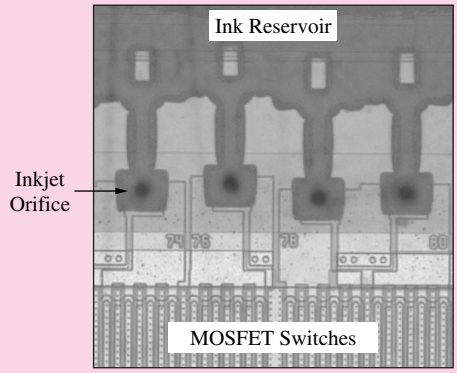


Simplified diagram of thermal inkjet structure integrated with MOS drive transistors. Voltage pulse on the gate causes I^2R heating in the resistor.



Heat from power dissipated in the resistor vaporizes a small amount of ink causing the ejection of an ink droplet out of the nozzle.

Thermal inkjet printer from the Hewlett-Packard Company.



Photomicrograph of inkjet print head

This diagram is a simplified illustration of a merged thermal inkjet system. A MOSFET transistor is located in the left segment of the silicon substrate. A metal layer connects the drain of the transistor to the thin-film resistive heating material directly under the ink cavity. When the gate of the transistor is driven with a voltage pulse, current passes through the resistor leading to a rapid heating of the ink in the cavity. The temperature of the ink in contact with the resistor increases until a small portion of the ink vaporizes. The vapor bubble forces an ink drop to be ejected from the nozzle at the top of the ink cavity and onto the paper. (In practice, the drops are directed down onto the paper.) At the end of the gate drive pulse, the resistor cools and the vapor bubble collapses, allowing more ink to be drawn into the cavity from an ink reservoir.

Due to the high densities and resolutions made possible by the merging of control and drive electronics with the printing structures, inkjet printers are now capable of generating photo-quality images at reasonable costs. As we will see throughout this text, making high-technology affordable and widely available is a common trait of microelectronics-based systems.

4.11 MOS TRANSISTOR SCALING (ADVANCED TOPICS)

In Chapter 1, we discussed the phenomenal increase in integrated circuit density and complexity. These changes have been driven by our ability to aggressively scale the physical dimensions of the MOS transistor. A theoretical framework for MOSFET miniaturization was first provided by Dennard, Gaensslen, Kuhn, and Yu [6, 7]. The basic tenant of the theory is to require that the electrical fields be maintained constant within the device as the geometry is changed. Thus, if a physical dimension is reduced by a factor of α, then the voltage applied across that dimension must also be decreased by the same factor.

4.11.1 Drain Current

These rules are applied to the transconductance parameter and triode region drain current expressions for the MOSFET in Eq. (4.80) in which the three physical dimensions, W, L, and T_{ox} are all reduced by the factor α, and each of the voltages including the threshold voltage is reduced by the same factor.

$$\begin{aligned} K_n^* &= \mu_n \frac{\varepsilon_{ox}}{T_{ox}/\alpha} \frac{W/\alpha}{L/\alpha} = \alpha \mu_n \frac{\varepsilon_{ox}}{T_{ox}} \frac{W}{L} = \alpha K_n \\ i_D^* &= \mu_n \frac{\varepsilon_{ox}}{T_{ox}/\alpha} \frac{W/\alpha}{L/\alpha} \left(\frac{v_{GS}}{\alpha} - \frac{V_{TN}}{\alpha} - \frac{v_{DS}}{2\alpha} \right) \frac{v_{DS}}{\alpha} = \frac{i_D}{\alpha} \end{aligned} \tag{4.80}$$

We see that scaled transconductance K_n^* is increased by the scale factor α, whereas the scaled drain current is reduced from the original value by the scale factor.

4.11.2 Gate Capacitance

In a similar manner, the total gate-channel capacitance of the device is also found to be reduced by α:

$$C_{GC}^* = (C_{ox}'')^* W^* L^* = \frac{\varepsilon_{ox}}{T_{ox}/\alpha} \frac{W/\alpha}{L/\alpha} = \frac{C_{GC}}{\alpha} \tag{4.81}$$

In Chapter 6 we will demonstrate that the delay of logic gates is limited by the transistor's ability to charge and discharge the capacitance associated with the circuit. Based on $i = C\,dv/dt$, an estimate of the delay of a scaled logic circuit is

$$\tau^* = C^*_{GC}\frac{\Delta V^*}{i^*_D} = \frac{C_{GC}}{\alpha}\frac{\Delta V/\alpha}{i_D/\alpha} = \frac{\tau}{\alpha} \tag{4.82}$$

We find that circuit delay is also improved by the scale factor α.

4.11.3 Circuit and Power Densities

As we scale down the dimensions by α, the number of circuits in a given area will increase by a factor of α^2. An important concern in scaling is therefore what happens to the power per circuit, and hence the power per unit area (power density) as dimensions are reduced. The total power supplied to a transistor circuit will be equal to the product of the supply voltage and the transistor drain current:

$$P^* = V^*_{DD}i^*_D = \left(\frac{V_{DD}}{\alpha}\right)\left(\frac{i_D}{\alpha}\right) = \frac{P}{\alpha^2}$$

and

$$\frac{P^*}{A^*} = \frac{P^*}{W^*L^*} = \frac{P/\alpha^2}{(W/\alpha)(L/\alpha)} = \frac{P}{WL} = \frac{P}{A} \tag{4.83}$$

The result in Eq. (4.83) is extremely important. It indicates that the power per unit area remains constant if a technology is properly scaled. Even though we are increasing the number of circuits by α^2, the total power for a given size integrated circuit die will remain constant. Violation of the **scaling theory** over many years, by maintaining a constant 5-V power supply as dimensions were reduced, led to almost unmanagable power levels in many of today's integrated circuits. The power problem was finally resolved by changing from NMOS to CMOS technology, and then by reducing the power supply voltages.

4.11.4 Power-Delay Product

A useful figure of merit for comparing logic families is the **power-delay product** (PDP), which is discussed in more detail in Chapters 6 to 9. The product of power and delay time represents energy, and the power-delay product represents a measure of the energy required to perform a simple logic operation.

$$\text{PDP}^* = P^*\tau^* = \frac{P}{\alpha^2}\frac{\tau}{\alpha} = \frac{\text{PDP}}{\alpha^3} \tag{4.84}$$

The PDP figure of merit shows the full power of technology scaling. The power-delay product is reduced by the cube of the scaling factor.

Each new generation of lithography technology corresponds to a scale factor $\alpha = \sqrt{2}$. Therefore each new technology generation increases the potential number of circuits per chip by a factor of 2 and improves the PDP by a factor of almost 3. Table 4.4 summarizes the performance changes achieved with **constant electric field scaling.**

TABLE 4.4
Constant Electric Field Scaling Results

PERFORMANCE MEASURE	SCALE FACTOR
Area/circuit	$1/\alpha^2$
Transconductance parameter	α
Current	$1/\alpha$
Capacitance	$1/\alpha$
Circuit delay	$1/\alpha$
Power/circuit	$1/\alpha^2$
Power/unit area (power density)	1
Power-delay product (PDP)	$1/\alpha^3$

EXERCISE: A MOS technology is scaled from a 1-μm feature size to 0.25 μm. What is the increase in the number of circuits/cm^2? What is the improvement in the power-delay product?

ANSWERS: 16 times; 64 times

EXERCISE: Suppose that the voltages are not scaled as the dimensions are reduced by a factor of α? How does the drain current of the transistor change? How do the power/circuit and power density scale?

ANSWERS: $I_D^* = \alpha I_D$; $P^* = \alpha P$; $P^*/A^* = \alpha^3 P$!!

4.11.5 CUTOFF FREQUENCY

The ratio of transconductance g_m to gate-channel capacitance C_{GC} represents the highest useful frequency of operation of the transistor, and this ratio is called the cutoff frequency f_T of the device. The cutoff frequency represents the highest frequency at which the transistor can provide amplification. We can find f_T for the MOSFET by combining Eqs. (4.23) and (4.37):

$$f_T = \frac{1}{2\pi}\frac{g_m}{C_{GC}} = \frac{1}{2\pi}\frac{\mu_n}{L^2}(V_{GS} - V_{TN}) \tag{4.85}$$

Here we see clearly the advantage of scaling the channel length of MOSFET. The cutoff frequency improves with the square of the reduction in channel length.

EXERCISE: (a) A MOSFET has a mobility of 500 cm^2/V · s and channel length of 1 μm. What is its cutoff frequency if the gate voltage exceeds the threshold voltage by 1 V? (b) Repeat for a channel length of 0.25 μm.

ANSWERS: (a) 7.96 GHz; (b) 12.7 GHz

4.11.6 High Field Limitations

Unfortunately the assumptions underlying constant-field scaling have often been violated due to a number of factors. For many years, the supply voltage was maintained constant at a standard level of 5 V, while the dimensions of the transistor were reduced, thus increasing the electric fields within the MOSFET. Increasing the electric field in the device can reduce long-term reliability and ultimately lead to breakdown of the gate oxide or *pn* junction.

High fields directly affect MOS transistor mobility in two ways. The first effect is a reduction in the mobility of the MOS transistor due to increasing carrier scattering at the channel oxide interface. The second effect of high electric fields is to cause a breakdown of the linear mobility-field relationship as discussed in Chapter 2. At low fields, carrier velocity is directly proportional to electric field, as assumed in Eq. (4.5), but for fields exceeding approximately 10^4 V/cm, the carriers reach a maximum velocity of approximately 10^7 cm/s called the saturation velocity v_{SAT} (see Fig. 2.5). Both mobility reduction and velocity saturation tend to linearize the drain current expressions for the MOSFET. The results of these effects can be incorporated into the drain current model for the MOSFET as indicated in Eqs. (4.86) through (4.88) in which the expression for carrier velocity is replaced with the maximum velocity limit v_{SAT}:

$$i_D = Q_n v_n = \frac{C''_{\text{ox}} W}{2}(v_{GS} - V_{TN})v_n \tag{4.86}$$

$$v_n = \mu_n \frac{v_{DS}}{L} \rightarrow v_{\text{SAT}} \tag{4.87}$$

This modification causes the square-law behavior to disappear from the saturation region equation:

$$\text{Saturation region:} \qquad i_D = \frac{C''_{\text{ox}} W}{2}(v_{GS} - V_{TN})v_{\text{SAT}} \tag{4.88}$$

Exercise: A MOSFET has a channel length of 1 μm. What value of V_{DS} will cause the electrons to reach saturation velocity? Repeat for a channel length of 0.1 μm.

Answers: 10 V, 1 V

4.11.7 Subthreshold Conduction

In our discussion of the MOSFET thus far, we have assumed that the transistor turns off abruptly as the gate-source voltage drops below the threshold voltage. In reality, this is not the case. As depicted in Fig. 4.44, the drain current decreases exponentially for values of V_{GS} less than V_{TN} (referred to as the **subthreshold region**), as indicated by the region of constant slope in the graph. A measure of the rate of turn off of the MOSFET in the subthreshold region is specified as the reciprocal of the slope $(1/S)$ in mV/decade of current change. Typical values range from 60 to 120 mV/decade. The value depends on the relative magnitudes of C''_{ox} and C_d in Fig. 4.3(b).

From Eq. (4.80), we see that the threshold voltage of the transistor should be reduced as the dimensions are reduced. However, the subthreshold region does not scale properly, and the curve in Fig. 4.44 tends to shift horizontally as V_{TN} is decreased. The reduced threshold increases the leakage current in "off" devices, which ultimately limits data storage time in the dynamic memory cells (see Chapter 8) and can play an important role in limiting battery life in low-power portable devices.

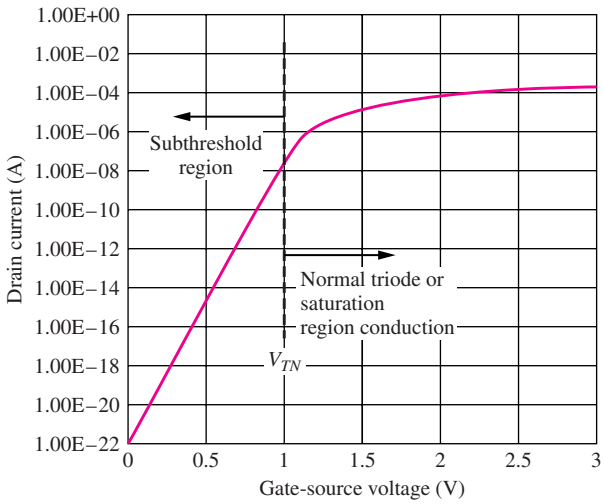


Figure 4.44 Subthreshold conduction in an NMOS transistor with $V_{TN} = 1$ V.

EXERCISE: (a) What is the leakage current in the device in Fig. 4.44 for $V_{GS} = 0.25$ V? (b) Suppose the transistor in Fig. 4.44 had $V_{TN} = 0.5$ V. What will be the leakage current for $V_{GS} = 0$ V? (c) A memory chip uses 10^9 of the transistors in part (b). What is the total leakage current if $V_{GS} = 0$ V for all the transistors?

ANSWERS: (a) $\cong 10^{-18}$ A; (b) $\cong 10^{-15}$ A; (c) $\cong 1$ μA

4.12 THE JUNCTION FIELD-EFFECT TRANSISTOR (JFET) (ADVANCED TOPIC)

Another type of field-effect transistor can be formed without the need for an insulating oxide by using *pn* junctions, as illustrated in Fig. 4.45. This device, the **junction field-effect transistor,** or **JFET,** consists of an *n*-type block of semiconductor material and two *pn* junctions that form the gate. Although less prevalent than MOSFETs, JFETs have many applications in both integrated and discrete circuit design, particularly in analog and RF and applications. In integrated circuits, JFETs are most often found in BiFET processes, which combine bipolar transistors with JFETs. The JFET provides a device with much lower input current and much higher input impedance than that typically achieved with the bipolar transistor.

In the ***n*-channel JFET,** current again enters the channel region at the drain and exits from the source. The resistance of the channel region is controlled by changing the physical width of the channel through modulation of the depletion layers that surround the *pn* junctions between the gate and the channel (see Sec. 3.1 and 3.6). In its triode region, the JFET can be thought of as simply a voltage-controlled resistor with its channel resistance determined by

$$R_{CH} = \frac{\rho}{t}\frac{L}{W} \tag{4.89}$$

where ρ = resistivity of the channel region

L = channel length

W = width of channel between the *pn* junction depletions regions

t = depth of channel into the page

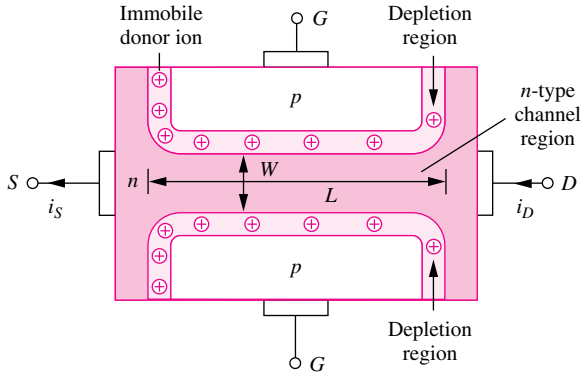


Figure 4.45 Basic n-channel JFET structure and important dimensions. (Note that for clarity the depletion layer in the p-type material is not indicated in the figure.)

When a voltage is applied between the drain and source, the channel resistance determines the current.

With no bias applied, as in Fig. 4.45, a resistive channel region exists connecting the drain and source. Application of a reverse bias to the gate-channel diodes will cause the depletion layers to widen, reducing the channel width and decreasing the current. Thus, the JFET is inherently a depletion-mode device — a voltage must be applied to the gate to turn the device off.

The JFET in Fig. 4.45 is drawn assuming one-sided step junctions ($N_A \gg N_D$) between the gate and channel in which the depletion layers extend only into the channel region of the device (see Sec. 3.1 and 3.6). Note how an understanding of the physics of the pn junction is used to create the JFET.

4.12.1 The JFET with Bias Applied

Figure 4.46(a) shows a JFET with 0 V on the drain and source and with the gate voltage $v_{GS} = 0$. The channel width is W. During normal operation, a reverse bias must be maintained across the pn junctions to provide isolation between the gate and channel. This reverse bias requires $v_{GS} \leq 0$ V.

In Fig. 4.46(b), v_{GS} has decreased to a negative value, and the depletion layers have increased in width. The width of the channel has now decreased, with $W' < W$, increasing the resistance of the channel region; see Eq. (4.89). Because the gate-source junction is reverse-biased, the gate current will equal the reverse saturation current of the pn junction, normally a very small value, and we will assume that $i_G \cong 0$.

For more negative values of v_{GS}, the channel width continues to decrease, increasing the resistance of the channel region. Finally, the condition in Fig. 4.46(c) is reached for $v_{GS} = V_P$, the pinch-off voltage; V_P is the (negative) value of gate-source voltage for which the conducting channel region completely disappears. The channel becomes pinched-off as the depletion regions from the two pn junctions merge at the center of the channel. At this point, the resistance of the channel region has become infinitely large. Further increases in v_{GS} do not substantially affect the internal appearance of the device in Fig. 4.47(c). However, v_{GS} must not exceed the reverse breakdown voltage of the gate-channel junction.

4.12.2 JFET Channel with Drain-Source Bias

Figures 4.47(a) to 4.47(c) show conditions in the JFET for increasing values of drain-source voltage v_{DS} and a fixed value of v_{GS}. For a small value of v_{DS}, as in Fig. 4.47(a), the resistive channel

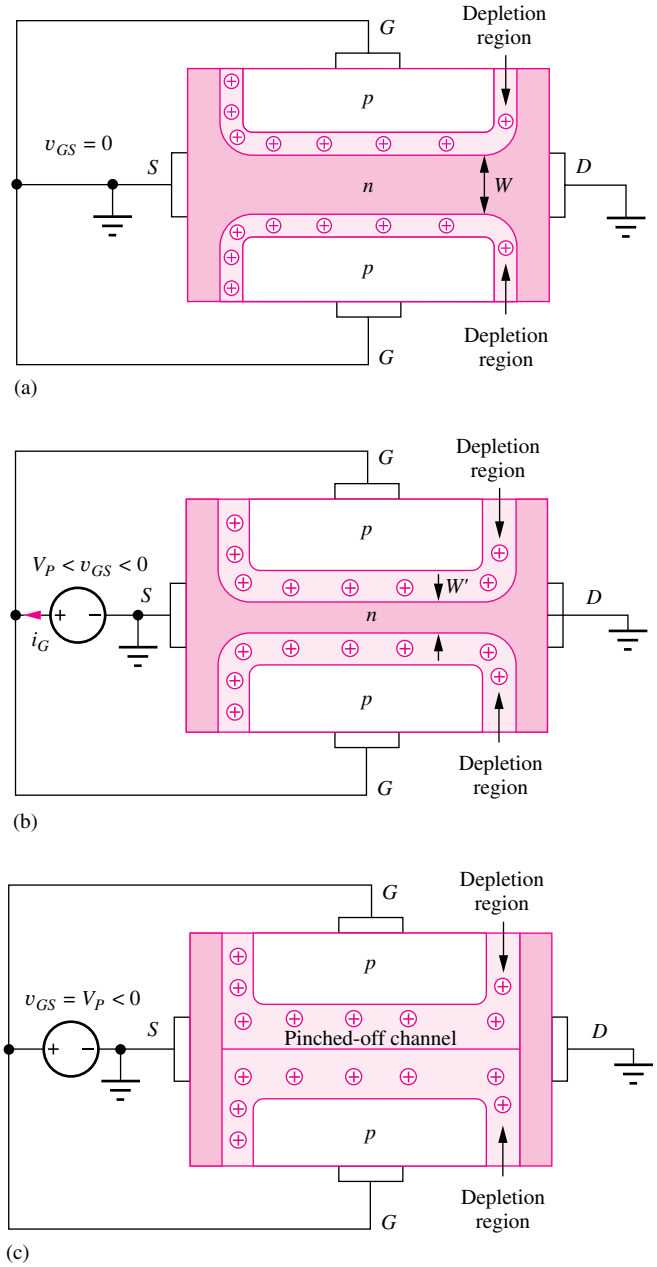


Figure 4.46 (a) JFET with zero gate-source bias. (b) JFET with negative gate-source voltage that is less negative than the pinch-off voltage V_P. Note $W' < W$. (c) JFET at pinch-off with $v_{GS} = V_P$.

connects the source and drain, the JFET is operating in its triode region, and the drain current will be dependent on the drain-source voltage v_{DS}. Assuming $i_G = 0$, the current entering the drain must exit from the source, as in the MOSFET. Note, however, that the reverse bias across the gate-channel junction is larger at the drain end of the channel than at the source end, and so the depletion layer is wider at the drain end of the device than at the source end. For increasing values of v_{DS}, the depletion layer at the drain becomes wider and wider until the channel pinches

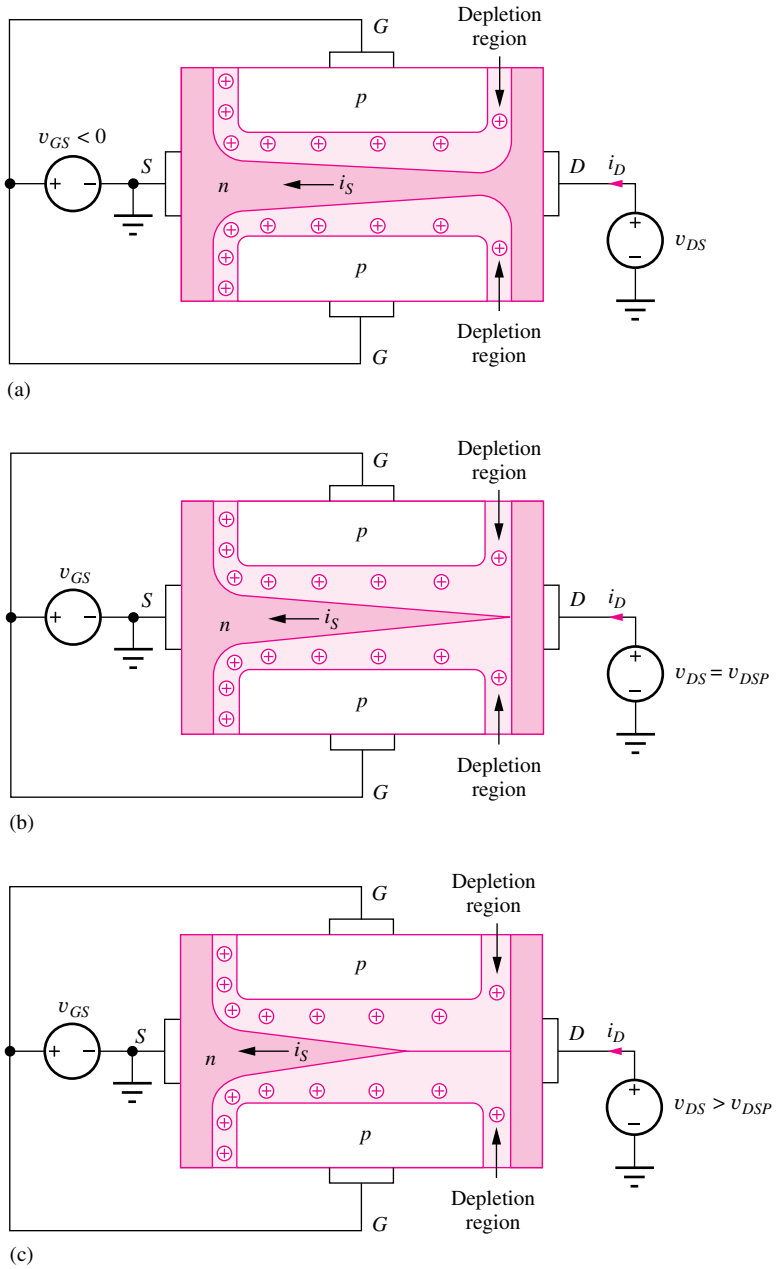


Figure 4.47 (a) JFET with small drain source. (b) JFET with channel just at pinch-off with $v_{DS} = v_{DSP}$. (c) JFET with v_{DS} greater than v_{DSP}.

off near the drain, as in Fig. 4.47(b). Pinch-off first occurs for

$$v_{GS} - v_{DSP} = V_P \qquad \text{or} \qquad v_{DSP} = v_{GS} - V_P \tag{4.90}$$

in which v_{DSP} is the value of drain voltage required to just pinch off the channel. Once the JFET channel pinches-off, the drain current saturates, just as for the MOSFET. Electrons are accelerated down the channel, injected into the depletion region, and swept on to the drain by the electric field.

Figure 4.47(c) shows the situation for an even larger value of v_{DS}. The pinch-off point moves toward the source, shortening the length of the resistive channel region. Thus, the JFET suffers from channel-length modulation in a manner similar to the MOSFET.

4.12.3 *n*-Channel JFET *i-v* Characteristics

Since the structure of the JFET is considerably different from the MOSFET, it is quite surprising that the i-v characteristics are virtually identical. We will rely on this similarity and not try to derive the JFET equations here. However, although mathematically equivalent, the equations for the JFET are usually written in a form slightly different from those of the MOSFET. We can develop this form starting with the saturation region expression for a MOSFET, in which the threshold voltage V_{TN} is replaced with the pinch-off voltage V_P:

$$i_D = \frac{K_n}{2}(v_{GS} - V_P)^2 \tag{4.91}$$

Factoring out $(-V_P)^2$ yields

$$i_D = \frac{K_n}{2}(-V_P)^2\left(1 - \frac{v_{GS}}{V_P}\right)^2 \qquad \text{or} \qquad i_D = I_{DSS}\left(1 - \frac{v_{GS}}{V_P}\right)^2 \tag{4.92}$$

in which the parameter I_{DSS} is defined by

$$I_{DSS} = \frac{K_n}{2}V_P^2 \qquad \text{or} \qquad K_n = \frac{2I_{DSS}}{V_P^2} \tag{4.93}$$

The pinch-off voltage V_P typically ranges from 0 to -25 V, and the value of I_{DSS} can range from 10 μA to more than 10 A.

If we include channel-length modulation, the expression for the drain current in pinch-off (saturation) becomes

$$I_D = I_{DSS}\left(1 - \frac{v_{GS}}{V_P}\right)^2(1 + \lambda v_{DS}) \qquad \text{for} \qquad v_{DS} \geq v_{GS} - V_P \geq 0 \tag{4.94}$$

The transfer characteristic for a JFET operating in pinch-off, based on Eq. (4.94), is shown in Fig. 4.48. I_{DSS} is the current in the JFET for $v_{GS} = 0$ and represents the maximum current in the device under normal operating conditions because the gate diode should be kept reverse-biased, with $v_{GS} \leq 0$.

The overall output characteristics for an n-channel JFET are reproduced in Fig. 4.49 with $\lambda = 0$. We see that the drain current decreases from a maximum of I_{DSS} toward zero as v_{GS} ranges from zero to the negative pinch-off voltage V_P.

The triode region of the device is also apparent in Fig. 4.49 for $v_{DS} \leq v_{GS} - V_P$. We can obtain an expression for the triode region of the JFET using the equation for the MOSFET triode region. Substituting for K_n and V_{TN} in Eq. (4.27) yields

$$i_D = \frac{2I_{DSS}}{V_P^2}\left(v_{GS} - V_P - \frac{v_{DS}}{2}\right)v_{DS} \quad \text{for } v_{GS} \geq V_P \qquad \text{and} \qquad v_{GS} - V_P \geq v_{DS} \geq 0 \tag{4.95}$$

Equations (4.94) and (4.95) represent our mathematical model for the n-channel JFET.

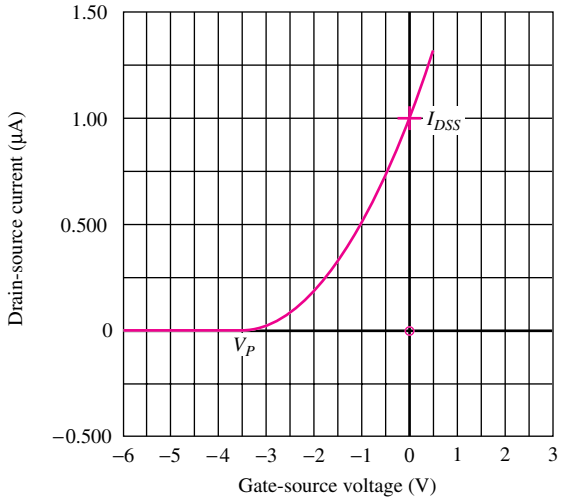


Figure 4.48 Transfer characteristic for a JFET operating in pinch-off with $I_{DSS} = 1$ mA and $V_P = -3.5$ V.

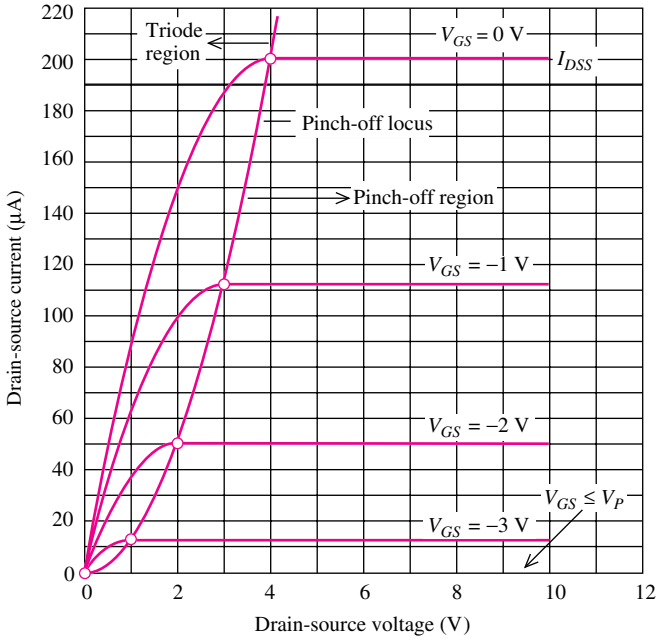


Figure 4.49 Output characteristics for a JFET with $I_{DSS} = 200$ μA and $V_P = -4$ V.

EXERCISE: (a) Calculate the current for the JFET in Fig. 4.48 for $V_{GS} = -2$ V and $V_{DS} = 3$ V. What is the minimum drain voltage required to pinch off the JFET? (b) Repeat for $V_{GS} = -1$ V and $V_{DS} = 6$ V. (c) Repeat for $V_{GS} = -2$ V and $V_{DS} = 0.5$ V.

ANSWERS: (a) 184 μA, 1.5 V; (b) 510 μA, 2.5 V; (c) 51.0 μA, 1.5 V

EXERCISE: (a) Calculate the current for the JFET in Fig. 4.49 for $V_{GS} = -2$ V and $V_{DS} = 0.5$ V. (b) Repeat for $V_{GS} = -1$ V and $V_{DS} = 6$ V.

ANSWERS: (a) 21.9 μA; (b) 113 μA

4.12.4 THE *p*-CHANNEL JFET

A ***p*-channel** version of the JFET can be fabricated by reversing the polarities of the n- and p-type regions in Fig. 4.45, as depicted in Fig. 4.50. As for the PMOSFET, the direction of current in the channel is opposite to that of the n-channel device, and the signs of the operating bias voltages will be reversed.

4.12.5 CIRCUIT SYMBOLS AND JFET MODEL SUMMARY

The circuit symbols and terminal voltages and currents for n-channel and p-channel JFETs are presented in Fig. 4.51. The arrow identifies the polarity of the gate-channel diode. The JFET structures in Figs. 4.45 and 4.50 are inherently symmetric, as were those of the MOSFET, and

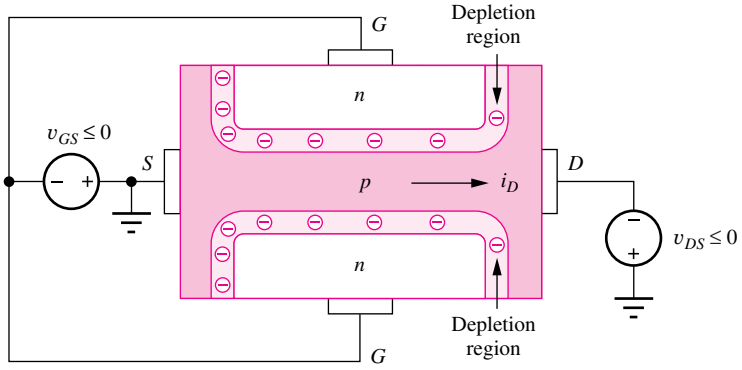


Figure 4.50 *p*-channel JFET with bias voltages.

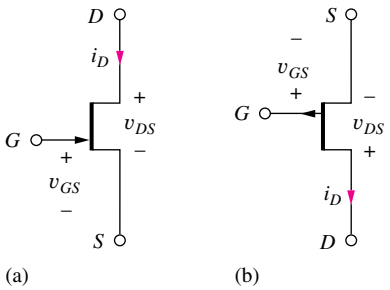


Figure 4.51 (a) *n*-channel and (b) *p*-channel JFET circuit symbols.

the source and drain are actually determined by the voltages in the circuit in which the JFET is used. However, the arrow that indicates the gate-channel junction is often offset to indicate the preferred source terminal of the device.

A summary of the mathematical models for the *n*-channel and *p*-channel JFETs follows. Because the JFET is a three-terminal device, the pinch-off voltage is independent of the terminal voltages.

n-CHANNEL JFET

For all regions:

$$i_G = 0 \quad \text{for} \quad v_{GS} \le 0 \tag{4.96}$$

Cutoff region:

$$i_D = 0 \quad \text{for} \quad v_{GS} \le V_P \quad (V_P < 0) \tag{4.97}$$

Triode region:

$$i_D = \frac{2I_{DSS}}{V_P^2}\left(v_{GS} - V_P - \frac{v_{DS}}{2}\right)v_{DS} \quad \text{for} \quad v_{GS} \ge V_P \quad \text{and} \quad v_{GS} - V_P \ge v_{DS} \ge 0 \tag{4.98}$$

Pinch-off region:

$$i_D = I_{DSS}\left(1 - \frac{v_{GS}}{V_P}\right)^2 (1 + \lambda v_{DS}) \quad \text{for} \quad v_{DS} \ge v_{GS} - V_P \ge 0 \tag{4.99}$$

p-CHANNEL JFET

For all regions:

$$i_G = 0 \quad \text{for} \quad v_{GS} \ge 0 \tag{4.100}$$

Cutoff region:

$$i_D = 0 \quad \text{for} \quad v_{GS} \le V_P \quad (V_P > 0) \tag{4.101}$$

Triode region:

$$i_D = \frac{2I_{DSS}}{V_P^2}\left(v_{GS} - V_P - \frac{v_{DS}}{2}\right)v_{DS} \quad \text{for} \quad v_{GS} \le V_P \qquad \text{and} \qquad |v_{GS} - V_P| \ge |v_{DS}| \ge 0 \tag{4.102}$$

Pinch-off region:

$$i_D = I_{DSS}\left(1 - \frac{v_{GS}}{V_P}\right)^2 (1 + \lambda|v_{DS}|) \qquad \text{for} \qquad |v_{DS}| \ge |v_{GS} - V_P| \ge 0 \tag{4.103}$$

Overall, JFETs behave in a manner very similar to that of depletion-mode MOSFETs, and the JFET is biased in the same way as a depletion-mode MOSFET. In addition, most circuit designs must ensure that the gate-channel diode remains reverse-biased. This is not a concern for the MOSFET. In certain circumstances, however, forward bias of the JFET diode can actually be used to advantage. For instance, we know that a silicon diode can be forward-biased by up to 0.4 to 0.5 V without significant conduction. In other applications, the gate diode can be used as a built-in diode clamp, and in some oscillator circuits, forward conduction of the gate diode is used to help stabilize the amplitude of the oscillation. This effect is explored in more detail during the discussion of oscillator circuits in Chapter 18.

4.12.6 JFET Capacitances

The gate-source and gate-drain capacitances of the JFET are determined by the depletion-layer capacitances of the reverse-biased *pn* junctions forming the gate of the transistor and will exhibit a bias dependence similar to that described by Eq. (3.21) in Chapter 3.

Exercise: (a) Calculate the drain current for a *p*-channel JFET described by $I_{DSS} = 2.5$ mA and $V_P = 4$ V and operating with $V_{GS} = 3$ V and $V_{DS} = -3$ V. What is the minimum drain-source voltage required to pinch off the JFET? (b) Repeat for $V_{GS} = 1$ V and $V_{DS} = -6$ V. (c) Repeat for $V_{GS} = 2$ V and $V_{DS} = -0.5$ V.

Answers: (a) 156 μA, −1.00 V; (b) 1.41 mA, −3.00 V; (c) 273 μA, −2.00 V

4.13 JFET MODELING IN SPICE

The circuit representation for the basic JFET model that is implemented in SPICE is given in Fig. 4.52. As for the MOSFET, the JFET model contains a number of additional parameters in an attempt to accurately represent the real device characteristics. Small resistances R_S and R_D appear in series with the JFET source and drain terminals, diodes are included between the gate and internal source and drain terminals, and device capacitances are included in the model.

The model for i_D is an adaptation of the MOSFET model and uses some of the parameter names and formulas from the MOSFET as can be observed in Eq. (4.104).

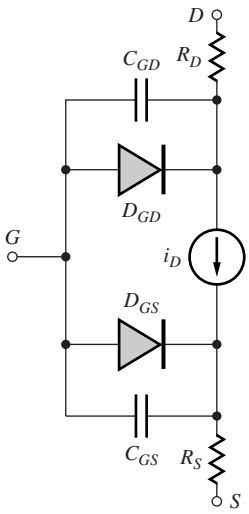


Figure 4.52 SPICE model for the *n*-channel JFET.

$$\text{Triode region:} \quad i_D = 2 \cdot \text{BETA}\left(v_{GS} - \text{VTO} - \frac{v_{DS}}{2}\right) v_{DS}(1 + \text{LAMBDA} \cdot v_{DS}) \quad \text{for} \quad v_{GS} - \text{VTO} \ge v_{DS} \ge 0 \tag{4.104}$$

$$\text{Pinch-off region:} \quad i_D = \text{BETA}(v_{GS} - \text{VTO})^2(1 + \text{LAMBDA} \cdot v_{DS}) \quad \text{for} \quad v_{DS} \ge v_{GS} - \text{VTO} \ge 0$$

TABLE 4.5
SPICE JFET Parameter Equivalences

PARAMETER	OUR TEXT	SPICE	DEFAULT
Transconductance	—	BETA	100 μA/V^2
Zero-bias drain current	I_{DSS}	—	—
Pinch-off voltage	V_P	VTO	−2 V
Cannel length modulation	λ	LAMBDA	0
Zero-bias gate-drain capacitance	C_{GD}	CGD	0
Zero-bias gate-source capacitance	C_{GS}	CGS	0
Gate-bulk capacitance per unit width	C_{GBO}	CGBO	0
Ohmic drain resistance	—	RD	0
Ohmic source resistance	—	RS	0
Gate diode saturation current	I_S	IS	10 fA

The transconductance parameter BETA is related to the JFET parameters by

$$\text{BETA} = \frac{I_{DSS}}{V_P^2} \tag{4.105}$$

The SPICE description adds a channel-length modulation term to the triode region expression. An additional quirk is that the value of VTO is always specified as a positive number for both n- and p-channel JFETS. Table 4.5 contains the equivalences of the SPICE model parameters and our equations summarized at the end of the previous section. Typical and default values of the SPICE model parameters can also be found in Table 4.5. For more detail see [5].

EXERCISE: An n-channel JFET is described by $I_{DSS} = 2.5$ mA, $V_P = -2$ V, and $\lambda = 0.025$ V^{-1}. What are the values of BETA and VTO for this transistor?

ANSWERS: 625 μA; 2 V; 0.025 V^{-1}

EXERCISE: A p-channel JFET is described by $I_{DSS} = 5$ mA, $V_P = 2$ V, and $\lambda = 0.02$ V^{-1}. What are the values of BETA and VTO for this transistor?

ANSWERS: 1.25 mA; 2 V; 0.02 V^{-1}

4.14 BIASING THE JFET AND DEPLETION-MODE MOSFET

The basic bias circuit for an n-channel JFET or depletion-mode MOSFET appears in Fig. 4.53. Because depletion-mode transistors conduct for $v_{GS} = 0$, a separate gate bias voltage is not required, and the bias circuit requires one less resistor than the four-resistor bias circuit discussed earlier in this chapter. In the circuits in Fig. 4.53, the value of R_S will set the source and drain currents, and the sum of R_S and R_D will determine the drain-source voltage. R_G is used to provide a dc connection between the gate and ground while maintaining a high resistance path for ac signal voltages that may be applied to the gate (in amplifier applications, for example). In some cases, even R_G may be omitted.

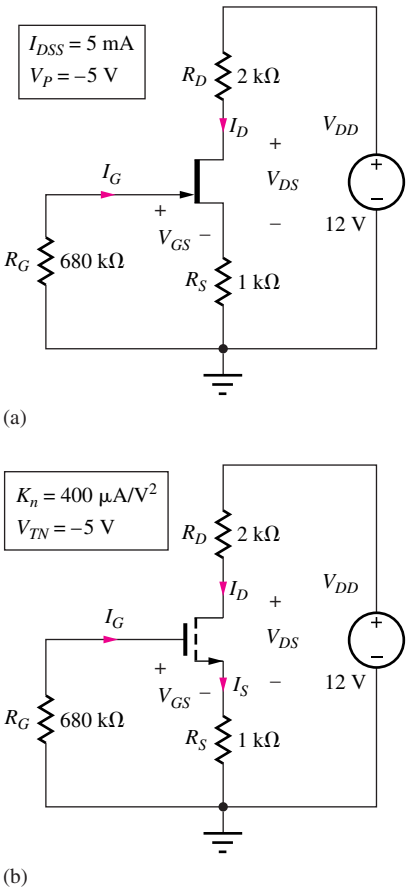


Figure 4.53 Bias circuits for (a) *n*-channel JFET and (b) depletion-mode MOSFET.

EXAMPLE 4.12 BIASING THE JFET AND DEPLETION-MODE MOSFET

Biasing of JFETs and depletion-mode MOSFETS is very similar, and this example presents a set of bias calculations for the two devices.

PROBLEM Find the quiescent operating point for the circuit in Fig. 4.53(a).

SOLUTION **Known Information and Given Data:** Circuit topology in Fig. 4.53(a) with $V_{DD} = 12$ V, $R_D = 2$ kΩ, $R_G = 680$ kΩ, $I_{DSS} = 5$ mA, and $V_P = -5$ V

Unknowns: V_{GS}, I_D, V_{DS}

Approach: Analyze the input loop to find V_{GS}. Use V_{GS} to find I_D, and I_D to determine V_{DS}.

Assumptions: The JFET is pinched-off, the gate-channel junction is reverse biased, and the reverse leakage current of the gate is negligible.

Analysis: Write the input loop equation including V_{GS}:

$$I_G R_G + V_{GS} + I_S R_S = 0 \qquad \text{or} \qquad V_{GS} = -I_D R_S \tag{4.106}$$

Equation (4.106) was simplified since $I_G = 0$ and $I_S = I_D$. By assuming the JFET is in the pinch-off region and using Eq. (4.92), Eq. (4.106) becomes

$$V_{GS} = -I_{DSS}R_S\left(1 - \frac{V_{GS}}{V_P}\right)^2 \tag{4.107}$$

Substituting in the circuit and transistor values into Eq. (4.107) yields

$$V_{GS} = -(5\times 10^{-3}\,\text{A})(1000\,\Omega)\left(1 - \frac{V_{GS}}{-5\,\text{V}}\right)^2 \quad \text{or} \quad V_{GS}^2 + 15V_{GS} + 25 = 0 \tag{4.108}$$

which has the roots -1.91 and -13.1 V. The second value is more negative than the pinch-off voltage of -5 V, so the transistor would be cutoff for this value of V_{GS}. Therefore $V_{GS} = -1.91$ V, and the drain and source currents are

$$I_D = I_S = \frac{1.91\,\text{V}}{1\,\text{k}\Omega} = 1.91\,\text{mA}$$

The drain-source voltage is found by writing the output loop equation:

$$V_{DD} = I_D R_D + V_{DS} + I_S R_S \tag{4.109}$$

which can be rearranged to yield

$$V_{DS} = V_{DD} - I_D(R_D + R_S) = 12 - (1.91\,\text{mA})(3\,\text{k}\Omega) = 6.27\,\text{V}$$

Check of Results: Our analysis yields

$$V_{GS} - V_P = -1.91\,\text{V} - (-5\,\text{V}) = +3.09\,\text{V} \qquad \text{and} \qquad V_{DS} = 6.27\,\text{V}$$

Because V_{DS} exceeds $(V_{GS} - V_P)$, the device is pinched off. In addition, the gate-source junction is reverse biased by 1.91 V. So, the JFET Q-point is (1.91 mA, 6.27 V).

Discussion: Because depletion-mode transistors conduct for $v_{GS} = 0$, a separate gate bias voltage is not required, and the bias circuit requires one less resistor than the four-resistor bias circuit discussed earlier in this chapter. The circuitry for biasing depletion-mode MOSFETs is identical as indicated in Fig. 4.53(b) — see the exercises after this example.

Computer-Aided Analysis: SPICE analysis yields the same Q-point as our hand calculations. If we add $\lambda = 0.02\ \text{V}^{-1}$, the Q-point shifts to (2.10 mA, 5.98 V). It is helpful to add a voltmeter to the circuit to directly measure V_{DS}.

EXERCISE: What are the values of VTO, BETA, and LAMBDA used in the simulation in the last example?

ANSWERS: -5 V; 0.2 mA; 0.02 V^{-1}

EXERCISE: Show that the expression for the gate-source voltage of the MOSFET in Fig. 4.53(b) is identical to Eq. (4.108). Find the Q-point for the MOSFET and show that it is the same as that for the JFET.

EXERCISE: What is the Q-point for the JFET in Fig. 4.53(a) if $V_{DD} = 9$ V?

ANSWER: (1.91 mA, 3.27 V)

EXERCISE: Find the Q-point in the circuit in Fig. 4.53(a) if R_S is changed to 2 kΩ.

ANSWER: (1.25 mA, 4.00 V)

EXERCISE: (a) Suppose the gate diode of the JFET in Fig. 4.53(a) has a reverse saturation current of 10 nA. Since the diode is reverse biased, $I_G = -10$ nA. What is the voltage at the gate terminal of the transistor? [See Eq. (4.106)]. What is the new value of V_{GS}? What will be the new Q-point of the JFET? (b) Repeat if the saturation current is 1 μA.

ANSWERS: (a) +6.80 mV, −1.91 V, (1.91 mA, 6.27 V); (b) 0.680 V, −1.64 V, (2.26 mA, 5.22 V)

SUMMARY

- This chapter discussed the structures and i-v characteristics of two types of field-effect transistors (FETs): the metal-oxide-semiconductor FET, or MOSFET, and the junction FET, or JFET.
- At the heart of the MOSFET is the MOS capacitor, formed by a metallic gate electrode insulated from the semiconductor by an insulating oxide layer. The potential on the gate controls the carrier concentration in the semiconductor region directly beneath the gate; three regions of operation of the MOS capacitor were identified: accumulation, depletion, and inversion.
- A MOSFET is formed when two pn junctions are added to the semiconductor region of the MOS capacitor. The junctions act as the source and drain terminals of the MOS transistor and provide a ready supply of carriers for the channel region of the MOSFET. The source and drain junctions must be kept reverse-biased at all times in order to isolate the channel from the substrate.
- MOS transistors can be fabricated with either n- or p-type channel regions and are referred to as NMOS or PMOS transistors, respectively. In addition, MOSFETs can be fabricated as either enhancement-mode or depletion-mode devices.
- For an enhancement-mode device, a gate-source voltage exceeding the threshold voltage must be applied to the transistor to establish a conducting channel between source and drain.
- In the depletion-mode device, a channel is built into the device during its fabrication, and a voltage must be applied to the transistor's gate to quench conduction.
- The JFET uses pn junctions to control the resistance of the conducting channel region. The gate-source voltage modulates the width of the depletion layers surrounding the gate-channel junctions and thereby changes the width of the channel region. A JFET can be fabricated with either n- or p-type channel regions, but because of its structure, the JFET is inherently a depletion-mode device.
- Both the MOSFET and JFET are symmetrical devices. The source and drain terminals of the device are actually determined by the voltages applied to the terminals. For a given geometry and set of voltages, the n-channel transistor will conduct two to three times the current of the p-channel device because of the difference between the electron and hole mobilities in the channel.
- Although structurally different, the i-v characteristics of MOSFETs and JFETs are very similar, and each type of FET has three regions of operation.
  - In cutoff, a channel does not exist, and the terminal currents are zero.

  - In the triode region of operation, the drain current in the FET depends on both the gate-source and drain-source voltages of the transistor. For small values of drain-source voltage, the transistor exhibits an almost linear relationship between its drain current and drain-source voltage. In the triode region, the FET can be used as a voltage-controlled resistor, in which the on-resistance of the transistor is controlled by the gate-source voltage of the transistor. Because of this behavior, the name *transistor* was developed as a contraction of "transfer resistor."
  - For values of drain-source voltage exceeding the pinch-off voltage, the drain current of the FET becomes almost independent of the drain-source voltage. In this region, referred to variously as the pinch-off region, the saturation region, or the active region, the drain-source current exhibits a square-law dependence on the voltage applied between the gate and source terminals. Variations in drain-source voltage do cause small changes in drain current in saturation due to channel-length modulation.
- Mathematical models for the i-v characteristics of both MOSFETs and JFETs were presented. The MOSFET is actually a four-terminal device and has a threshold voltage that depends on the source-bulk voltage of the transistor.
  - Key parameters for the MOSFET include the transconductance parameters K_n or K_p, the zero-bias threshold voltage V_{TO}, body effect parameter γ, and channel-length modulation parameter λ as well as the width W and length L of the channel.
  - The JFET was modeled as a three-terminal device with constant pinch-off voltage. Key parameters for the JFET include saturation current I_{DSS}, pinch-off voltage V_P, and channel-length modulation parameter λ.
- A variety of examples of bias circuits were presented, and the mathematical model was used to find the quiescent operating point, or Q-point, for various types of MOSFETs. The Q-point represents the dc values of drain current and drain-source voltage: (I_D, V_{DS}).
- The i-v characteristics are often displayed graphically in the form of either the output characteristics, which plot i_D versus v_{DS}, or the transfer characteristics, which graph i_D versus v_{GS}. Examples of finding the Q-point using graphical load-line and iterative numerical analyses were discussed. The examples included application of the field-effect transistor as both electronic current and voltage sources.
- The most important bias circuit in discrete design is the four-resistor circuit which yields a well-stabilized operating point. On the other hand, the current mirror, in which the output current is a scaled replica of the input current, finds very broad application in the design of both digital and analog integrated circuits. The mirror ratio is controlled by the circuit designer's choice of transistor W/L ratios.
- The gate-source, gate-drain, drain-bulk, source-bulk, and gate-bulk capacitances of MOS transistors were discussed, and the Meyer model for the gate-source and gate-bulk capacitances was introduced. All the capacitances are nonlinear functions of the terminal voltages of the transistor. The capacitances of the JFET are determined by the capacitance of the reverse-biased gate-channel junctions and also exhibit a nonlinear dependence on the terminal voltages of the transistor.
- Complex models for MOSFETs and JFETs are built into SPICE circuit analysis programs. These models contain many circuit elements and parameters to attempt to model the true behavior of the transistor as closely as possible.
- Part of the IC designer's job often includes layout of the transistors based on a set of technology-specific ground rules that define minimum feature dimensions and spaces between features.

- Constant electric field scaling provides a framework for proper miniaturization of MOS devices in which the power density remains constant as the transistor density increases. In this case, circuit delay improves directly with the scale factor α, whereas the power-delay product improves with the cube of α.
- The cutoff frequency f_T of the transistor represents the highest frequency at which the transistor can provide amplification. Cutoff frequency f_T improves with the square of the scale factor.
- The electric fields in small devices can become very high, and the carrier velocity tends to saturate at fields above 10 kV/cm. Subthreshold leakage current becomes increasingly important as devices are scaled to small dimension.

KEY TERMS

Accumulation
Accumulation region
Active region
Alignment tolerance T
Body effect
Body-effect parameter γ
Body terminal (B)
Bulk terminal (B)
C_{GS}, C_{GD}, C_{GB}, C_{DB}, C_{SB}, C''_{ox}, C_{GDO}, C_{GSO}
Capacitance per unit width
Channel length L
Channel-length modulation
Channel-length modulation parameter λ
Channel region
Channel width W
Constant electric field scaling
Current sink
Current source
Cutoff frequency
Depletion
Depletion-mode device
Depletion-mode MOSFETs
Depletion region
Design rules
Drain (D)
Electronic current source
Enhancement-mode device
Field-effect transistor (FET)
Four-resistor bias
Gate (G)
Gate-channel capacitance C_{GC}
Gate-drain capacitance C_{GD}
Gate-source capacitance C_{GS}
Ground rules
High field limitations
Inversion layer
Inversion region
Junction field-effect transistor (JFET)
KP
K'_n, K'_p
LAMDA, λ
Triode region
Metal-oxide-semiconductor field-effect transistor (MOSFET)
Minimum feature size F
Mirror ratio
MOS capacitor
n-channel JFET
n-channel MOS (NMOS)
n-channel MOSFET
n-channel transistor
NMOSFET
NMOS transistor
On-resistance (R_{on})
Output characteristics
Output resistance
Overlap capacitance
Oxide thickness
p-channel JFET
p-channel MOS (PMOS)
PHI
Pinch-off locus
Pinch-off point
Pinch-off region
Pinch-off voltage
PMOS transistor
Power delay product
Quiescent operating point
Q-point
Saturation region
Saturation voltage
Scaling theory
Small-signal output resistance
SPICE MODELS
Source (S)

Substrate sensitivity
Substrate terminal
Surface potential parameter $2\phi_F$
Subthreshold region
Threshold voltage V_{TN}, V_{TP}
Transconductance g_m
Transconductance parameter — K'_n, K'_p, KP
Transfer characteristic
Triode region
V_{TN}, V_{TP}, VT, VTO
Zero-substrate-bias value for V_{TN}

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PROBLEMS

Use the parameters in Table 4.6 as needed in the problems here.

TABLE 4.7
MOS Transistor Parameters

	NMOS DEVICE	PMOS DEVICE
V_{TO}	+0.75 V	−0.75 V
γ	$0.75\sqrt{\text{V}}$	$0.5\sqrt{\text{V}}$
$2\phi_F$	0.6 V	0.6 V
K′	25 μA/V^2	10 μA/V^2

$\varepsilon_{ox} = 3.9\varepsilon_o$ and $\varepsilon_s = 11.7\varepsilon_o$ where $\varepsilon_o = 8.854 \times 10^{-14}$ F/cm

4.1 Characteristics of the MOS Capacitor

4.1. (a) The MOS capacitor in Fig. 4.1 has $V_{TN} = 1$ V and $V_G = 2$ V. To what region of operation does this bias condition correspond? (b) Repeat for $V_G = -3$ V. (c) Repeat for $V_G = 0.5$ V.

4.2. Calculate the capacitance of an MOS capacitor with an oxide thickness T_{ox} of (a) 50 nm, (b) 20 nm, (c) 10 nm, and (d) 5 nm.

4.3. The minimum value of the depletion-layer capacitance can be estimated using an expression similar to Eq. (3.18): $C_d = \varepsilon_S / x_d$ in which the depletion-layer width is $x_d \cong \sqrt{\frac{2\varepsilon_S}{qN_B}(0.75\text{ V})}$ and N_B is the substrate doping. Estimate C_d for $N_B = 10^{-15}$/cm^3.

4.2 The NMOS Transistor

Triode (Linear) Region Characteristics

4.4. Calculate K'_n for an NMOS transistor with $\mu_n = 500$ cm^2/V · s for an oxide thickness of (a) 40 nm, (b) 20 nm, (c) 10 nm, and (d) 5 nm.

4.5. (a) What is the charge density (C/cm^2) in the channel if the oxide thickness is 25 nm and the oxide voltage exceeds the threshold voltage by 1 V? (b) Repeat for a 10-nm oxide and a bias 2 V above threshold.

4.6. (a) What is the electron velocity in the channel if $\mu_n = 500$ cm^2/V · s and the electric field is 1000 V/cm? (b) Repeat for $\mu_n = 400$ cm^2/V · s with a field of 3000 V/cm.

4.7. Equation (4.2) indicates that the charge/unit · length in the channel of a pinched-off transistor decreases as one proceeds from source to drain. However, our text argued that the current

entering the drain terminal is equal to the current exiting from the source terminal. How can a constant current exist everywhere in the channel between the drain and source terminals if the first statement is indeed true?

4.8. An NMOS transistor has $K_n' = 200\ \mu A/V^2$. What is the value of K_n if $W = 60\ \mu m$, $L = 3\ \mu m$? If $W = 3\ \mu m$, $L = 0.15\ \mu m$? If $W = 10\ \mu m$, $L = 0.25\ \mu m$?

4.9. Calculate the drain current in an NMOS transistor for $V_{GS} = 0$, 1 V, 2 V, and 3 V, with $V_{DS} = 0.1$ V, if $W = 10\ \mu m$, $L = 1\ \mu m$, $V_{TN} = 1.5$ V, and $K_n' = 250\ \mu A/V^2$. What is the value of K_n?

4.10. Calculate the drain current in an NMOS transistor for $V_{GS} = 0$, 1 V, 2 V, and 3 V, with $V_{DS} = 0.25$ V, if $W = 5\ \mu m$, $L = 0.5\ \mu m$, $V_{TN} = 1$ V, and $K_n' = 250\ \mu A/V^2$. What is the value of K_n?

4.11. Identify the source, drain, gate, and bulk terminals and find the current I in the transistors in Fig. 4.54. Assume $V_{TN} = 0.70$ V.

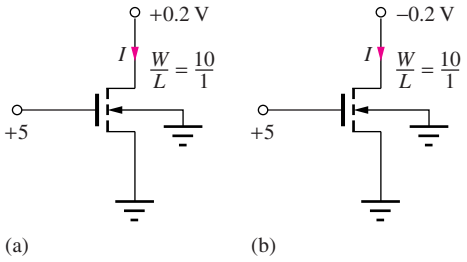

Figure 4.54

4.12. (a) What is the drain current in the transistor in Fig. 4.54(a) if the drain voltage is changed to 0.5 V? Assume $V_{TN} = 0.75$ V. (b) If the gate voltage is changed to 3 V and the drain voltage remains at 0.2 V?

4.13. (a) What is the drain current in the transistor in Fig. 4.54(b) if −0.2 V is changed to −0.5 V? Assume $V_{TN} = 0.75$ V. (b) If the gate voltage is changed to 3 V and the upper terminal voltage is replaced by −1 V?

4.14. (a) Design a transistor (choose W) to have $K_n = 5\ mA/V^2$ if $L = 0.5$ mm. (See Table 4.6.) (b) Repeat for $K_n = 750\ mA/V^2$.

On Resistance

4.15. What is the on-resistance of an NMOS transistor with $W/L = 100/1$ if $V_{GS} = 5$ V and $V_{TN} = 0.75$ V? (b) If $V_{GS} = 3.3$ V and $V_{TN} = 0.60$ V? (See Table 4.6.)

4.16. (a) What is the W/L ratio required for an NMOS transistor to have an on-resistance of 1 kΩ when $V_{GS} = 5$ V and $V_{SB} = 0$? (b) Repeat for $V_{GS} = 3.3$ V.

4.17. (a) Plot a graph of attenuation versus V_{GG} for the attenuator in Fig. 4.8 if $K_n = 500\ \mu A/V^2$, $V_{TN} = 1$ V, $R = 2$ kΩ and $0 \le V_{GG} \le 5$ V. (b) Plot a similar graph for cutoff frequency of the high-pass filter.

4.18. What value of K_n is required for the attenuator in Fig. 4.8 to give 20-dB attenuation for $V_{GG} = 5$ V if $V_{TN} = 1$ V and $R = 5$ KΩ?

4.19. Draw a circuit for a voltage-controlled low-pass filter similar to the circuits in Fig. 4.8.

4.20. The switch in a dc-to-dc boost converter (see Sec. 3.16) can easily be implemented with the NMOS transistor M_S shown in Fig. 4.55. Suppose that M_S must conduct a current $I_D = 4$ A with $V_{DS} \le 0.1$ V when it is on. What is the maximum on-resistance of M_S? If $V_G = 5$ V is used to turn on M_S and $V_{TN} = 2$ V, what is the minimum value of K_n required to achieve the required on-resistance?

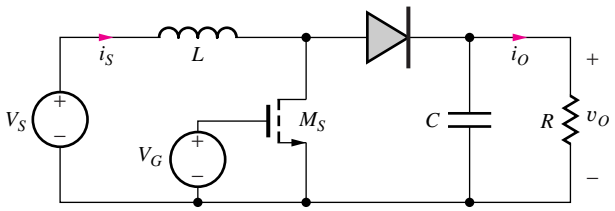

Figure 4.55

**4.21. Simulate the boost converter in Fig. 4.55 with $V_S = 5$ V, $T_{on} = 15$ mS, $T_{off} = 5$ mS, $R = 20$ W, $C = 50\ \mu F$, and $L = 0.75$ mH for $0 \le t \le 5$ mS. Assume M_S has $V_{TN} = 2$ V, $K_n = 15\ A/V^2$, and V_G switches between 0 V and 5 V with 1-ns rise and fall times. Graph v_O, i_O, i_S, and the diode current as a function of time.

Saturation of the i-v Characteristics

*4.22. The output characteristics for an NMOS transistor are given in Fig. 4.56. What are the values of K_n

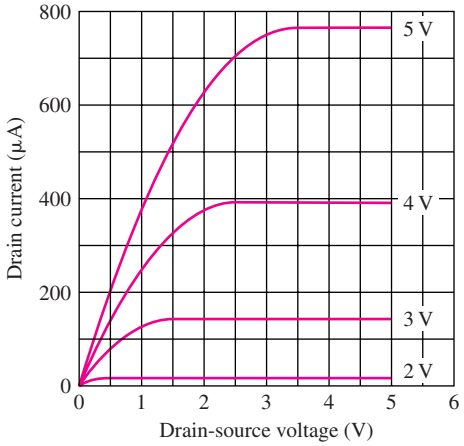

Figure 4.56

and V_{TN} for this transistor? Is this an enhancement-mode or depletion-mode transistor? What is W/L for this device?

4.23. Add the $V_{GS} = 3.5$ V and $V_{GS} = 4.5$ V curves to the i-v characteristic of Fig. 4.56. What are the values of i_{DSAT} and v_{DSAT} for these new curves?

4.24. Calculate the drain current in an NMOS transistor for $V_{GS} = 0$, 1 V, 2 V, and 3 V, with $V_{DS} = 4$ V, if $W = 10$ μm, $L = 1$ μm, $V_{TN} = 1.5$ V, and $K'_N = 250$ μA/V^2. What is the value of K_n? Check the saturation region assumption.

4.25. Calculate the drain current in an NMOS transistor for $V_{GS} = 0$, 1 V, 2 V, and 3 V, with $V_{DS} = 3.3$ V, if $W = 5$ μm, $L = 0.5$ μm, $V_{TN} = 1$ V, and $K'_n = 375$ μA/V^2. What is the value of K_n? Check the saturation region assumption.

Regions of Operation

4.26. Find the region of operation and drain current in an NMOS transistor with $W/L = 10/1$ for $V_{TN} = 0.75$ V and (a) $V_{GS} = 2$ V and $V_{DS} = 0.2$ V, (b) $V_{GS} = 2$ V and $V_{DS} = 2.5$ V, (c) $V_{GS} = 0$ V and $V_{DS} = 4$ V.

4.27. Identify the region of operation of an NMOS transistor with $K_n = 250$ μA/V^2 and $V_{TN} = 1$ V for (a) $V_{GS} = 5$ V and $V_{DS} = 6$ V, (b) $V_{GS} = 0$ V and $V_{DS} = 6$ V, (c) $V_{GS} = 2$ V and $V_{DS} = 2$ V, (d) $V_{GS} = 1.5$ V and $V_{DS} = 0.5$, (e) $V_{GS} = 2$ V and $V_{DS} = -0.5$ V, and (f) $V_{GS} = 3$ V and $V_{DS} = -6$ V.

4.28. Identify the region of operation of an NMOS transistor with $K_n = 400$ μA/V^2 and $V_{TN} = 0.7$ V for (a) $V_{GS} = 3.3$ V and $V_{DS} = 3.3$ V, (b) $V_{GS} = 0$ V and $V_{DS} = 3.3$ V, (c) $V_{GS} = 2$ V and $V_{DS} = 2$ V, (d) $V_{GS} = 1.5$ V and $V_{DS} = 0.5$, (e) $V_{GS} = 2$ V and $V_{DS} = -0.5$ V, and (f) $V_{GS} = 3$ V and $V_{DS} = -3$ V.

4.29. (a) Identify the source, drain, gate, and bulk terminals for the transistor in the circuit in Fig. 4.57. Assume $V_{DD} > 0$. (b) Repeat for $V_{DD} < 0$.

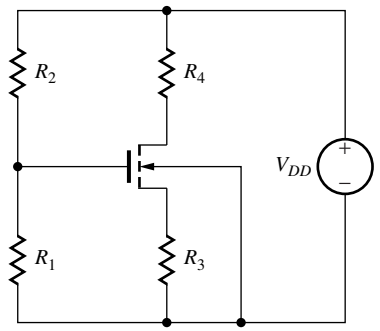

Figure 4.57

4.30. (a) Identify the source, drain, gate, and bulk terminals for each of the transistors in the circuit in Fig. 4.58(a). Assume $V_{DD} > 0$. (b) Repeat for the circuit in Fig. 4.58(b).

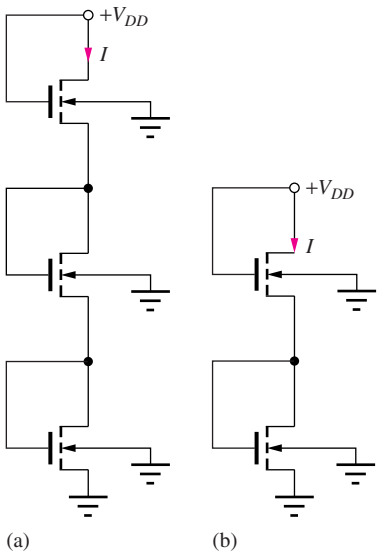

Figure 4.58

Transconductance

4.31 Calculate the transconductance for an NMOS transistor for $V_{GS} = 2$ V and 3.3 V, with $V_{DS} = 3.3$ V, if $W = 10$ μm, $L = 1$ μm, $V_{TN} = 0.7$ V, and $K'_n = 250$ μA/V^2. Check the saturation region assumption.

4.32 (a) Estimate the transconductance for the transistor in Fig. 4.56 for $V_{GS} = 4$ V and $V_{DS} = 4$ V. (*Hint:* $g_m \cong \Delta i_D / \Delta V_{GS}$.) (b) Repeat for $V_{GS} = 3$ V and $V_{DS} = 4.5$ V.

Channel-Length Modulation

4.33 (a) Calculate the drain current in an NMOS transistor if $K_n = 250\ \mu\text{A/V}^2$, $V_{TN} = 1$ V, $\lambda = 0.025\ \text{V}^{-1}$, $V_{GS} = 5$ V, and $V_{DS} = 6$ V. (b) Repeat assuming $\lambda = 0$.

4.34 (a) Calculate the drain current in an NMOS transistor if $K_n = 500\ \mu\text{A/V}^2$, $V_{TN} = 1.5$ V, $\lambda = 0.02\ \text{V}^{-1}$, $V_{GS} = 4$ V, and $V_{DS} = 5$ V. (b) Repeat assuming $\lambda = 0$.

4.35 (a) Find the drain current for the transistor in Fig. 4.59 if $\lambda = 0$. (b) Repeat if $\lambda = 0.025\ \text{V}^{-1}$. (c) Repeat part (a) if the W/L ratio is changed to 25/1.

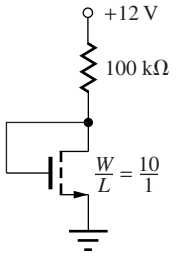

Figure 4.59

4.36 (a) Find the drain current for the transistor in Fig. 4.59 if $\lambda = 0$ and the W/L ratio is changed to 25/1. (b) Repeat if $\lambda = 0.025\ \text{V}^{-1}$.

4.37 (a) Find the current I in Fig. 4.60 if $V_{DD} = 10$ V and $\lambda = 0$. Both transistors have $W/L = 10/1$. (b) What is the current if both transistors have $W/L = 20/1$? (c) Repeat part (a) for $\lambda = 0.02\ \text{V}^{-1}$.

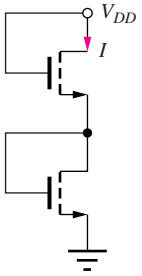

Figure 4.60

Transfer Characteristics and the Depletion-Mode MOSFET

4.38. (a) Calculate the drain current in an NMOS transistor if $K_n = 250\ \mu\text{A/V}^2$, $V_{TN} = -2$ V, $\lambda = 0$, $V_{GS} = 5$ V, and $V_{DS} = 6$ V. (b) Repeat assuming $\lambda = 0.025\ \text{V}^{-1}$.

4.39. An NMOS depletion-mode transistor is operating with $V_{DS} = V_{GS} > 0$. What is the region of operation for this device?

4.40. (a) Calculate the drain current in an NMOS transistor if $K_n = 200\ \mu\text{A/V}^2$, $V_{TN} = -3$ V, $\lambda = 0$, $V_{GS} = 0$ V, and $V_{DS} = 6$ V. (b) Repeat assuming $\lambda = 0.025\ \text{V}^{-1}$.

4.41. (a) Find the Q-point for the transistor in Fig. 4.61(a) if $V_{TN} = -2$ V. (b) Repeat for $R = 50$ kΩ and $W/L = 20/1$. (c) Repeat for Fig. 4.61(b).

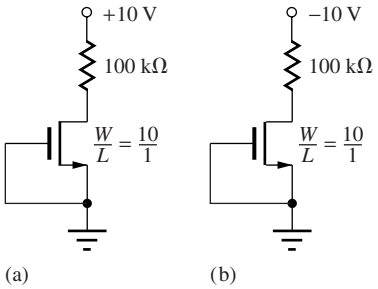

Figure 4.61

4.42. (a) Find the Q-point for the transistor in Fig. 4.61(a) if $V_{TN} = -1$ V and W/L is changed to 20/1. (b) Repeat for Fig. 4.61(b).

Body Effect or Substrate Sensitivity

4.43. Repeat Prob. 4.26 for $V_{SB} = 1.5$ V with the values from Table 4.6

4.44. (a) An NMOS transistor with $W/L = 5/1$ has $V_{TO} = 1$ V, $2\phi_F = 0.6$ V, and $\gamma = 0.7\ \sqrt{\text{V}}$. The transistor is operating with $V_{SB} = 3$ V, $V_{GS} = 2.5$ V, and $V_{DS} = 5$ V. What is the drain current in the transistor? (b) Repeat for $V_{DS} = 0.5$ V.

4.45. An NMOS transistor with $W/L = 13.8/1$ has $V_{TO} = 1.5$ V, $2\phi_F = 0.75$ V, and $\gamma = 0.5\ \sqrt{\text{V}}$. The transistor is operating with $V_{SB} = 5$ V, $V_{GS} = 2$ V, and $V_{DS} = 5$ V. What is the drain current in the transistor? (b) Repeat for $V_{DS} = 0.5$ V.

4.46. A depletion-mode NMOS transistor has $V_{TO} = -1.5$ V, $2\phi_F = 0.75$ V, and $\gamma = 1.5\ \sqrt{\text{V}}$. What

source-bulk voltage is required to change this transistor into an enhancement-mode device with a threshold voltage of +0.75 V?

*4.47. The measured body-effect characteristic for an NMOS transistor is given in Table 4.7. What are the best values of V_{TO}, γ, and $2\phi_F$ (in the least-squares sense — see Prob. 3.29) for this transistor?

TABLE 4.8

V_{SB} (V)	V_{TN} (V)
0	0.710
0.5	0.912
1.0	1.092
1.5	1.232
2.0	1.377
2.5	1.506
3.0	1.604
3.5	1.724
4.0	1.822
4.5	1.904
5.0	2.005

4.3 PMOS Transistors

4.48. Calculate K'_p for a PMOS transistor with $\mu_p = 200\ \text{cm}^2/\text{V}\cdot\text{s}$ for an oxide thickness of (a) 50 nm, (b) 20 nm, (c) 10 nm, and (d) 5 nm.

*4.49. The output characteristics for a PMOS transistor are given in Fig. 4.62. What are the values of K_p and V_{TP} for this transistor? Is this an enhancement-mode or depletion-mode transistor? What is the value of W/L for this device?

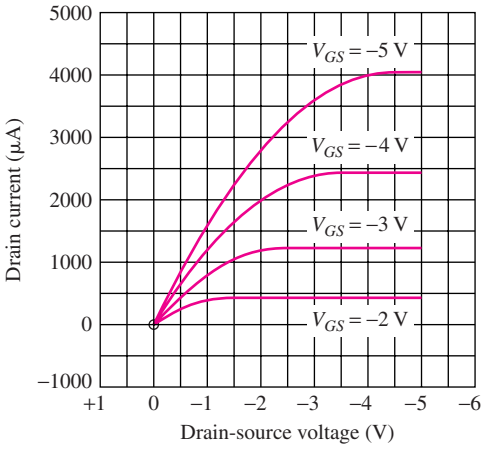

Figure 4.62

4.50. Add the $V_{GS} = -3.5$ V and $V_{GS} = -4.5$ V curves to the i-v characteristic of Fig. 4.62. What are the values of i_{DSAT} and v_{DSAT} for these new curves?

4.51. Find the region of operation and drain current in a PMOS transistor with $W/L = 10/1$ for $V_{BS} = 0$ V and (a) $V_{GS} = -1.1$ V and $V_{DS} = -0.2$ V and (b) $V_{GS} = -1.3$ V and $V_{DS} = -0.2$ V. (c) Repeat parts (a) and (b) for $V_{BS} = 1$ V.

4.52. (a) What is the W/L ratio required for an PMOS transistor to have an on-resistance of 1 kΩ when $V_{GS} = -5$ V and $V_{BS} = 0$? Assume $V_{TP} = -0.70$ V. (b) Repeat for an NMOS transistor with $V_{GS} = -5$ V and $V_{BS} = 0$? Assume $V_{TN} = 0.70$ V.

4.53. (a) What is the W/L ratio required for a PMOS transistor to have an on-resistance of 2 Ω when $V_{GS} = -5$ V and $V_{SB} = 0$? Assume $V_{TP} = -0.70$ V. (b) Repeat for an NMOS transistor with $V_{GS} = -5$ V and $V_{BS} = 0$? Assume $V_{TN} = 0.70$ V.

4.54. (a) Calculate the on-resistance for a PMOS transistor having $W/L = 100/1$ and operating with $V_{GS} = -5$ V and $V_{TP} = -0.75$ V. (b) Repeat for a similar NMOS transistor with $V_{GS} = 5$ V and $V_{TN} = 0.75$ V. (c) What W/L ratio is required for the PMOS transistor to have the same R_{on} as the NMOS transistor in (b)?

4.55. (a) Identify the source, drain, gate, and bulk terminals for the transistors in the two circuits in Fig. 4.63(a). Assume $V_{DD} = 10$ V. (b) Repeat for Fig. 4.63(b).

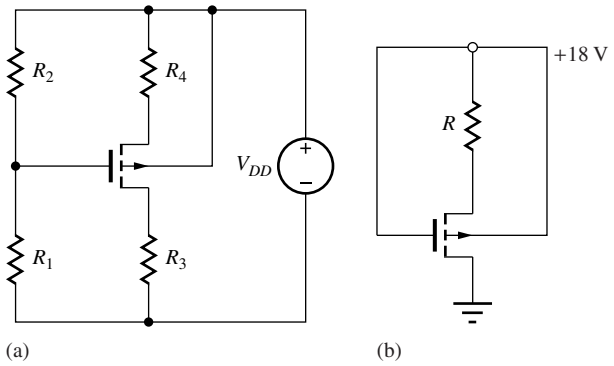

Figure 4.63

4.56. What is the on-resistance and voltage V_O for the parallel combination of the NMOS ($W/L = 10/1$) and PMOS ($W/L = 25/1$) transistors in Fig. 4.64

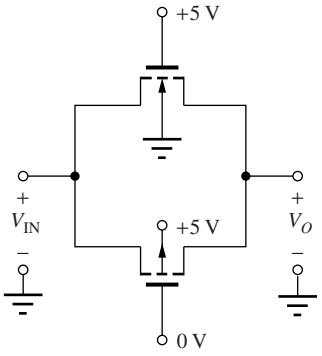

Figure 4.64

for $V_{IN} = 0$ V? (b) For $V_{IN} = 5$ V? This circuit is called a transmission-gate.

4.57. The switch in a dc-to-dc buck converter (see Sec. 3.17) can easily be implemented with the PMOS transistor M_S shown in Fig. 4.65. Suppose M_S must conduct a current $I_D = 0.5$ A with $V_{SD} \leq 0.1$ V when it is on. What is the maximum on-resistance of M_S? If $V_G = 0$ V is used to turn on M_S with $V_S = 10$ V and $V_{TP} = -2$ V, what is the minimum value of K_p is required to achieve the required on-resistance?

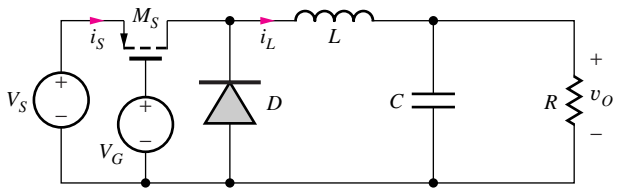

Figure 4.65

**4.58. Simulate the buck converter in Fig. 4.65 with $V_S = 5$ V, $T_{ON} = 12.5$ μS, $T_{OFF} = 12.5$ μS, $R = 5\Omega$, $C = 2$ μF, and $L = 0.625$ mH for $0 \leq t \leq 5$ mS. Assume M_S has $V_{TP} = -2$ V, $K_p = 15$ A/V^2, and V_G switches between 10 V and 0 V with 1-ns rise and fall times. Graph v_O, i_L, i_S, and the diode current as a function of time.

4.59. A PMOS transistor is operating with $V_{BS} = 0$ V, $V_{GS} = -1.5$ V, and $V_{DS} = -0.5$ V. What are the region of operation and drain current in this device if $W/L = 20/1$?

4.60. A PMOS transistor is operating with $V_{BS} = 4$ V, $V_{GS} = -1.5$ V, and $V_{DS} = -4$ V. What are the region of operation and drain current in this device if $W/L = 20/1$?

4.4 MOSFET Circuit Symbols

4.61. The PMOS transistor in Fig. 4.63(a) is conducting current. Is $V_{TP} > 0$ or $V_{TP} < 0$ for this transistor? Based on this value of V_{TP}, what type transistor is in the circuit? Is the proper symbol used in this circuit for this transistor? If not, what symbol should be used?

4.62. The PMOS transistor in Fig. 4.63(b) is conducting current. Is $V_{TP} > 0$ or $V_{TP} < 0$ for this transistor? Based on this value of V_{TP}, what type transistor is in the circuit? Is the proper symbol used in this circuit for this transistor? If not, what symbol should be used?

4.63. (a) Redraw the circuits in Fig. 4.63(a) with a three-terminal PMOS transistor with its body connected to its source. (b) Repeat for Fig. 4.63(b).

4.64. Redraw the circuit in Fig. 4.31 with a four-terminal NMOS transistor with its body connected to −3 V.

4.65. Redraw the circuit in Fig. 4.32 with a four-terminal NMOS transistor with its body connected to −3 V.

4.5 MOS Transistor Fabrication and Layout Design Rules

4.66. Layout a transistor with $W/L = 10/1$ similar to Fig. 4.23. What fraction of the total area does the channel represent?

4.67. Layout a transistor with $W/L = 5/1$ similar to Fig. 4.23 using $T = F = 2\,\Lambda$. What fraction of the total area does the channel represent?

4.68. Layout a transistor with $W/L = 5/1$ similar to Fig. 4.23 but change the alignment so that mask 3 is aligned to mask 1. What fraction of the total area does the channel represent?

4.69. Layout a transistor with $W/L = 5/1$ similar to Fig. 4.23 but change the alignment so that masks 2, 3, and 4 are all aligned to mask 1. What fraction of the total area does the channel represent?

4.6 Capacitances in MOS Transistors

4.70. Calculate C''_{ox} and C_{GC} for an MOS transistor with $W = 20$ μm and $L = 2$ μm with an oxide thickness of (a) 50 nm, (b) 20 nm, and (c) 10 nm.

4.71. Calculate C''_{ox} and C_{GC} for an MOS transistor with $W = 5$ μm and $L = 0.5$ μm with an oxide thickness of 20 nm.

4.72. In a certain MOSFET, the value of C'_{OL} can be calculated using an effective overlap distance of

0.5 μm. What is the value of C'_{OL} for an oxide thickness of 20 nm.

4.73. What are the values of C_{GS} and C_{GD} for a transistor with $C''_{ox} = 1.4 \times 10^{-3}$ F/m^2 and $C'_{OL} = 4 \times 10^{-9}$ F/m if $W = 10$ μm and $L = 1$ μm operating in (a) the triode region, (b) the saturation region, and (c) cutoff?

4.74. A large-power MOSFET has an effective gate area of 25×10^6 μm^2. What is the value of C_{GC} if T_{ox} is 100 nm?

4.75. (a) Find C_{GS} and C_{GD} for the transistor in Fig. 4.23 for the triode region if $\Lambda = 0.5$ μm, $T_{ox} = 150$ nm, and $C_{GSO} = C_{GDO} = 20$ pF/m. (b) Repeat for the saturation region. (c) Repeat for the cutoff region.

4.76. (a) Repeat Prob. 4.74 for a transistor similar to Fig. 4.23 but with $W/L = 10/1$. (b) With $W/L = 100/1$.

4.77. Find C_{SB} and C_{DB} for the transistor in Fig. 4.23 if $\Lambda = 0.5$ μm, the substrate doping is 10^{16}/cm^3, the source and drain doping is 10^{20}/cm^3, and $C_{JSW} = C_J(5 \times 10^{-4}$ cm).

4.7 MOSFET Modeling in SPICE

4.78. What are the values of SPICE model parameters KP, LAMBDA, VTO, PHI, W, and L for a transistor with the following characteristics: $V_{TN} = 0.7$ V, $K_n = 175$ μA/V^2, $W = 5$ μm, $L = 0.25$ μm, $\lambda = 0.02$ V^{-1}, and $2\phi_F = 0.8$ V?

4.79. (a) What are the values of SPICE model parameters VTO, PHI, and GAMMA for the transistor in Fig. 4.17? (b) Repeat for the transistor in Prob. 4.47.

4.8 Biasing the NMOS Field-Effect Transistor

Load Line Analysis

4.80. Draw the load line for the circuit in Fig. 4.66 on the output characteristics in Fig. 4.56 and locate the Q-point. Assume $V_{DD} = +4$ V. What is the operating region of the transistor?

4.81. Draw the load line for the circuit in Fig. 4.66 on the output characteristics in Fig. 4.56 and locate the Q-point. Assume $V_{DD} = +5$ V and the resistor is changed to 10 kΩ. What is the operating region of the transistor?

4.82. Draw the load line for the circuit in Fig. 4.67 on the output characteristics in Fig. 4.56 and locate the Q-point. Assume $V_{DD} = +6$ V. What is the operating region of the transistor?

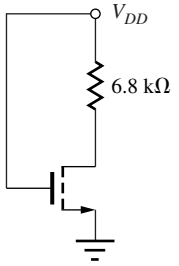

Figure 4.66

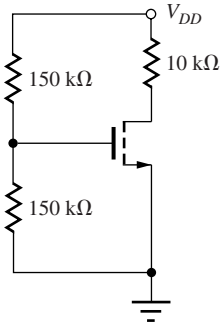

Figure 4.67

4.83. Draw the load line for the circuit in Fig. 4.67 on the output characteristics in Fig. 4.56 and locate the Q-point. Assume $V_{DD} = +8$ V. What is the operating region of the transistor?

Four-Resistor Biasing

4.84. Find the Q-point for the transistor in Fig. 4.68 for $R_1 = 100$ kΩ, $R_2 = 220$ kΩ, $R_3 = 24$ kΩ, $R_4 = 12$ kΩ, and $V_{DD} = 12$ V. Assume that $V_{TO} = 1$ V, $\gamma = 0$, and $W/L = 5/1$.

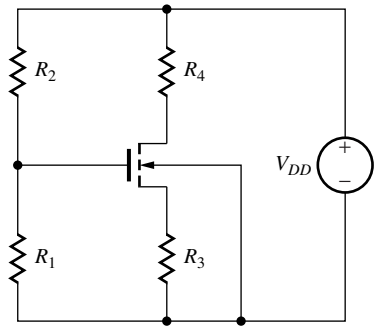

Figure 4.68

4.85. Repeat Prob. 4.84 with $V_{DD} = 15$ V.

4.86. Find the Q-point for the transistor in Fig. 4.68 for $R_1 = 200$ kΩ, $R_2 = 430$ kΩ, $R_3 = 47$ kΩ, $R_4 = 24$ kΩ, and $V_{DD} = 12$ V. Assume that $V_{TO} = 1$ V, $\gamma = 0$, and $W/L = 5/1$.

4.87. Use SPICE to simulate the circuit in Prob. 4.84 and compare the results to hand calculations.

4.88. Use SPICE to simulate the circuit in Prob. 4.85 and compare the results to hand calculations.

4.89. Use SPICE to simulate the circuit in Prob. 4.86 and compare the results to hand calculations.

4.90. The drain current in the circuit in Fig. 4.28 was found to be 50 μA. The gate bias circuit in the

example could have been designed with many different choices for resistors R_1 and R_2. Some possibilities for (R_1, R_2) are (3 kΩ, 7 kΩ), (12 kΩ, 28 kΩ), (300 kΩ, 700 kΩ), and (1.2 MΩ, 2.8 MΩ). Which of these choices would be the best and why?

*4.91. Suppose the design of Ex. 4.4 is implemented with $V_{EQ} = 4$ V, $R_S = 1.7$ kΩ, and $R_D = 38.3$ kΩ. (a) What would be the Q-point if $K_n = 35$ μA/V^2? (b) If $K_n = 25$ μA/V^2 but $V_{TN} = 0.75$ V?

4.92. (a) Simulate the circuit in Ex. 4.3 and compare the results to the calculations. (b) Repeat for the circuit design in Ex. 4.4.

4.93. Design a four-resistor bias network for an NMOS transistor to give a Q-point of (100 μA, 4 V) with $V_{DD} = 12$ V and $R_{EQ} \cong 250$ kΩ. Use the parameters from Table 4.6.

4.94. Design a four-resistor bias network for an NMOS transistor to give a Q-point of (250 μA, 3 V) with $V_{DD} = 9$ V and $R_{EQ} \cong 250$ kΩ. Use the parameters from Table 4.6.

4.95. Design a four-resistor bias network for an NMOS transistor to give a Q-point of (500 μA, 5 V) with $V_{DD} = 15$ V and $R_{EQ} \cong 600$ kΩ. Use the parameters from Table 4.6.

Depletion-Mode Devices

4.96. What is the Q-point of the transistor in Fig. 4.68 if $R_1 = 1$ MΩ, $R_2 = \infty$, $R_3 = 10$ kΩ, $R_4 = 5$ kΩ, and $V_{DD} = 15$ V if $V_{TN} = -5$ V and $K_n = 1$ mA/V^2.

4.97. What is the Q-point of the transistor in Fig. 4.68 if $R_1 = 470$ kΩ, $R_2 = \infty$, $R_3 = 27$ kΩ, $R_4 = 51$ kΩ, and $V_{DD} = 12$ V if $V_{TN} = -4$ V and $K_n = 600$ μA/V^2.

4.98. Design a bias network for a depletion-mode NMOS transistor to give a Q-point of (250 μA, 5 V) with $V_{DD} = 15$ V if $V_{TN} = -5$ V and $K_n = 1$ mA/V^2.

*4.99. Design a bias network for a depletion-mode NMOS transistor to give a Q-point of (2 mA, 5 V) with $V_{DD} = 15$ V if $V_{TN} = -2$ V and $K_n = 250$ μA/V^2. (*Hint:* You may wish to consider the four-resistor bias network.)

Two-Resistor Biasing

4.100. (a) Find the Q-point for the transistor in the circuit in Fig. 4.69(a) if $V_{DD} = +12$ V. (b) Repeat for the circuit in Fig. 4.69(b).

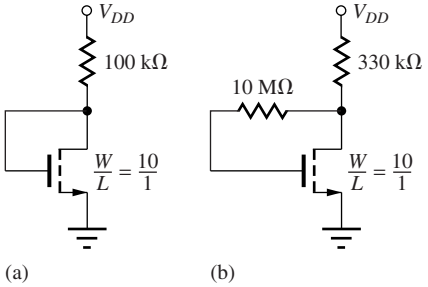

Figure 4.69

4.101. (a) Find the Q-point for the transistor in the circuit in Fig. 4.69(a) if $V_{DD} = +12$ V and W/L is changed to 20/1? (b) Repeat for the circuit in Fig. 4.69(b).

4.102. (a) Find the Q-point for the transistor in the circuit in Fig. 4.69(b) if $V_{DD} = +15$ V. (b) Repeat for $V_{DD} = +15$ V with W/L is changed to 25/1?

4.103. (a) Find the Q-point for the transistor in the circuit in Fig. 4.69(b) if $V_{DD} = +12$ V and the 330 kΩ resistor is increased to 470 kΩ. (b) Repeat if the 10 MΩ resistor is reduced to 2 MΩ.

Body Effect

4.104. Find the solution to Eq. set (4.54) using MATLAB. (b) Repeat for $\gamma = 0.75\ \sqrt{\text{V}}$.

4.105. Find the solution to Eq. set (4.54) using a spreadsheet if $\gamma = 0.75\ \sqrt{\text{V}}$. (b) Repeat for $\gamma = 1.25\ \sqrt{\text{V}}$.

4.106. Find the Q-point for the transistor in Fig. 4.68 for $R_1 = 100$ kΩ, $R_2 = 220$ kΩ, $R_3 = 24$ kΩ, $R_4 = 12$ kΩ, and $V_{DD} = 12$ V. Assume that $V_{TO} = 1$ V, $\gamma = 0.6\ \sqrt{\text{V}}$, and $W/L = 5/1$.

*4.107. (a) Repeat Prob. 4.106 with $\gamma = 0.75\ \sqrt{\text{V}}$. (b) Repeat prob. 4.106 with $R_4 = 24$ kΩ.

4.108. (a) Use SPICE to simulate the circuit in Prob. 4.106 and compare the results to hand calculations. (b) Repeat for Prob. 4.107(a). (c) Repeat for Prob. 4.107(b).

General Bias Problems

4.109. (a) Find the current I in Fig. 4.70 if $V_{DD} = 5$ V assuming that $\gamma = 0$, $V_{TO} = 1$ V, and the transistors both have $W/L = 10/1$. (b) Repeat for $V_{DD} = 10$ V. *(c) Repeat part (a) with $\gamma = 0.5\sqrt{\text{V}}$.

4.110. Find the Q-point for the transistor in Fig. 4.71 if $R = 20$ kΩ, $V_{TO} = 1$ V, and $W/L = 1/1$.

4.111. Find the Q-point for the transistor in Fig. 4.71 if $R = 10$ kΩ, $V_{TO} = 1$ V, and $W/L = 1/1$.

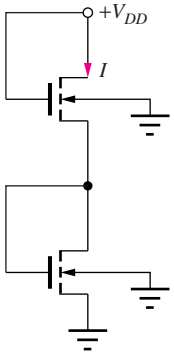

Figure 4.70

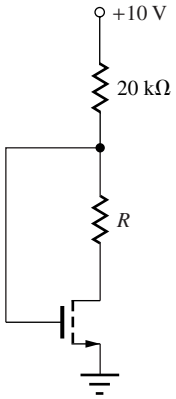

Figure 4.71

**4.112. (a) Find the current I in Fig. 4.72 assuming that $\gamma = 0$ and $W/L = 20/1$ for each transistor. (b) Repeat part (a) for $W/L = 50/1$. **(c) Repeat part (a) with $\gamma = 0.5\ \sqrt{\text{V}}$.

**4.113. (a) Simulate the circuit in Fig. 4.72 using SPICE and compare the results to those of Prob. 4.112(a). (b) Repeat for Prob. 4.112(b). **(c) Repeat for Prob. 4.112(c).

4.114. What value of W/L is required to set $V_{DS} = 0.50$ V in the circuit in Fig. 4.73 if $V = 5$ V and $R = 100$ kΩ?

4.115. What value of W/L is required to set $V_{DS} = 0.25$ V in the circuit in Fig. 4.73 if $V = 3.3$ V and $R = 150$ kΩ?

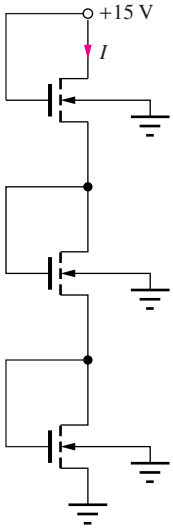

Figure 4.72

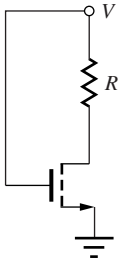

Figure 4.73

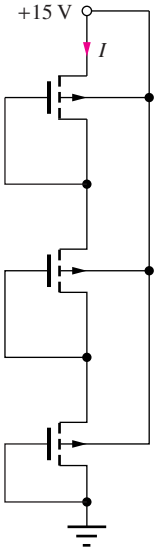

Figure 4.74

4.9 Biasing the PMOS Field-Effect Transistor

4.116. (a) Find the Q-point for the transistor in Fig. 4.75(a) if $V_{DD} = -15$ V, $R = 75$ kΩ, and $W/L = 1/1$. (b) Find the Q-point for the transistor in Fig. 4.75(b) if $V_{DD} = -15$ V, $R = 75$ kΩ, and $W/L = 1/1$.

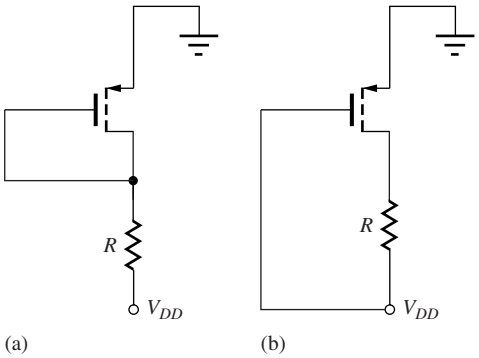

Figure 4.75

4.117. Simulate the circuits in Prob. 4.116 with $V_{DD} = -15$ V and compare the Q-point results to hand calculations.

*4.118. (a) Find current I and voltage V_O in Fig. 4.76 if $W/L = 20/1$ for both transistors and $V_{DD} = 10$ V. (b) What is the current if $W/L = 80/1$?

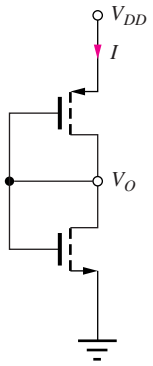

Figure 4.76

**4.119. (a) Find the current I in Fig. 4.74 assuming that $\gamma = 0$ and $W/L = 40/1$ for each transistor. (b) Repeat part (a) for $W/L = 75/1$. **(c) Repeat part (a) with $\gamma = 0.5\ \sqrt{\text{V}}$.

*4.120. (a) Simulate the circuit in Prob. 4.119(a) and compare the results to those of Prob. 4.119(a). (b) Repeat for Prob. 4.119(b). (c) Repeat for Prob. 4.119(c).

4.121. Draw the load line for the circuit in Fig. 4.77 on the output characteristics in Fig. 4.62 and locate the Q-point. What is the operating region of the transistor?

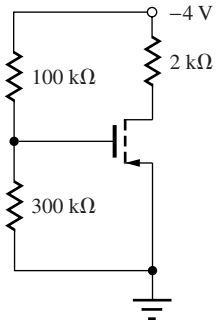

Figure 4.77

4.122. (a) Find the Q-point for the transistor in Fig. 4.78 if $R = 50\,\text{k}\Omega$. Assume that $\gamma = 0$ and $W/L = 20/1$. (b) What is the permissible range of values for R if the transistor is to remain in the saturation region?

4.123. Simulate the circuit of Prob. 4.122(a) and find the Q-point. Compare the results to hand calculations.

*4.124. (a) Find the Q-point for the transistor in Fig. 4.78 if $R = 43\ \text{k}\Omega$. Assume that $\gamma = 0.5\ \sqrt{\text{V}}$ and $W/L = 20/1$. (b) What is the permissible range of values for R if the transistor is to remain in the saturation region?

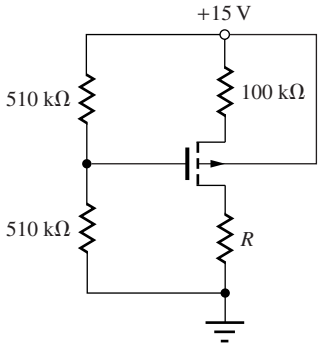

Figure 4.78

4.125. Simulate the circuit of Prob. 4.124(a) and find the Q-point. Compare the results to hand calculations.

4.126. (a) Find the Q-point for the transistor in Fig. 4.79 if $V_{DD} = 12$ V, $R = 100\ \text{k}\Omega$, $W/L = 10/1$, and $\gamma = 0$. (b) Repeat for $\gamma = 1\ \sqrt{\text{V}}$.

4.127. Find the Q-point current for the transistor in Fig. 4.79 if all resistors are reduced by a factor of 2. Assume saturation region operation. What value of R is needed to set $V_{DS} = 5$ V. Assume that $\gamma = 0$ and $W/L = 40/1$.

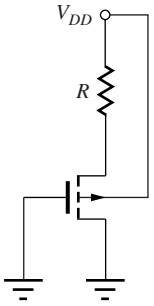

Figure 4.79

4.128. Repeat Prob. 4.127 if $\gamma = 0.5\ \sqrt{\text{V}}$ and $W/L = 40/1$.

4.129. (a) Find the Q-point current for the transistor in Fig. 4.78 if the upper 510-kΩ resistor is changed to 270 kΩ. Assume that the transistor is saturated, $\gamma = 0$, and $W/L = 20/1$. (b) What is the permissible range of values for R if the transistor is to remain in the saturation region?

4.130. Repeat Prob. 4.128 if $\gamma = 0.5\ \sqrt{\text{V}}$.

4.131. (a) Design a four-resistor bias network for a PMOS transistor to give a Q-point of (1 mA, −5 V) with $V_{DD} = -15$ V and $R_{EQ} \geq 100\ \text{k}\Omega$. Use the parameters from Table 4.6. (b) Repeat for an NMOS transistor with $V_{DS} = +6$ V.

4.132. (a) Design a four-resistor bias network for a PMOS transistor to give a Q-point of (500 μA, −3 V) with $V_{DD} = -9$ V and $R_{EQ} \geq 1\ \text{M}\Omega$. Use the parameters from Table 4.6. (b) Repeat for an NMOS transistor with $V_{DS} = +3$ V.

4.133. Find the Q-point for the transistor in Fig. 4.80 if $V_{TO} = +4$ V, $\gamma = 0$, and $W/L = 10/1$.

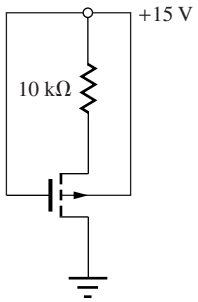

Figure 4.80

4.134. Find the Q-point for the transistor in Fig. 4.80 if $V_{TO} = +4$ V, $\gamma = 0.25\ \sqrt{\text{V}}$, and $W/L = 10/1$.

4.135. Find the Q-point for the transistor in Fig. 4.81 if $V_{TO} = -1$ V and $W/L = 10/1$.

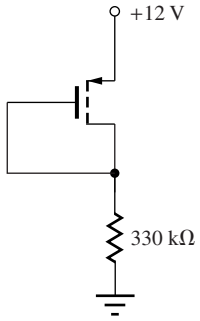

Figure 4.81

4.136. Find the Q-point for the transistor in Fig. 4.81 if $V_{TO} = -3$ V and $W/L = 30/1$.

4.137. What is the Q-point for each transistor in Fig. 4.82?

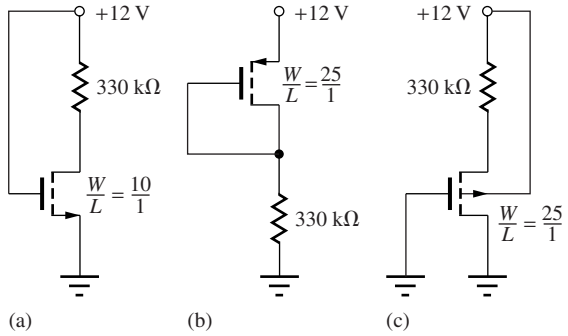

Figure 4.82

4.10 Current Sources and the MOS Current Mirror

4.138. (a) Find the Q-point for the transistor in Fig. 4.68 for $R_1 = 1$ MΩ, $R_2 = 2.2$ MΩ, $R_3 = 240$ kΩ, $R_4 = 0$, and $V_{DD} = 12$ V. Assume that $V_{TO} = 1$ V, $\gamma = 0$, and $W/L = 7.5/1$. (b) Repeat if $\gamma = 0.6\ \sqrt{\text{V}}$.

4.139. Find the Q-point for the transistor in Fig. 4.63(a) for $R_1 = 430$ kΩ, $R_2 = 220$ kΩ, $R_3 = 0$, $R_4 = 120$ kΩ, and $V_{DD} = 12$ V. Assume that $V_{TO} = -1$ V, $\gamma = 0$, and $W/L = 10/1$. (b) Repeat if $\gamma = 0.75\ \sqrt{\text{V}}$.

4.140. The depletion-mode MOSFET in Fig. 4.83 is to be used as a current source. The transistor has $W/L = 25/1$, $V_{TO} = -5$ V, and $\gamma = 0$. What value of R is required to set the current to 100 μA? What is the minimum value for V?

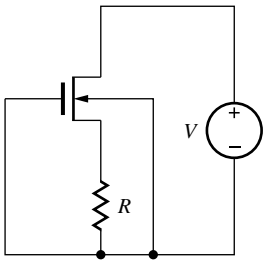

Figure 4.83

*4.141. Repeat Prob. 4.140 if $\gamma = 0.5\ \sqrt{\text{V}}$.

4.142. What are the output currents and output resistances for the current sources in Fig. 4.84 if $I_{\text{REF}} = 30$ μA, $K_n' = 25\ \mu\text{A/V}^2$, $V_{TN} = 0.75$ V, and $\lambda = 0.015\ \text{V}^{-1}$?

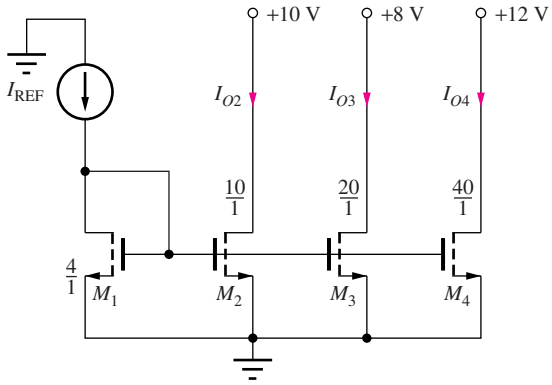

Figure 4.84

4.143. What is the minimum value of V_{DS} needed to saturate transistor M_4 in Prob. 4.142?

*4.144. What are the output currents and output resistances for the current sources in Fig. 4.85 if $R = 30$ kΩ, $K_p' = 15\ \mu\text{A/V}^2$, $V_{TP} = -0.90$ V and $\lambda = 0.01\ \text{V}^{-1}$?

4.145. What value of R is required in Fig. 4.85 to have $I_{O2} = 35$ μA? Use device data from Prob. 4.144. What is the minimum value of V_{DS} required to saturate M_3?

4.146. Simulate the current source array in Prob. 4.142 and compare the results to the hand calculations.

4.147. Simulate the current source array in Prob. 4.144 and compare the results to the hand calculations.

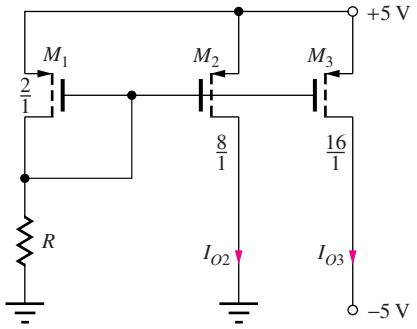

Figure 4.85

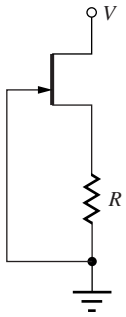

Figure 4.86

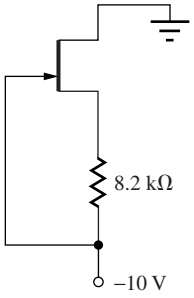

Figure 4.87

4.11 MOS Transistor Scaling

4.148. (a) A transistor has $T_{ox} = 40$ nm, $V_{TN} = 1$ V, $\mu_n = 500$ cm^2/V · s, $L = 2$ μm, and $W = 20$ μm. What are K_n and the saturated value of i_D for this transistor if $V_{GS} = 4$ V? (b) The technology is scaled by a factor of 2. What are the new values of T_{ox}, W, L, V_{TN}, V_{GS}, K_n, and i_D?

4.149. (a) A transistor has an oxide thickness of 20 nm with $L = 1$ μm and $W = 20$ μm. What is C_{GC} for this transistor? (b) The technology is scaled by a factor of 2. What are the new values of T_{ox}, W, L, and C_{GC}?

4.150. Show that the cutoff frequency of a PMOS device is given by $f_T = \frac{1}{2\pi}\frac{\mu_p}{L^2}|V_{GS} - V_{TP}|$.

4.151. (a) An NMOS device has $\mu_n = 400$ cm^2/V · s. What is the cutoff frequency for $L = 1$ μm if the transistor is biased at 1 V above threshold? What would be the cutoff frequency of a similar PMOS device if $\mu_p = 0.4\,\mu_n$? (b) Repeat for $L = 0.1$ μm.

4.152. An NMOS transistor has $T_{ox} = 80$ nm, $\mu_n = 400$ cm^2/V·s, $L = 0.1$ μm, $W = 2$ μm, and $V_{GS} - V_{TN} = 2$ V. (a) What is the saturation region current predicted by Eq. (4.19)? (b) What is the saturation current predicted by Eq. (4.88) if we assume $v_{SAT} = 10^7$ cm/s?

4.153. The NMOS transistor in Fig. 4.44 is biased with $V_{GS} = 0$ V. What is the drain current? (b) What is the drain current if the threshold voltage is reduced to 0.5 V?

4.12 The Junction Field-Effect Transistor (JFET)

4.154. The JFET in Fig. 4.86 has $I_{DSS} = 500$ μA and $V_P = -3$ V. Find the Q-point for the JFET for (a) $R = 0$ and $V = 5$ V (b) $R = 0$ and $V = 0.25$ V, and (c) $R = 8.2$ kΩ and $V = 5$ V.

4.155. Find the Q-point for the JFET in Fig. 4.87 if $I_{DSS} = 5$ mA and $V_P = -5$ V.

4.156. Find the on-resistance of the JFET in Fig. 4.88 if $I_{DSS} = 1$ mA and $V_P = -5$ V. Repeat for $I_{DSS} = 100$ μA and $V_P = -2$ V.

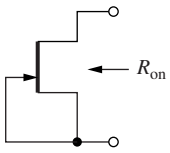

Figure 4.88

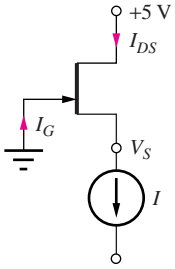

Figure 4.89

4.157. The JFET in Fig. 4.89 has $I_{DSS} = 1$ mA and $V_P = -4$ V. Find I_D, I_G, and V_S for the JFET if (a) $I = 0.5$ mA and (b) $I = 2$ mA.

*4.158. The JFETs in Fig. 4.90 have $I_{DSS1} = 200$ μA, $V_{P1} = -2$ V, $I_{DSS2} = 500$ μA, and $V_{P2} = -4$ V. (a) Find the Q-point for the two JFETs if $V = 9$ V. (b) What is the minimum value of V that will ensure that both J_1 and J_2 are in pinch-off?

*4.159. The JFETs in Fig. 4.91 have $I_{DSS} = 200$ μA and $V_P = +2$ V. (a) Find the Q-point for the two JFETs

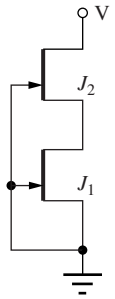

Figure 4.90

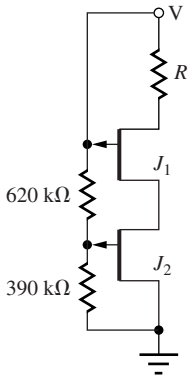

Figure 4.91

if $R = 10\ \text{k}\Omega$ and $V = 15$ V. (b) What is the minimum value of V that will ensure that both J_1 and J_2 are in pinch-off if $R = 10\ \text{k}\Omega$?

4.160. (a) The JFET in Fig. 4.92(a) has $I_{DSS} = 250\ \mu\text{A}$ and $V_P = -2$ V. Find the Q-point for the JFET. (b) The JFET in Fig. 4.92(b) has $I_{DSS} = 250\ \mu\text{A}$ and $V_P = +2$ V. Find the Q-point for the JFET.

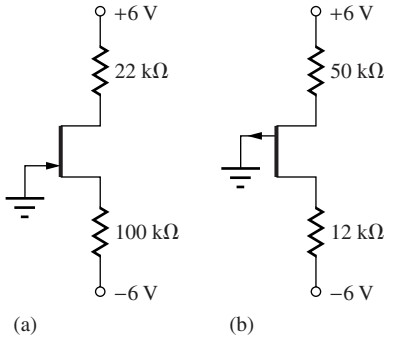

Figure 4.92

4.161. Simulate the circuit in Prob. 4.160(a) and compare the results to hand calculations. (b) Repeat for Prob. 4.160(b).

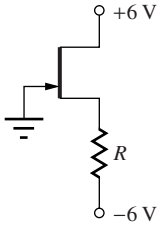

Figure 4.93

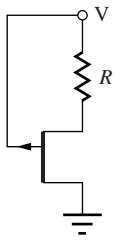

Figure 4.94

4.162. The JFET in Fig. 4.93 has $I_{DSS} = 250\ \mu\text{A}$ and $V_P = -2$ V. Find the Q-point for JFET for (a) $R = 100\ \text{k}\Omega$ and (b) $R = 10\ \text{k}\Omega$.

4.163. The JFET in Fig. 4.94 has $I_{DSS} = 500\ \mu\text{A}$ and $V_P = +3$ V. Find the Q-point for JFET for (a) $R = 0$ (b) $R = 10\ \text{k}\Omega$, and (c) $R = 100\ \text{k}\Omega$.

4.164. Simulate the circuit in Prob. 4.158(a) and compare the results to hand calculations.

4.165. Simulate the circuit in Prob. 4.159(a) and compare the results to hand calculations.

4.166. Use SPICE to plot the i-v characteristic for the circuit in Fig. 4.90 for $0 \le V \le 15$ V if the JFETs have $I_{DSS1} = 200\ \mu\text{A}$, $V_{P1} = -2$ V, $I_{DSS2} = 500\ \mu\text{A}$, and $V_{P2} = -4$ V.