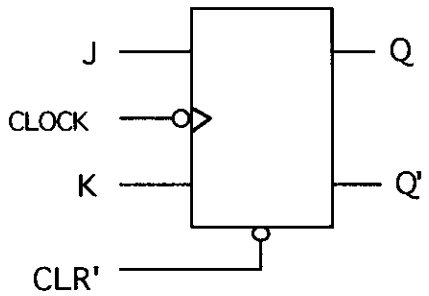
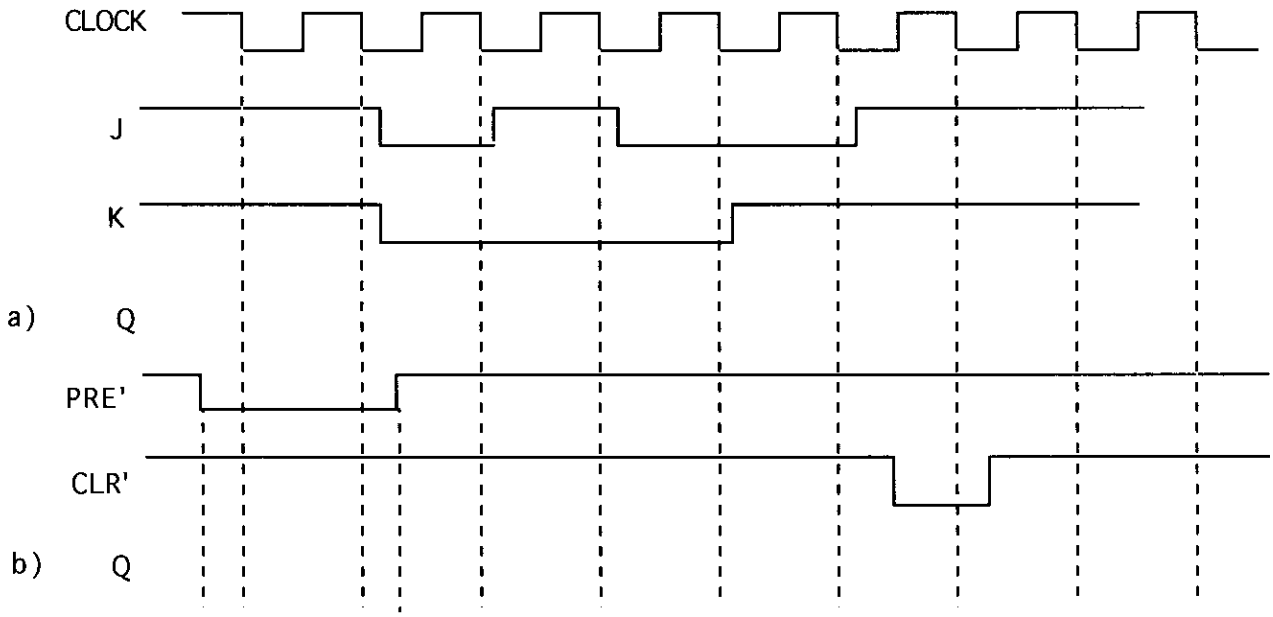
Test 7
All Problems worth 20%.

1. For the following JK trailing-edge triggered flip flop with an active low clear, show the timing diagram for Q.

   a) Assuming no PRE' or CLR' input.
   b) With the PRE' and CLR' inputs shown.



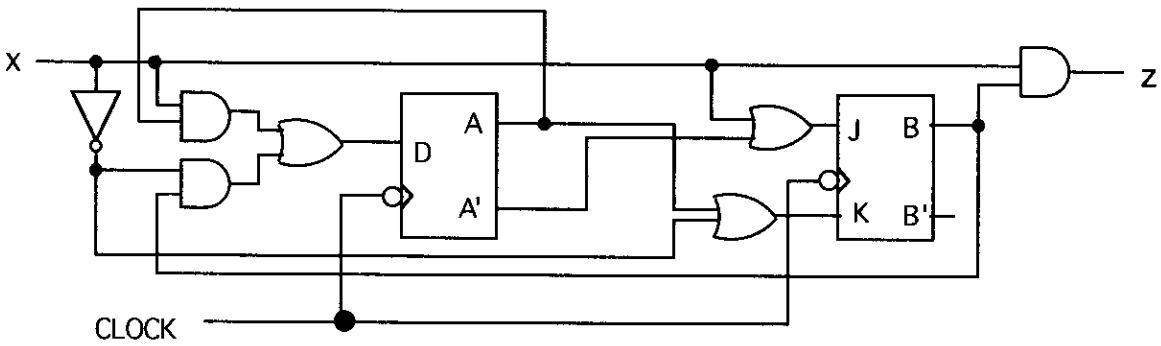



2. For the following state table, complete the timing trace as far as you can

| $q_1$ $q_2$ | $q_1$* $q_2$* | | z | |
|---|---|---|---|---|
| | x = 0 | x = 1 | x = 0 | x = 1 |
| 0 0 | 0 1 | 0 0 | 0 | 0 |
| 0 1 | 1 0 | 0 1 | 1 | 0 |
| 1 0 | 0 0 | 1 1 | 1 | 1 |
| 1 1 | 1 0 | 1 0 | 0 | 0 |

| | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| x | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 |
| $q_1$ | 0 | | | | | | | | | |
| $q_2$ | 0 | | | | | | | | | |
| z | | | | | | | | | | |

3. For the following circuit, complete the state table. (Decide if you need one or two columns for z.




| A B | A* B* | | z |
|---|---|---|---|
| | x = 0 | x = 1 | |
| 0 0 | | | |
| 0 1 | | | |
| 1 0 | | | |
| 1 1 | | | |

4. For the following state table, design a system using a JK flip flop for A, a D flip flop for B, and AND, OR and NOT gate. Show the flip flop input equations and the output equation; you do NOT need to draw a block diagram.

| A B | A* B* | | z | |
|---|---|---|---|---|
| | x= 0 | x= 1 | x= 0 | x= 1 |
| 0 0 | 0 1 | 0 1 | 0 | 0 |
| 0 1 | 0 1 | 1 0 | 1 | 0 |
| 1 0 | 1 1 | 0 0 | 1 | 1 |
| 1 1 | 1 0 | 1 0 | 0 | 0 |

5. For the following state table and state assignment, design a system using an JK flip flop for $q_1$ and a SR flip flop for $q_2$. Show the flip flop input equations and the output equation; you do NOT need to draw a block diagram.

| q | q * | | z |
|---|---|---|---|
| | x = 0 | x = 1 | |
| A | C | B | 0 |
| B | B | A | 1 |
| C | A | B | 1 |

| q | $q_1$ | $q_2$ |
|---|---|---|
| A | 0 | 0 |
| B | 1 | 1 |
| C | 0 | 1 |