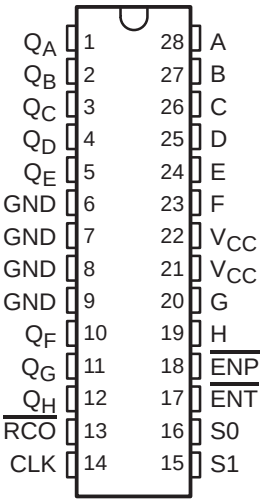
- **Inputs Are TTL-Voltage Compatible**
- **Asynchronous Clear**
- **Fully Independent Clock Circuit Simplifies Use**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

DW PACKAGE
(TOP VIEW)



description

The 74ACT11867 is a synchronous presettable binary counter featuring an internal carry look-ahead for cascading in high-speed counting applications. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation helps eliminate the output counting spikes that are normally associated with asynchronous (ripple-clock) counters. A buffered clock (CLK) input triggers the eight flip-flops on the rising (positive-going) edge of the clock waveform.

The counters are fully programmable; that is, the outputs can each be preset to either logic level. The load-mode circuitry allows parallel loading of the cascaded counters. As loading is synchronous, selecting the load mode disables the counter and causes the outputs to agree with the data inputs after the next clock rising edge.

The carry look-ahead circuitry is provided for cascading counters for n-bit synchronous applications without additional gating. This is done with two count-enable inputs and a carry output. Both count-enable ($\overline{ENP}$ and $\overline{ENT}$) inputs must be low to count. The direction of the count is determined by the levels of the select (S0 and S1) inputs (see the function table). Input $\overline{ENT}$ is fed forward to enable the ripple-carry ($\overline{RCO}$) output. $\overline{RCO}$ then produces a low-level pulse while the count is zero (all outputs low) when counting down or 255 during counting up (all outputs high). This low-level overflow carry pulse can be used to enable successive cascaded stages. Transitions at $\overline{ENP}$ and $\overline{ENT}$ are allowed regardless of the level of the clock input.

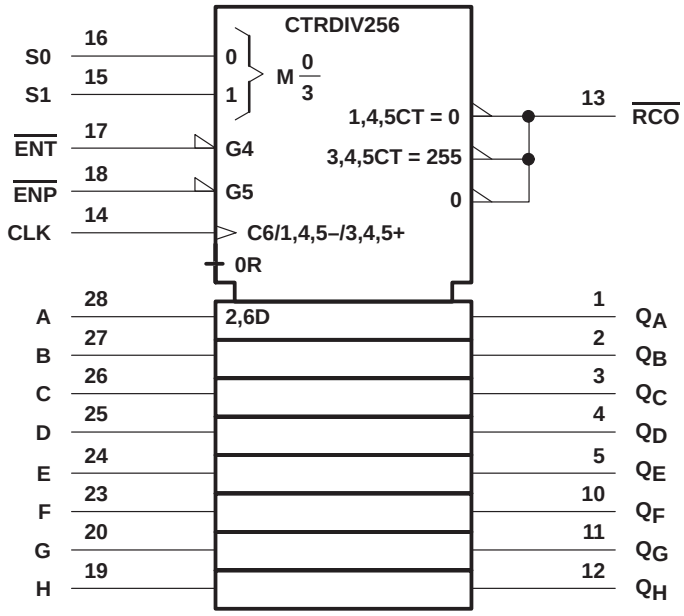
These counters feature a fully independent clock circuit. Whenever $\overline{ENP}$ and/or $\overline{ENT}$ is taken high, $\overline{RCO}$ either goes high or remains high. The function of the counter (whether enabled, disabled, loading, or counting) is dictated solely by the conditions meeting the stable setup and hold times.

The 74ACT11867 is characterized for operation from –40°C to 85°C.

MODE FUNCTION TABLE

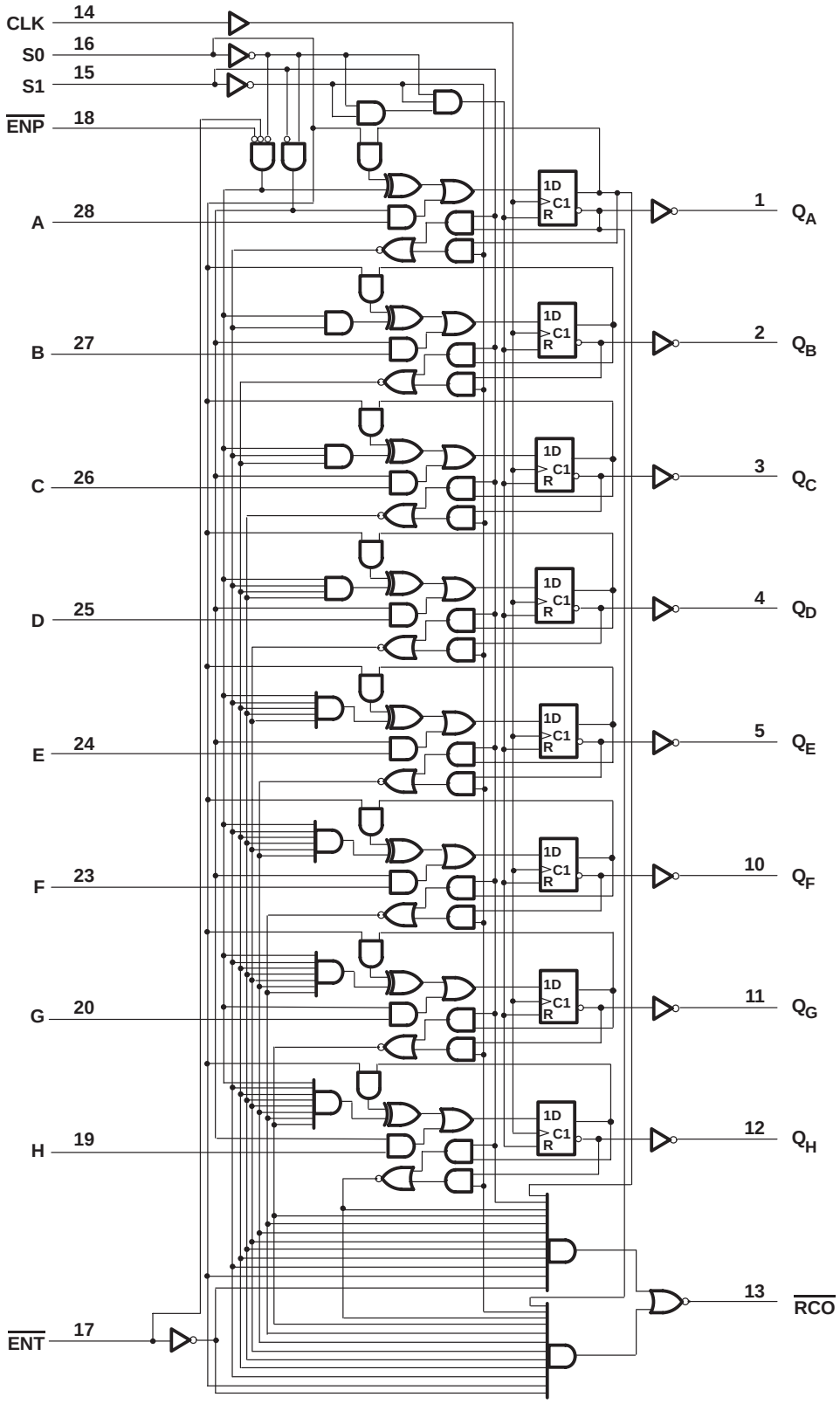
S1	S0	FUNCTION
L	L	Clear
L	H	Count down
H	L	Load
H	H	Count up

logic symbol†

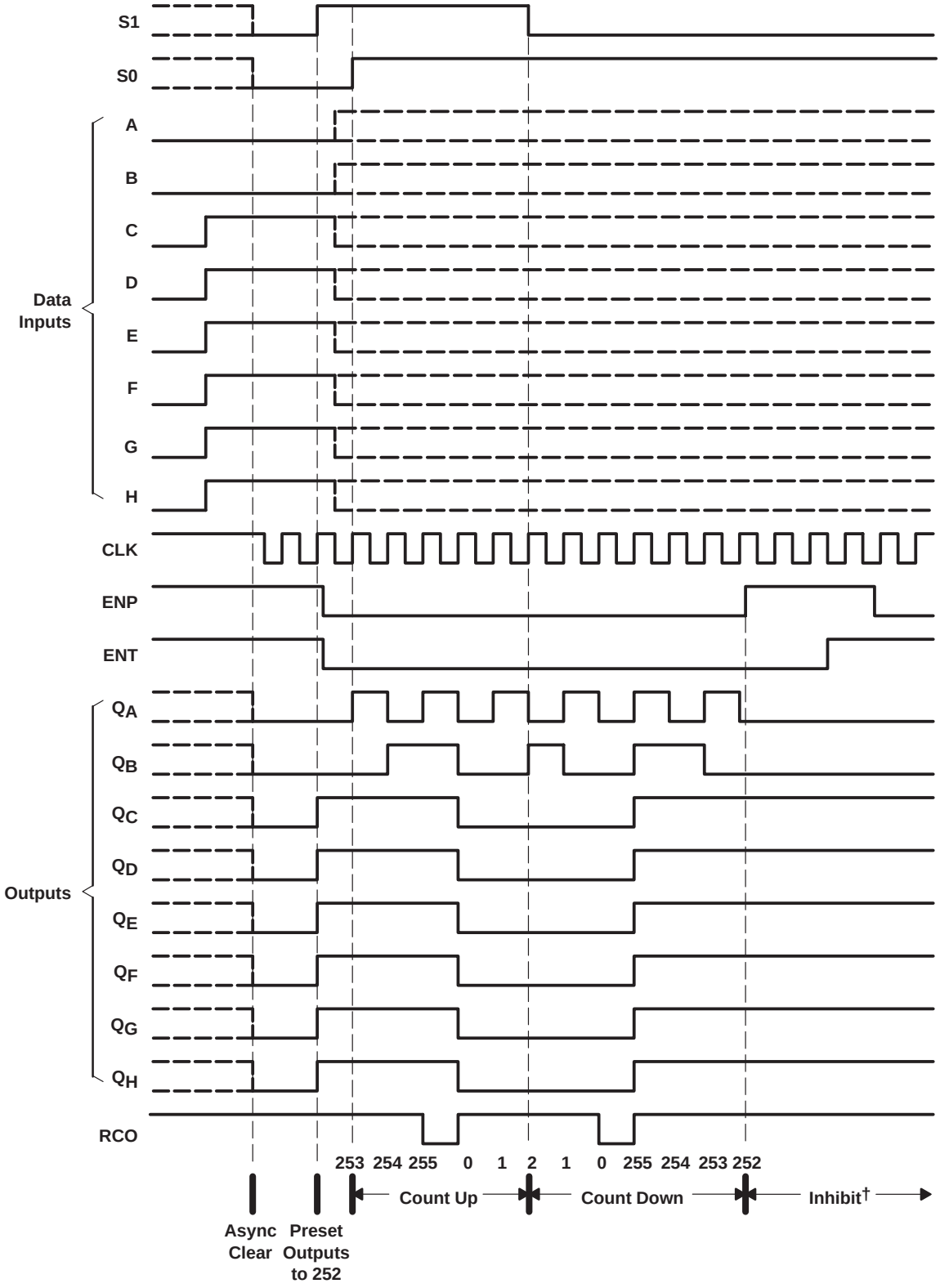


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



output sequence



† $\overline{\text{ENT}}$ and $\overline{\text{ENP}}$ must both be low for counting to occur.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND . . . . . ±225 mA
Package thermal impedance, θ_{JA} (see Note 2): DW package . . . . . 78°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
I_{OH}	High-level output current			–24	mA
I_{OL}	Low-level output current			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	ns/V
T_A	Operating free-air temperature	–40		85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}	I_{OH} = –50 µA		4.5 V	4.4			4.4		V
			5.5 V	5.4			5.4		
	I_{OH} = –24 mA		4.5 V	3.94			3.8		
			5.5 V	4.94			4.8		
	I_{OH} = –75 mA†		5.5 V				3.85		
V_{OL}	I_{OL} = 50 µA		4.5 V			0.1		0.1	V
			5.5 V			0.1		0.1	
	I_{OL} = 24 mA		4.5 V			0.36		0.44	
			5.5 V			0.36		0.44	
	I_{OL} = 75 mA†		5.5 V					1.65	
I_I	$V_I = V_{CC}$ or GND		5.5 V			±0.1		±1	µA
I_{CC}	$V_I = V_{CC}$ or GND,	I_O = 0	5.5 V			8		80	µA
ΔI_{CC}‡	One input at 3.4 V,	Other inputs at V_{CC} or GND	5.5 V			0.9		1	mA
C_i	$V_I = V_{CC}$ or GND		5 V		4.5				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
f_{clock}	Clock frequency		0	70	0	70	MHz
t_w	Pulse duration	S0 and S1 low	12		12		ns
		CLK	6.5		6.5		
t_{su}§	Setup time before CLK↑	Data	8		8		ns
		$\overline{ENP}$, $\overline{ENT}$	4		4		
		S0, S1 (load)	11		11		
		S0, S1 (count down)	11		11		
		S0, S1 (count up)	11		11		
t_h	Hold time after CLK↑	Data	1		1		ns
t_{skew}	Skew time between S0 and S1 to avoid inadvertent clear¶	S0 and S1 low		0		0	ns

§ This setup time is required to ensure stable data.
¶ This is the maximum time for which S0 and S1 can be low simultaneously when the device transitions between the load (S1 = H, S0 = L) and count-down (S1 = L, S0 = H) modes.

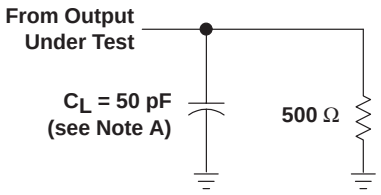
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			70			70		MHz
t_{PLH}	CLK	$\overline{RCO}$	6	9.9	12.7	6	14.6	ns
t_{PHL}			6.4	10.9	14.2	6.4	16.3	
t_{PLH}	CLK	Q	5	8.9	11.9	5	13.6	ns
t_{PHL}			4.9	9	12.2	4.9	14	
t_{PLH}	$\overline{ENT}$	$\overline{RCO}$	3.9	6.8	9.1	3.9	10.5	ns
t_{PHL}			3.1	7	10.2	3.1	11.5	
t_{PHL}	Clear (S0, S1 low)	Q	6.3	11.9	16.6	6.3	19.1	ns
t_{PLH}	S0, S1 (count up/down)	$\overline{RCO}$	5.5	10.4	15.6	5.5	17.8	ns
t_{PHL}	S0, S1 (count up/down)	$\overline{RCO}$	5.6	10.1	14.8	5.6	17.2	ns
t_{PHL}	Clear (S0, S1 low)	$\overline{RCO}$	6.2	11.3	15.6	6.2	17.8	ns

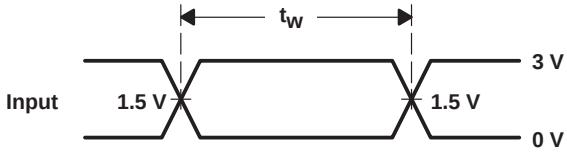
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF,	f = 1 MHz	62	pF

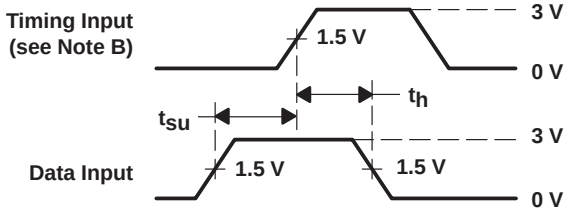
PARAMETER MEASUREMENT INFORMATION



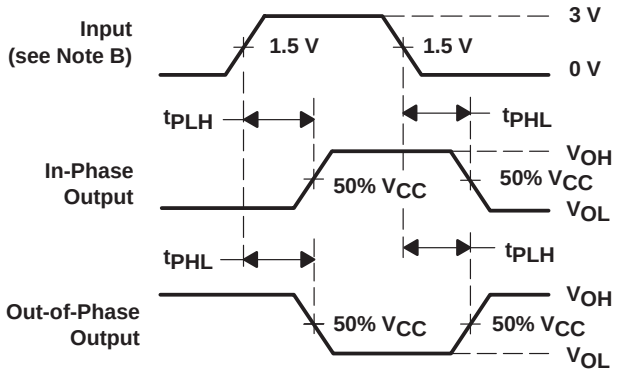
LOAD CIRCUIT



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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