

# SN54AHC00, SN74AHC00 QUADRUPLE 2-INPUT POSITIVE-NAND GATES

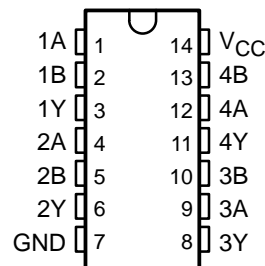
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- Operating Range 2-V to 5.5-V  $V_{CC}$
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

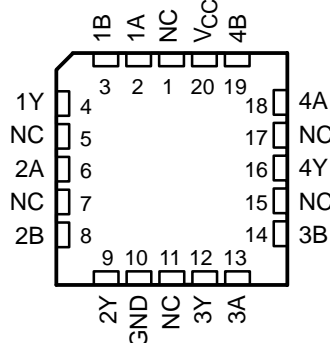
## description

The 'AHC00 devices perform the Boolean function  $Y = \overline{A} \cdot \overline{B}$  or  $Y = \overline{A + B}$  in positive logic.

SN54AHC00 . . . J OR W PACKAGE  
SN74AHC00 . . . D, DB, DGV, N, NS, OR PW PACKAGE  
(TOP VIEW)



SN54AHC00 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP – N	Tube	SN74AHC00N	SN74AHC00N
	SOIC – D	Tube	SN74AHC00D	AHC00
		Tape and reel	SN74AHC00DR	
	SOP – NS	Tape and reel	SN74AHC00NSR	AHC00
	SSOP – DB	Tape and reel	SN74AHC00DBR	HA00
	TSSOP – PW	Tape and reel	SN74AHC00PWR	HA00
–55°C to 125°C	TVSOP – DGV	Tape and reel	SN74AHC00DGV	HA00
	CDIP – J	Tube	SNJ54AHC00J	SNJ54AHC00J
	CFP – W	Tube	SNJ54AHC00W	SNJ54AHC00W
	LCCC – FK	Tube	SNJ54AHC00FK	SNJ54AHC00FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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**TEXAS  
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

# SN54AHC00, SN74AHC00

## QUADRUPLE 2-INPUT POSITIVE-NAND GATES

SCLS227G – OCTOBER 1995 – REVISED FEBRUARY 2002

FUNCTION TABLE  
(each gate)

INPUTS		OUTPUT Y
A	B	
H	H	L
L	X	H
X	L	H

logic diagram, each gate (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±25 mA
Continuous current through $V_{CC}$ or GND	±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2):	
D package	86°C/W
DB package	96°C/W
DGV package	127°C/W
N package	80°C/W
NS package	76°C/W
PW package	113°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

# SN54AHC00, SN74AHC00 QUADRUPLE 2-INPUT POSITIVE-NAND GATES

SCLS227G – OCTOBER 1995 – REVISED FEBRUARY 2002

## recommended operating conditions (see Note 3)

			SN54AHC00		SN74AHC00		UNIT
			MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage		2	5.5	2	5.5	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2 V	1.5		1.5		V
		V <sub>CC</sub> = 3 V	2.1		2.1		
		V <sub>CC</sub> = 5.5 V	3.85		3.85		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2 V		0.5		0.5	V
		V <sub>CC</sub> = 3 V		0.9		0.9	
		V <sub>CC</sub> = 5.5 V		1.65		1.65	
V <sub>I</sub>	Input voltage		0	5.5	0	5.5	V
V <sub>O</sub>	Output voltage		0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 2 V		–50		–50	μA
		V <sub>CC</sub> = 3.3 V ± 0.3 V		–4		–4	mA
		V <sub>CC</sub> = 5 V ± 0.5 V		–8		–8	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 2 V		50		50	μA
		V <sub>CC</sub> = 3.3 V ± 0.3 V		4		4	mA
		V <sub>CC</sub> = 5 V ± 0.5 V		8		8	
Δt/Δv	Input transition rise or fall rate	V <sub>CC</sub> = 3.3 V ± 0.3 V		100		100	ns/V
		V <sub>CC</sub> = 5 V ± 0.5 V		20		20	
T <sub>A</sub>	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54AHC00		SN74AHC00		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = –50 μA	2 V	1.9	2		1.9		1.9		V
		3 V	2.9	3		2.9		2.9		
		4.5 V	4.4	4.5		4.4		4.4		
	I <sub>OH</sub> = –4 mA	3 V	2.58			2.48		2.48		
	I <sub>OH</sub> = –8 mA	4.5 V	3.94			3.8		3.8		
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	2 V			0.1		0.1		0.1	V
		3 V			0.1		0.1		0.1	
		4.5 V			0.1		0.1		0.1	
	I <sub>OL</sub> = 4 mA	3 V			0.36		0.5		0.44	
	I <sub>OL</sub> = 8 mA	4.5 V			0.36		0.5		0.44	
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	0 V to 5.5 V			±0.1		±1*		±1	μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			2		20		20	μA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		2	10				10	pF

\* On products compliant to MIL-PRF-38535, this parameter is not production tested at V<sub>CC</sub> = 0 V.



# SN54AHC00, SN74AHC00

## QUADRUPLE 2-INPUT POSITIVE-NAND GATES

SCLS227G – OCTOBER 1995 – REVISED FEBRUARY 2002

**switching characteristics over recommended operating free-air temperature range,  
V<sub>CC</sub> = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			SN54AHC00		SN74AHC00		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	A or B	Y	C <sub>L</sub> = 15 pF	5.5*	7.9*	1*	9.5*	1	9.5	ns	
t <sub>PHL</sub>				5.5*	7.9*	1*	9.5*	1	9.5		
t <sub>PLH</sub>	A or B	Y	C <sub>L</sub> = 50 pF	8	11.4	1	13	1	13	ns	
t <sub>PHL</sub>				8	11.4	1	13	1	13		

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

**switching characteristics over recommended operating free-air temperature range,  
V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			SN54AHC00		SN74AHC00		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	A or B	Y	C <sub>L</sub> = 15 pF	3.7*	5.5*	1*	6.5*	1	6.5	ns	
t <sub>PHL</sub>				3.7*	5.5*	1*	6.5*	1	6.5		
t <sub>PLH</sub>	A or B	Y	C <sub>L</sub> = 50 pF	5.2	7.5	1	8.5	1	8.5	ns	
t <sub>PHL</sub>				5.2	7.5	1	8.5	1	8.5		

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

**noise characteristics, V<sub>CC</sub> = 5 V, C<sub>L</sub> = 50 pF, T<sub>A</sub> = 25°C (see Note 4)**

PARAMETER		SN74AHC00			UNIT
		MIN	TYP	MAX	
V <sub>OL(P)</sub>	Quiet output, maximum dynamic V <sub>OL</sub>	0.3	0.8		V
V <sub>OL(V)</sub>	Quiet output, minimum dynamic V <sub>OL</sub>	–0.3	–0.8		V
V <sub>OH(V)</sub>	Quiet output, minimum dynamic V <sub>OH</sub>	4.6			V
V <sub>IH(D)</sub>	High-level dynamic input voltage	3.5			V
V <sub>IL(D)</sub>	Low-level dynamic input voltage		1.5		V

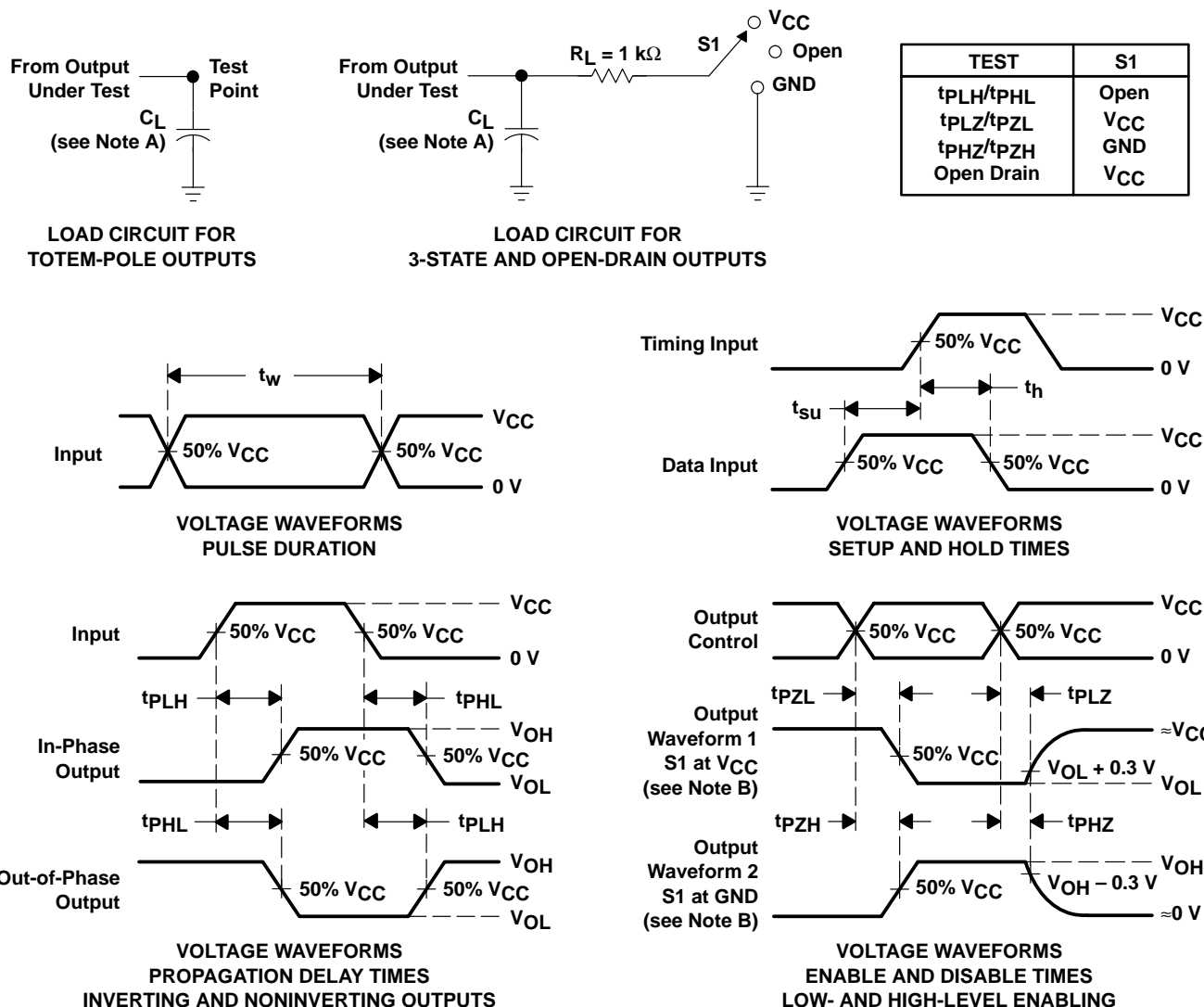
NOTE 4: Characteristics are for surface-mount packages only.

**operating characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C**

PARAMETER	TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub> Power dissipation capacitance	No load, f = 1 MHz	9.5	pF



# PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\text{ }\Omega$ ,  $t_r \leq 3\text{ ns}$ ,  $t_f \leq 3\text{ ns}$ .
- D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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