The Bipolar Junction Transistor

Chapter 5

In Chapter 2, we saw that the rectifying current–voltage characteristics of the diode are useful in electronic switching and waveshaping circuits. However, diodes are not capable of amplifying currents or voltages. As was shown in Chapter 4, the electronic device that is capable of current and voltage amplification, or gain, in conjunction with other circuit elements, is the transistor. The development of the transistor by Bardeen, Brattain, and Schockley at Bell Telephone Laboratories in the late 1940s started the first electronics revolution of the 1950s and 1960s. This invention led to the development of the first integrated circuit in 1958 and to the transistor operational amplifier (op-amp), which is one of the most widely used electronic circuits.

The bipolar transistor, which is introduced in this chapter, is one of the two major types of transistors. The second type of transistor, the field-effect transistor (FET), was introduced in Chapter 3. These two device types are the basis of modern microelectronics. Each device type is equally important and each has particular advantages for specific applications.

PREVIEW

In this chapter, we will:

- Discuss the physical structure and operation of the bipolar junction transistor.
- Understand and become familiar with the dc analysis and design techniques of bipolar transistor circuits.
- Examine three basic applications of bipolar transistor circuits.
- Investigate various dc biasing schemes of bipolar transistor circuits, including integrated circuit biasing.
- Consider the dc biasing of multistage or multi-transistor circuits.
- As an application, incorporate the bipolar transistor in a circuit design that enhances the simple diode electronic thermometer discussed in Chapter 1.

5.1 BASIC BIPOLAR JUNCTION TRANSISTOR

Objective: • Understand the physical structure, operation, and characteristics of the bipolar junction transistors (BJT), including the npn and pnp devices.

The **bipolar junction transistor (BJT)** has three separately doped regions and contains two pn junctions. A single pn junction has two modes of operation—forward bias and reverse bias. The bipolar transistor, with two pn junctions, therefore has four possible modes of operation, depending on the bias condition of each pn junction, which is one reason for the versatility of the device. With three separately doped regions, the bipolar transistor is a three-terminal device. The basic transistor principle is that *the voltage between two terminals controls the current through the third terminal*.

Our discussion of the bipolar transistor starts with a description of the basic transistor structure and a qualitative description of its operation. To describe its operation, we use the pn junction concepts presented in Chapter 1. However, the two pn junctions are sufficiently close together to be called interacting pn junctions. The operation of the transistor is therefore totally different from that of two back-to-back diodes.

Current in the transistor is due to the flow of both electrons and holes, hence the name **bipolar.** Our discussion covers the relationship between the three terminal currents. In addition, we present the circuit symbols and conventions used in bipolar circuits, the bipolar transistor current–voltage characteristics, and finally, some nonideal current–voltage characteristics.

5.1.1 Transistor Structures

Figure 5.1 shows simplified block diagrams of the basic structure of the two types of bipolar transistor: npn and pnp. The **npn bipolar transistor** contains a thin p-region between two n-regions. In contrast, the **pnp bipolar transistor** contains a thin n-region sandwiched between two p-regions. The three regions and their terminal connections are called the **emitter, base,** and **collector.**[1] The operation of the device depends on the two pn junctions being in close proximity, so the width of the base must be very narrow, normally in the range of tenths of a micrometer (10^{-6} m).

The actual structure of the bipolar transistor is considerably more complicated than the block diagrams of Figure 5.1. For example, Figure 5.2 is the cross section of

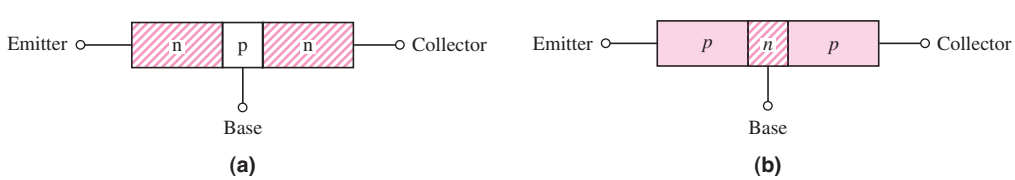

Figure 5.1 Simple geometry of bipolar transistors: (a) npn and (b) pnp

[1]The reason for the names **emitter** and **collector** for the terminals will become obvious as we go through the operation of the transistor. The term **base** refers to the structure of the original transistor.

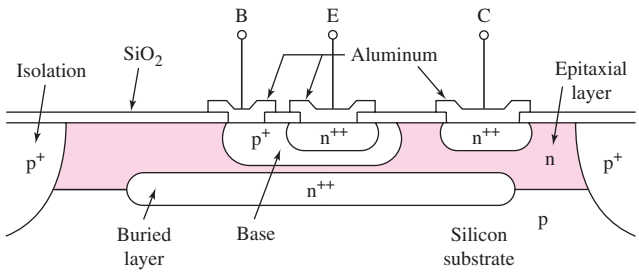

Figure 5.2 Cross section of a conventional integrated circuit npn bipolar transistor

a classic npn bipolar transistor fabricated in an integrated circuit. One important point is that the device is not symmetrical electrically. This asymmetry occurs because the geometries of the emitter and collector regions are not the same, and the impurity doping concentrations in the three regions are substantially different. For example, the impurity doping concentrations in the emitter, base, and collector may be on the order of 10^{19}, 10^{17}, and 10^{15} cm^{-3}, respectively. Therefore, even though both ends are either p-type or n-type on a given transistor, switching the two ends makes the device act in drastically different ways.

Although the block diagrams in Figure 5.1 are highly simplified, they are still useful for presenting the basic transistor characteristics.

5.1.2 npn Transistor: Forward-Active Mode Operation

Since the transistor has two pn junctions, four possible bias combinations may be applied to the device, depending on whether a forward or reverse bias is applied to each junction. For example, if the transistor is used as an amplifying device, the **base–emitter (B–E) junction** is forward biased and the **base–collector (B–C) junction** is reverse biased, in a configuration called the **forward-active operating mode,** or simply the **active region.** The reason for this bias combination will be illustrated as we look at the operation of such transistors and the characteristics of circuits that use them.

Transistor Currents

Figure 5.3 shows an idealized npn bipolar transistor biased in the forward-active mode. Since the B–E junction is forward biased, electrons from the emitter are injected across

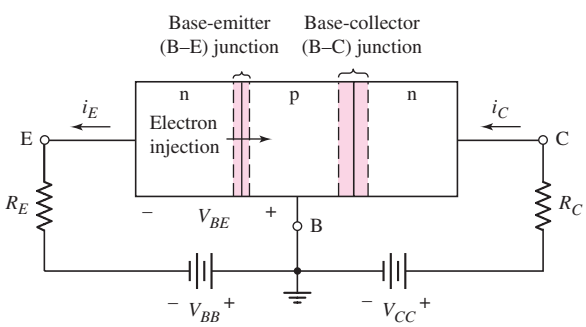

Figure 5.3 An npn bipolar transistor biased in the forward-active mode; base–emitter junction forward biased and base–collector junction reverse biased

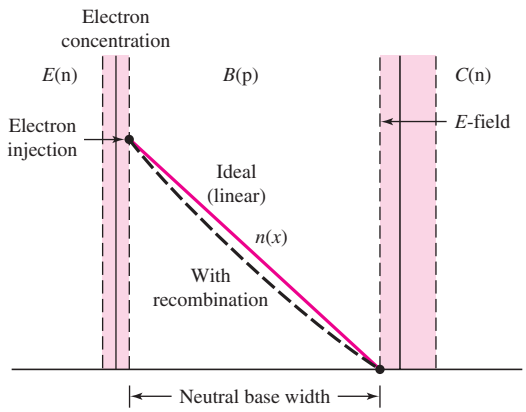

Figure 5.4 Minority carrier electron concentration across the base region of an npn bipolar transistor biased in the forward-active mode. Minority carrier concentration is a linear function versus distance for an ideal transistor (no carrier recombination), and is a nonlinear function versus distance for a real device (with carrier recombination).

the B–E junction into the base, creating an excess minority carrier concentration in the base. Since the B–C junction is reverse biased, the electron concentration at the edge of that junction is approximately zero.

The base region is very narrow so that, in the ideal case, the injected electrons will not recombine with any of the majority carrier holes in the base. In this case, the electron distribution versus distance through the base is a straight line as shown in Figure 5.4. Because of the large gradient in this concentration, electrons that are injected, or *emitted,* from the emitter region diffuse across the base, are swept across the base–collector space-charge region by the electric field, and are *collected* in the collector region creating the collector current. However, if some carrier recombination does occur in the base, the electron concentration will deviate from the ideal linear curve, as shown in the figure. To minimize recombination effects, the width of the neutral base region must be small compared to the minority carrier diffusion length.

Emitter Current: Since the B–E junction is forward biased, we expect the current through this junction to be an exponential function of B–E voltage, just as we saw that the current through a pn junction diode was an exponential function of the forward-biased diode voltage. We can then write the current at the emitter terminal as

$$i_E = I_{EO}[e^{v_{BE}/V_T} - 1] \cong I_{EO}e^{v_{BE}/V_T} \tag{5.1}$$

where the approximation of neglecting the (-1) term is usually valid since $v_{BE} \gg V_T$ in most cases.[2] The parameter V_T is the usual thermal voltage. The emission coefficient n that multiplies V_T is assumed to be 1, as we discussed in Chapter 1 in considering the ideal diode equation. The flow of the negatively charged electrons is through the emitter into the base and is opposite to the conventional current direction. The conventional emitter current direction is therefore out of the emitter terminal.

[2]The voltage notation v_{BE}, with the dual subscript, denotes the voltage between the B (base) and E (emitter) terminals. Implicit in the notation is that the first subscript (the base terminal) is positive with respect to the second subscript (the emitter terminal).

We will assume that the ideality factor n in this diode equation is unity (see Chapter 1).

The multiplying constant, I_{EO}, contains electrical parameters of the junction, but in addition is directly proportional to the active B–E cross-sectional area. Therefore, if two transistors are identical except that one has twice the area of the other, then the emitter currents will differ by a factor of two for the same applied B–E voltage. Typical values of I_{EO} are in the range of 10^{-12} to 10^{-16} A, but may, for special transistors, vary outside of this range.

Collector Current: Since the doping concentration in the emitter is much larger than that in the base region, the vast majority of emitter current is due to the injection of electrons into the base. The number of these injected electrons reaching the collector is the major component of collector current.

The number of electrons reaching the collector per unit time is proportional to the number of electrons injected into the base, which in turn is a function of the B–E voltage. To a first approximation, the collector current is proportional to e^{v_{BE}/V_T} and is independent of the reverse-biased B–C voltage. The device therefore looks like a **constant-current source.** The collector current is controlled by the B–E voltage; in other words, the current at one terminal (the collector) is controlled by the voltage across the other two terminals. *This control is the basic transistor action.*

We can write the collector current as

$$i_C = I_S e^{v_{BE}/V_T} \tag{5.2}$$

The collector current is slightly smaller than the emitter current, as we will show. The emitter and collector currents are related by $i_C = \alpha i_E$. We can also relate the coefficients by $I_S = \alpha I_{EO}$. The parameter α is called the **common-base current gain** whose value is always slightly less than unity. The reason for this name will become clearer as we proceed through the chapter.

Base Current: Since the B–E junction is forward biased, holes from the base are injected across the B–E junction into the emitter. However, because these holes do not contribute to the collector current, they are not part of the transistor action. Instead, the flow of holes forms one component of the base current. This component is also an exponential function of the B–E voltage, because of the forward-biased B–E junction. We can write

$$i_{B1} \propto e^{v_{BE}/V_T} \tag{5.3(a)}$$

A few electrons recombine with majority carrier holes in the base. The holes that are lost must be replaced through the base terminal. The flow of such holes is a second component of the base current. This "recombination current" is directly proportional to the number of electrons being injected from the emitter, which in turn is an exponential function of the B–E voltage. We can write

$$i_{B2} \propto e^{v_{BE}/V_T} \tag{5.3(b)}$$

The total base current is the sum of the two components from Equations (5.3(a)) and (5.3(b)):

$$i_B \propto e^{v_{BE}/V_T} \tag{5.4}$$

Figure 5.5 shows the flow of electrons and holes in an npn bipolar transistor, as well as the terminal currents.[3] (Reminder: the conventional current direction is the

[3]A more thorough study of the physics of the bipolar transistor shows that there are other current components, in addition to the ones mentioned. However, these additional currents do not change the basic properties of the transistor and can be neglected for our purposes.

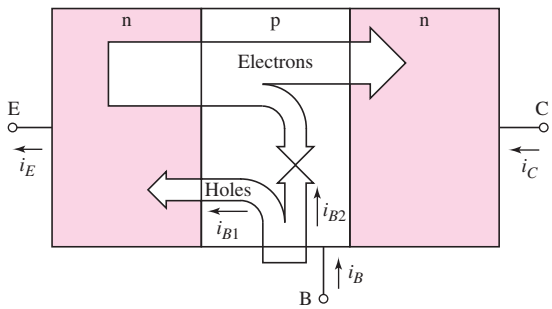

Figure 5.5 Electron and hole currents in an npn bipolar transistor biased in the forward-active mode. Emitter, base, and collector currents are proportional to e^{v_{BE}/V_T}.

same as the flow of positively charged holes and opposite to the flow of negatively charged electrons.)

If the concentration of electrons in the n-type emitter is much larger than the concentration of holes in the p-type base, then the number of electrons injected into the base will be much larger than the number of holes injected into the emitter. This means that the i_{B1} component of the base current will be much smaller than the collector current. In addition, if the base width is small, then the number of electrons that recombine in the base will be small, and the i_{B2} component of the base current will also be much smaller than the collector current.

Common-Emitter Current Gain

In the transistor, the rate of flow of electrons and the resulting collector current are an exponential function of the B–E voltage, as is the resulting base current. This means that the collector current and the base current are linearly related. Therefore, we can write

$$\frac{i_C}{i_B} = \beta \tag{5.5}$$

or

$$i_B = I_{BO} e^{v_{BE}/V_T} = \frac{i_C}{\beta} = \frac{I_S}{\beta} e^{v_{BE}/V_T} \tag{5.6}$$

The parameter β is the **common-emitter current gain**[4] and is a key parameter of the bipolar transistor. In this idealized situation, β is considered to be a constant for any given transistor. The value of β is usually in the range of $50 < \beta < 300$, but it can be smaller or larger for special devices.

The value of β is highly dependent upon transistor fabrication techniques and process tolerances. Therefore, the value of β varies between transistor types and also between transistors of a given type, such as the discrete 2N2222. In any example or problem, we generally assume that β is a constant. However, it is important to realize that β can and does vary.

Figure 5.6 shows an npn bipolar transistor in a circuit. Because the emitter is the common connection, this circuit is referred to as a **common-emitter configuration.** When the transistor is biased in the forward-active mode, the B–E junction is forward

[4]Since we are considering the case of a transistor biased in the forward-active mode, the common–base current gain and common-emitter current gain parameters are often denoted as α_F and β_F, respectively. For ease of notation, we will simply define these parameters as α and β.

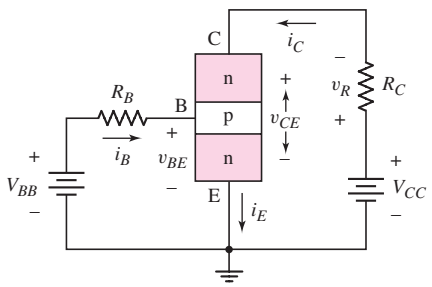

Figure 5.6 An npn transistor circuit in the common-emitter configuration. Shown are the current directions and voltage polarities for the transistor biased in the forward-active mode.

biased and the B–C junction is reverse biased. Using the piecewise linear model of a pn junction, we assume that the B–E voltage is equal to $V_{BE}(\text{on})$, the junction turn-on voltage. Since $V_{CC} = v_{CE} + i_C R_C$, the power supply voltage must be sufficiently large to keep the B–C junction reverse biased. The base current is established by V_{BB} and R_B, and the resulting collector current is $i_C = \beta i_B$.

If we set $V_{BB} = 0$, the B–E junction will have zero applied volts; therefore, $i_B = 0$, which implies that $i_C = 0$. This condition is called **cutoff.**

Current Relationships

If we treat the bipolar transistor as a single node, then, by Kirchhoff's current law, we have

$$i_E = i_C + i_B \tag{5.7}$$

If the transistor is biased in the forward-active mode, then

$$i_C = \beta i_B \tag{5.8}$$

Substituting Equation (5.8) into (5.7), we obtain the following relationship between the emitter and base currents:

$$i_E = (1 + \beta) i_B \tag{5.9}$$

Solving for i_B in Equation (5.8) and substituting into Equation (5.9), we obtain a relationship between the collector and emitter currents, as follows:

$$i_C = \left(\frac{\beta}{1 + \beta}\right) i_E \tag{5.10}$$

We can write $i_C = \alpha i_E$ so

$$\alpha = \frac{\beta}{1 + \beta} \tag{5.11}$$

The parameter α is called the common-base current gain and is always slightly less than 1. We may note that if $\beta = 100$, then $\alpha = 0.99$, so α is indeed close to 1. From Equation (5.11), we can state the common-emitter current gain in terms of the common-base current gain:

$$\beta = \frac{\alpha}{1 - \alpha} \tag{5.12}$$

Summary of Transistor Operation

We have presented a first-order model of the operation of the npn bipolar transistor biased in the forward-active region. The forward-biased B–E voltage, v_{BE}, causes an

exponentially related flow of electrons from the emitter into the base where they diffuse across the base region and are collected in the collector region. The collector current, i_C, is independent of the B–C voltage as long as the B–C junction is reverse biased. The collector, then, behaves as an ideal current source. The collector current is a fraction α of the emitter current, and the base current is a fraction $1/\beta$ of the collector current. If $\beta \gg 1$, then $\alpha \cong 1$ and $i_C \cong i_E$.

EXAMPLE 5.1

Objective: Calculate the collector and emitter currents, given the base current and current gain.

Assume a common-emitter current gain of $\beta = 150$ and a base current of $i_B = 15\ \mu$A. Also assume that the transistor is biased in the forward-active mode.

Solution: The relation between collector and base currents gives

$$i_C = \beta i_B = (150)(15\ \mu\text{A}) \Rightarrow 2.25\,\text{mA}$$

and the relation between emitter and base currents yields

$$i_E = (1+\beta)i_B = (151)(15\ \mu\text{A}) \Rightarrow 2.27\,\text{mA}$$

From Equation (5.11), the common-base current gain is

$$\alpha = \frac{\beta}{1+\beta} = \frac{150}{151} = 0.9934$$

Comment: For reasonable values of β, the collector and emitter currents are nearly equal, and the common-base current gain is nearly 1.

EXERCISE PROBLEM

Ex 5.1: An npn transistor is biased in the forward-active mode. The base current is $I_B = 8.50\ \mu$A and the emitter current is $I_E = 1.20$ mA. Determine β, α, and I_C. (Ans. $\beta = 140.2$, $\alpha = 0.9929$, $I_C = 1.1915$ mA)

5.1.3 pnp Transistor: Forward-Active Mode Operation

We have discussed the basic operation of the npn bipolar transistor. The complementary device is the pnp transistor. Figure 5.7 shows the flow of holes and electrons in a pnp device biased in the forward-active mode. Since the B–E junction is forward biased, the p-type emitter is positive with respect to the n-type base, holes flow from the emitter into the base, the holes diffuse across the base, and they are swept into the collector. The collector current is a result of this flow of holes.

Again, since the B–E junction is forward biased, the emitter current is an exponential function of the B–E voltage. Noting the direction of emitter current and the polarity of the foward-biased B–E voltage, we can write

$$i_E = I_{EO} e^{v_{EB}/V_T} \tag{5.13}$$

where v_{EB} is the voltage between the emitter and base, and now implies that the emitter is positive with respect to the base. We are again assuming the -1 term in the ideal diode equation is negligible.

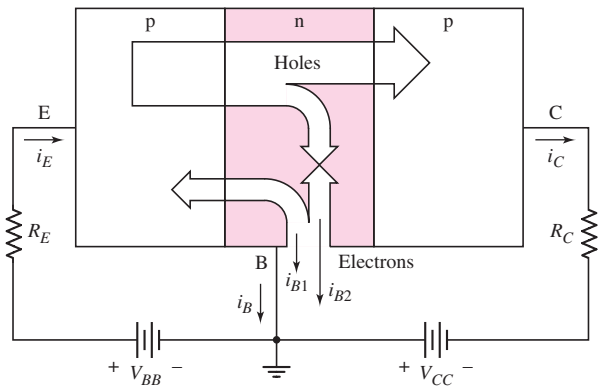

Figure 5.7 Electron and hole currents in a pnp bipolar transistor biased in the forward-active mode. Emitter, base, and collector currents are proportional to e^{v_{EB}/V_T}.

The collector current is an exponential function of the E–B voltage, and the direction is out of the collector terminal, which is opposite to that in the npn device. We can now write

$$i_C = \alpha i_E = I_S e^{v_{EB}/V_T} \tag{5.14}$$

where α is again the common-base current gain.

The base current in a pnp device is the sum of two components. The first component, i_{B1}, comes from electrons flowing from the base into the emitter as a result of the forward-biased E–B junction. We can then write $i_{B1} \propto \exp(v_{EB}/V_T)$. The second component, i_{B2}, comes from the flow of electrons supplied through the base terminal to replace those lost by recombination with the minority carrier holes injected into the base from the emitter. This component is proportional to the number of holes injected into the base, so $i_{B2} \propto \exp(v_{EB}/V_T)$. Therefore the total base current is $i_B = i_{B1} + i_{B2} \propto \exp(v_{EB}/V_T)$. The direction of the base current is out of the base terminal. Since the total base current in the pnp device is an exponential function of the E–B voltage, we can write

$$i_B = I_{BO} e^{v_{EB}/V_T} = \frac{i_C}{\beta} = \frac{I_S}{\beta} e^{v_{EB}/V_T} \tag{5.15}$$

The parameter β is also the common-emitter current gain of the pnp bipolar transistor.

The relationships between the terminal currents of the pnp transistor are exactly the same as those of the npn transistor and are summarized in Table 5.1 in the next section. Also the relationships between β and α are the same as given in Equations (5.11) and (5.12).

5.1.4 Circuit Symbols and Conventions

The block diagram and conventional circuit symbol of an npn bipolar transistor are shown in Figures 5.8(a) and 5.8(b). The arrowhead in the circuit symbol is always placed on the emitter terminal, and it indicates the direction of the emitter current. For the npn device, this direction is out of the emitter. The simplified block diagram and conventional circuit symbol of a pnp bipolar transistor are shown in Figures 5.9(a) and 5.9(b). Here, the arrowhead on the emitter terminal indicates that the direction of the emitter current is into the emitter.

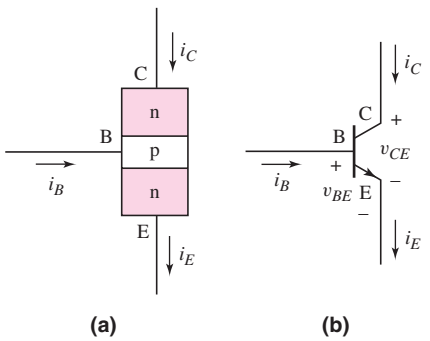

Figure 5.8 npn bipolar transistor: (a) simple block diagram and (b) circuit symbol. Arrow is on the emitter terminal and indicates the direction of emitter current (out of emitter terminal for the npn device).

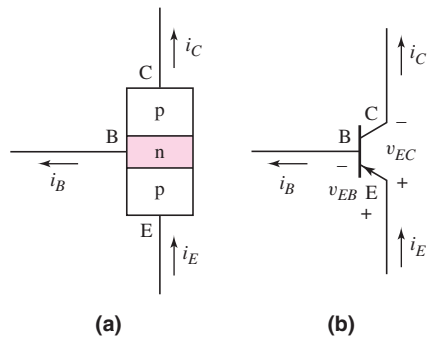

Figure 5.9 pnp bipolar transistor: (a) simple block diagram and (b) circuit symbol. Arrow is on the emitter terminal and indicates the direction of emitter current (into emitter terminal for the pnp device).

Table 5.1 Summary of the bipolar current–voltage relationships in the active region

npn	pnp
$i_C = I_S e^{v_{BE}/V_T}$	$i_C = I_S e^{v_{EB}/V_T}$
$i_E = \frac{i_C}{\alpha} = \frac{I_S}{\alpha} e^{v_{BE}/V_T}$	$i_E = \frac{i_C}{\alpha} = \frac{I_S}{\alpha} e^{v_{EB}/V_T}$
$i_B = \frac{i_C}{\beta} = \frac{I_S}{\beta} e^{v_{BE}/V_T}$	$i_B = \frac{i_C}{\beta} = \frac{I_S}{\beta} e^{v_{EB}/V_T}$
For both transistors	
$i_E = i_C + i_B$	$i_C = \beta i_B$
$i_E = (1+\beta) i_B$	$i_C = \alpha i_E = \left(\frac{\beta}{1+\beta}\right) i_E$
$\alpha = \frac{\beta}{1+\beta}$	$\beta = \frac{\alpha}{1-\alpha}$

Referring to the circuit symbols given for the npn (Figure 5.8(b)) and pnp (Figure 5.9(b)) transistors showing current directions and voltage polarities, we can summarize the current–voltage relationships as given in Table 5.1.

Figure 5.10(a) shows a common-emitter circuit with an npn transistor. The figure includes the transistor currents, and the base-emitter (B–E) and collector–emitter

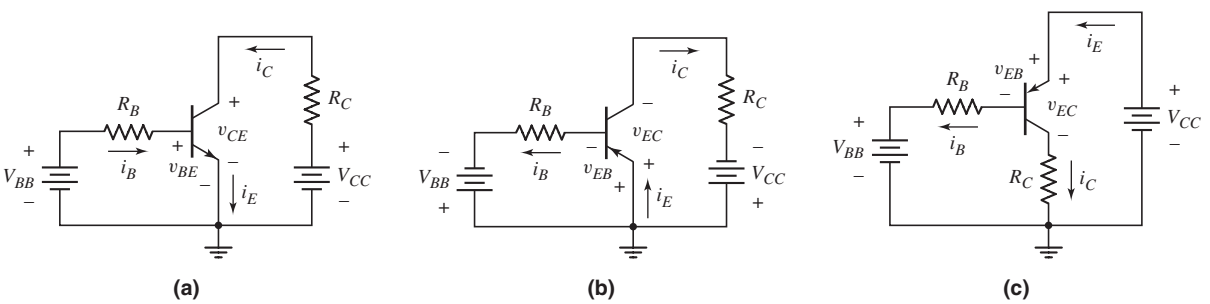

Figure 5.10 Common-emitter circuits: (a) with an npn transistor, (b) with a pnp transistor, and (c) with a pnp transistor biased with a positive voltage source

(C–E) voltages. Figure 5.10(b) shows a common-emitter circuit with a pnp bipolar transistor. Note the different current directions and voltage polarities in the two circuits. A more usual circuit configuration using the pnp transistor is shown in Figure 5.10(c). This circuit allows positive voltage supplies to be used.

Test Your Understanding

TYU 5.1 (a) The common-emitter current gains of two transistors are $\beta = 60$ and $\beta = 150$. Determine the corresponding common-base current gains. (b) The common-base current gains of two transistors are $\alpha = 0.9820$ and $\alpha = 0.9925$. Determine the corresponding common-emitter current gains. (Ans. (a) $\alpha = 0.9836$, $\alpha = 0.9934$; (b) $\beta = 54.6$, $\beta = 132.3$)

TYU 5.2 An npn transistor is biased in the forward-active mode. The base current is $I_B = 5.0\,\mu\text{A}$ and the collector current is $I_C = 0.62\,\text{mA}$. Determine I_E, β, and α. (Ans. $I_E = 0.625\,\text{mA}$, $\beta = 124$, and $\alpha = 0.992$)

TYU 5.3 The emitter current in a pnp transistor biased in the forward-active mode is $I_E = 1.20\,\text{mA}$. The common-base current gain of the transistor is $\alpha = 0.9915$. Determine β, I_B, and I_C. (Ans. $\beta = 117$, $I_B = 10.2\,\mu\text{A}$, $I_C = 1.19\,\text{mA}$)

5.1.5 Current–Voltage Characteristics

Figures 5.11(a) and 5.11(b) are **common-base circuit configurations** for an npn and a pnp bipolar transistor, respectively. The current sources provide the emitter current. Previously, we stated that the collector current i_C was nearly independent of the C–B voltage as long as the B–C junction was reverse biased. When the B–C junction becomes forward biased, the transistor is no longer in the forward-active mode, and the collector and emitter currents are no longer related by $i_C = \alpha i_E$.

Figure 5.12 shows the typical common-base current–voltage characteristics. When the collector–base junction is reverse biased, then for constant values of emitter

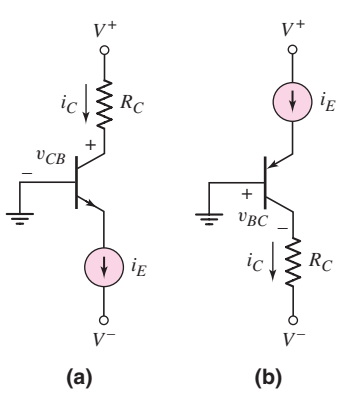

Figure 5.11 Common-base circuit configuration with constant current source biasing: (a) an npn transistor and (b) a pnp transistor

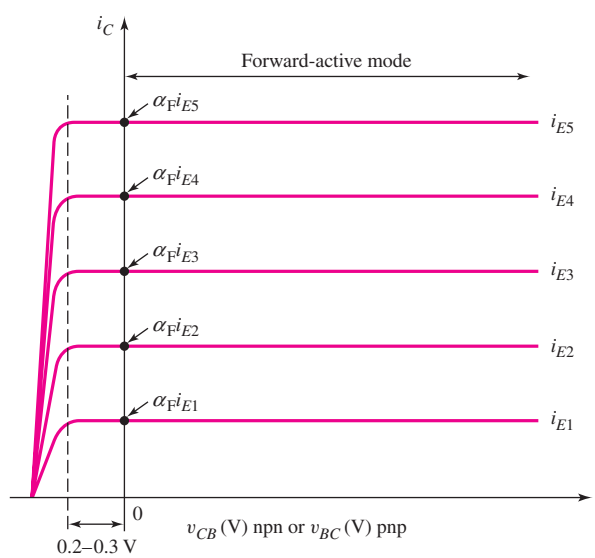

Figure 5.12 Transistor current–voltage characteristics of the common-base circuit

current, the collector current is nearly equal to i_E. These characteristics show that the common-base device is nearly an ideal constant-current source.

The C–B voltage can be varied by changing the V^+ voltage (Figure 5.11(a)) or the V^- voltage (Figure 5.11(b)). When the collector–base junction becomes forward biased in the range of 0.2 and 0.3 V, the collector current i_C is still essentially equal to the emitter current i_E. In this case, the transistor is still basically biased in the forward-active mode. However, as the forward-bias C–B voltage increases, the linear relationship between the collector and emitter currents is no longer valid, and the collector current very quickly drops to zero.

The common-emitter circuit configuration provides a slightly different set of current–voltage characteristics, as shown in Figure 5.13. For these curves, the collector current is plotted against the collector–emitter voltage, for various constant values of the base current. These curves are generated from the common-emitter circuits shown in Figure 5.10. In this circuit, the V_{BB} source forward biases the B–E junction and controls the base current i_B. The C–E voltage can be varied by changing V_{CC}.

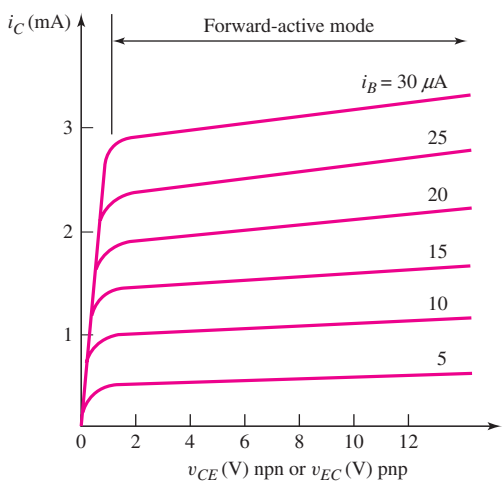

Figure 5.13 Transistor current–voltage characteristics of the common-emitter circuit

In the npn device, in order for the transistor to be biased in the forward-active mode, the B–C junction must be zero or reverse biased, which means that V_{CE} must be greater than approximately $V_{BE}(\text{on})$.[5] For $V_{CE} > V_{BE}(\text{on})$, there is a finite slope to the curves. If, however, $V_{CE} < V_{BE}(\text{on})$, the B–C junction becomes forward biased, the transistor is no longer in the forward-active mode, and the collector current very quickly drops to zero.

Figure 5.14 shows an exaggerated view of the current–voltage characteristics plotted for constant values of the B–E voltage. The curves are theoretically linear with respect to the C–E voltage in the forward-active mode. The slope in these characteristics is due to an effect called base-width modulation that was first analyzed by J. M. Early. The phenomenon is generally called the *Early effect*. When the curves are extrapolated to zero current, they meet at a point on the negative voltage axis, at $v_{CE} = -V_A$. The voltage V_A is a positive quantity called the **Early voltage.** Typical

[5]Even though the collector current is essentially equal to the emitter current when the B–C junction becomes slightly forward biased, as was shown in Figure 5.12, the transistor is said to be biased in the forward-active mode when the B–C junction is zero or reverse biased.

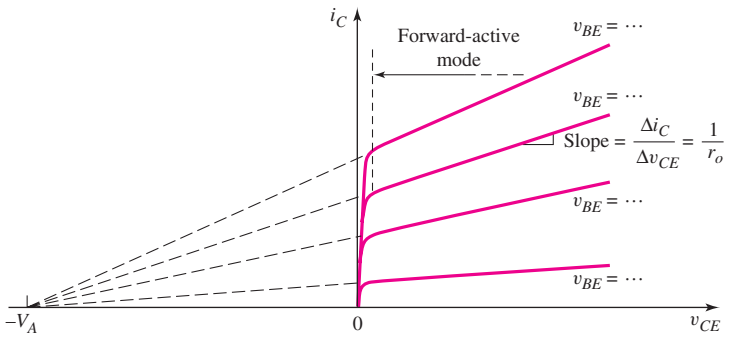

Figure 5.14 Current-voltage characteristics for the common-emitter circuit, showing the Early voltage and the finite output resistance, r_o, of the transistor

values of V_A are in the range $50 < V_A < 300$ V. For a pnp transistor, this same effect is true except the voltage axis is v_{EC}.

For a given value of v_{BE} in an npn transistor, if v_{CE} increases, the reverse-bias voltage on the collector–base junction increases, which means that the width of the B–C space-charge region also increases. This in turn reduces the neutral base width W (see Figure 5.4). A decrease in the base width causes the gradient in the minority carrier concentration to increase, which increases the diffusion current through the base. The collector current then increases as the C–E voltage increases.

The linear dependence of i_C versus v_{CE} in the forward-active mode can be described by

$$i_C = I_S(e^{v_{BE}/V_T}) \cdot \left(1 + \frac{v_{CE}}{V_A}\right) \tag{5.16}$$

where I_S is assumed to be constant.

In Figure 5.14, the nonzero slope of the curves indicates that the **output resistance** r_o looking into the collector is finite. This output resistance is determined from

$$\frac{1}{r_o} = \left.\frac{\partial i_C}{\partial v_{CE}}\right|_{v_{BE}=\text{const.}} \tag{5.17}$$

Using Equation (5.16), we can show that

$$r_o \cong \frac{V_A}{I_C} \tag{5.18}$$

where I_C is the quiescent collector current when v_{BE} is a constant and v_{CE} is small compared to V_A.

In most cases, the dependence of i_C on v_{CE} is not critical in the dc analysis or design of transistor circuits. However, the finite output resistance r_o may significantly affect the amplifier characteristics of such circuits. This effect is examined more closely in Chapter 6 of this text.

Test Your Understanding

TYU 5.4 The output resistance of a bipolar transistor is $r_o = 225\ \text{k}\Omega$ at $I_C = 0.8$ mA. (a) Determine the Early voltage. (b) Using the results of part (a), find r_o at (i) $I_C = 0.08$ mA and (ii) $I_C = 8$ mA. (Ans. (a) $V_A = 180$ V; (b) (i) $r_o = 2.25\ \text{M}\Omega$, (ii) $r_o = 22.5\ \text{k}\Omega$)

TYU 5.5 Assume that $I_C = 1$ mA at $V_{CE} = 1$ V, and that V_{BE} is held constant. Determine I_C at $V_{CE} = 10$ V if: (a) $V_A = 75$ V; and (b) $V_A = 150$ V. (Ans. $I_C =$ 1.12 mA, 1.06 mA)

5.1.6 Nonideal Transistor Leakage Currents and Breakdown Voltage

In discussing the current–voltage characteristics of the bipolar transistor in the previous sections, two topics were ignored: leakage currents in the reverse-biased pn junctions and breakdown voltage effects.

Leakage Currents

In the common-base circuits in Figure 5.11, if we set the current source $i_E = 0$, transistors will be cut off, but the B–C junctions will still be reverse biased. A reverse-bias leakage current exists in these junctions, and this current corresponds to the reverse-bias saturation current in a diode, as described in Chapter 1. The direction of these reverse-bias leakage currents is the same as that of the collector currents. The term I_{CBO} is the collector leakage current in the common-base configuration, and is the collector-base leakage current when the emitter is an open circuit. This leakage current is shown in Figure 5.15(a).

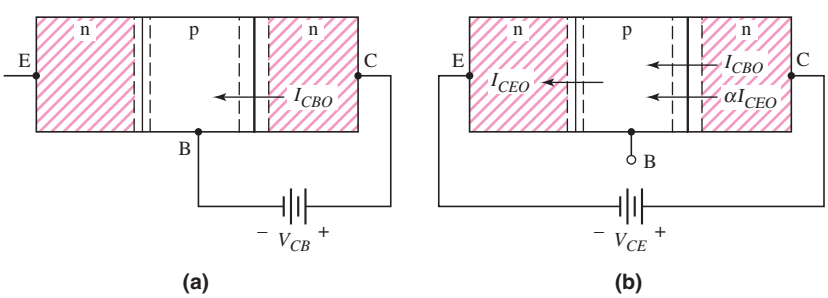

Figure 5.15 Block diagram of an npn transistor in an (a) open-emitter configuration showing the junction leakage current I_{CBO} and (b) open-base configuration showing the leakage current I_{CEO}

Another leakage current can exist between the emitter and collector with the base terminal an open circuit. Figure 5.15(b) is a block diagram of an npn transistor in which the base is an open circuit ($i_B = 0$). The current component I_{CBO} is the normal leakage current in the reverse-biased B–C pn junction. This current component causes the base potential to increase, which forward biases the B–E junction and induces the B–E current I_{CEO}. The current component αI_{CEO} is the normal collector current resulting from the emitter current I_{CEO}. We can write

$$I_{CEO} = \alpha I_{CEO} + I_{CBO} \tag{5.19(a)}$$

or

$$I_{CEO} = \frac{I_{CBO}}{1-\alpha} \cong \beta I_{CBO} \tag{5.19(b)}$$

This relationship indicates that the open-base configuration produces different characteristics than the open-emitter configuration.

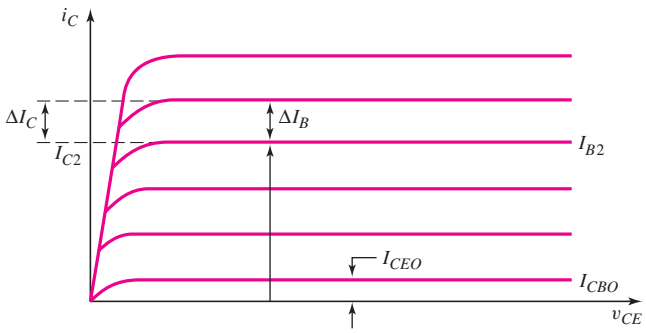

Figure 5.16 Transistor current–voltage characteristics for the common-emitter circuit including leakage currents. The dc beta and ac beta for the transistor can be determined from this set of characteristics. The Early voltage for this set of characteristics is assumed to be $V_A = \infty$.

When the transistor is biased in the forward-active mode, the various leakage currents still exist. Common-emitter current–voltage characteristics are shown in Figure 5.16, in which the leakage current has been included. A dc beta or dc common-emitter current gain can be defined, for example, as

$$\beta_{\text{dc}} = \frac{I_{C2}}{I_{B2}} \tag{5.20}$$

where the collector current I_{C2} includes the leakage current as shown in the figure. An ac β is defined as

$$\beta_{\text{ac}} = \frac{\Delta I_C}{\Delta I_{B|V_{CE}=\text{const.}}} \tag{5.21}$$

This definition of beta excludes the leakage current as shown in the figure.

If the leakage currents are negligible, the two values of beta are equal. We will assume in the remainder of this text that the leakage currents can be neglected and beta can simply be denoted as β as previously defined.

Breakdown Voltage: Common-Base Characteristics

The common-base current–voltage characteristics shown in Figure 5.12 are ideal in that breakdown is not shown. Figure 5.17 shows the same i_C versus v_{CB} characteristics with the breakdown voltage.

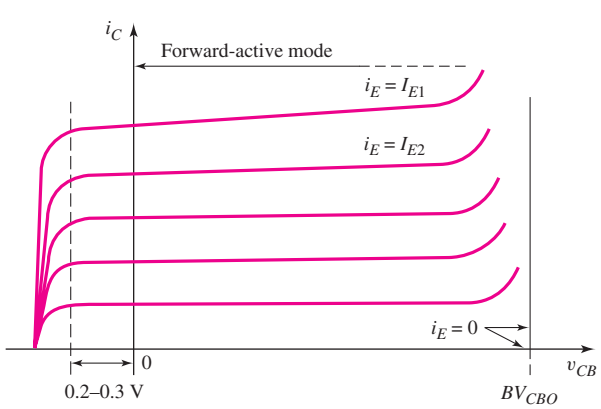

Figure 5.17 The i_C versus v_{CB} common-base characteristics, showing the collector–base junction breakdown

Consider the curve for $i_E = 0$ (the emitter terminal is effectively an open circuit). The collector–base junction breakdown voltage is indicated as BV_{CBO}. This is a simplified figure in that it shows breakdown occurring abruptly at BV_{CBO}. For the curves in which $i_E > 0$, breakdown actually begins earlier. The carriers flowing across the junction initiate the breakdown avalanche process at somewhat lower voltages.

Breakdown Voltage: Common-Emitter Characteristics

Figure 5.18 shows the i_C versus v_{CE} characteristics of an npn transistor, for various constant base currents, and an ideal breakdown voltage of BV_{CEO}. The value of BV_{CEO} is less than the value of BV_{CBO} because BV_{CEO} includes the effects of the transistor action, while BV_{CBO} does not. This same effect was observed in the I_{CEO} leakage current.

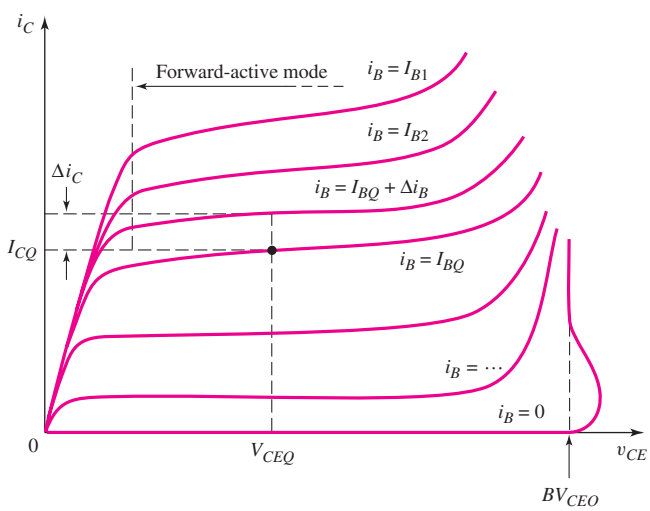

Figure 5.18 Common-emitter characteristics showing breakdown effects

The breakdown voltage characteristics for the two configurations are also different. The breakdown voltage for the open-base case is given by

$$BV_{CEO} = \frac{BV_{CBO}}{\sqrt[n]{\beta}} \tag{5.22}$$

where n is an empirical constant usually in the range of 3 to 6.

EXAMPLE 5.2

Objective: Calculate the breakdown voltage of a transistor connected in the open-base configuration.

Assume that the transistor current gain is $\beta = 100$ and that the breakdown voltage of the B–C junction is $BV_{CBO} = 120$ V.

Solution: If we assume an empirical constant of $n = 3$, we have

$$BV_{CEO} = \frac{BV_{CBO}}{\sqrt[n]{\beta}} = \frac{120}{\sqrt[3]{100}} = 25.9\,\text{V}$$

Comment: The breakdown voltage of the open-base configuration is substantially less than that of the C–B junction. This represents a worst-case condition, which must be considered in any circuit design.

Design Pointer: The designer must be aware of the breakdown voltage of the specific transistors used in a circuit, since this will be a limiting factor in the size of the dc bias voltages that can be used.

EXERCISE PROBLEM

Ex 5.2: The open-emitter breakdown voltage is $BV_{CBO} = 200$ V, the current gain is $\beta = 120$, and the empirical constant is $n = 3$. Determine BV_{CEO}. (Ans. 40.5 V)

Breakdown may also occur in the B–E junction if a reverse-bias voltage is applied to that junction. The junction breakdown voltage decreases as the doping concentrations increase. Since the emitter doping concentration is usually substantially larger than the doping concentration in the collector, the B–E junction breakdown voltage is normally much smaller than that of the B–C junction. Typical B–E junction breakdown voltage values are in the range of 6 to 8 V.

Test Your Understanding

TYU 5.6 A particular transistor circuit requires a minimum open-base breakdown voltage of $BV_{CEO} = 30$ V. If $\beta = 100$ and $n = 3$, determine the minimum required value of BV_{CBO}. (Ans. 139 V)

5.2 DC ANALYSIS OF TRANSISTOR CIRCUITS

Objective: • Understand and become familiar with the dc analysis and design techniques of bipolar transistor circuits.

We've considered the basic transistor characteristics and properties. We can now start analyzing and designing the dc biasing of bipolar transistor circuits. A primary purpose of the rest of the chapter is to become familiar and comfortable with the bipolar transistor and transistor circuits. The dc biasing of transistors, the focus of this chapter, is an important part of designing bipolar amplifiers, the focus of the next chapter.

The piecewise linear model of a pn junction can be used for the dc analysis of bipolar transistor circuits. We will first analyze the common-emitter circuit and introduce the load line for that circuit. We will then look at the dc analysis of other bipolar transistor circuit configurations. Since a transistor in a linear amplifier must be biased in the forward-active mode, we emphasize, in this section, the analysis and design of circuits in which the transistor is biased in this mode.

5.2.1 Common-Emitter Circuit

One of the basic transistor circuit configurations is called the **common-emitter circuit.** Figure 5.19(a) shows one example of a common-emitter circuit. The emitter terminal is obviously at ground potential. This circuit configuration will appear in many amplifiers that will be considered in Chapter 6.

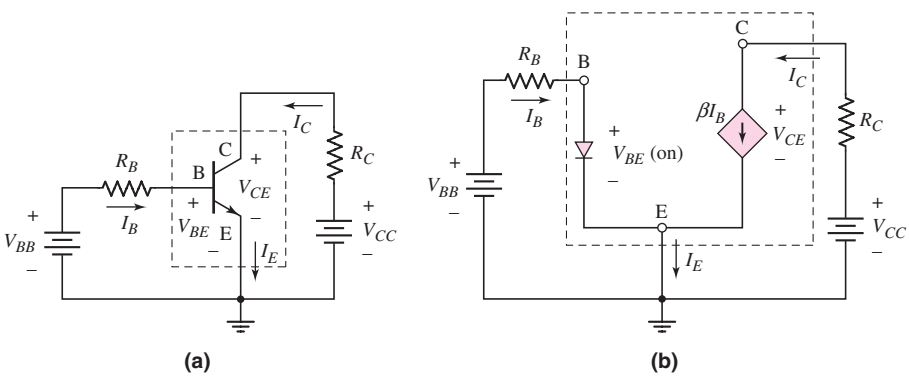

Figure 5.19 (a) Common-emitter circuit with npn transistor and (b) dc equivalent circuit. Transistor equivalent circuit is shown within the dotted lines with piecewise linear transistor parameters.

Figure 5.19(a) shows a common-emitter circuit with an npn transistor, and Figure 5.19(b) shows the dc equivalent circuit. We will assume that the B–E junction is forward biased, so the voltage drop across that junction is the cut-in or turn-on voltage $V_{BE}(\text{on})$. When the transistor is biased in the forward-active mode, the collector current is represented as a dependent current source that is a function of the base current. We are neglecting the reverse-biased junction leakage current and the Early effect in this case. In the following circuits, we will be considering dc currents and voltages, so the dc notation for these parameters will be used.

The base current is

$$I_B = \frac{V_{BB} - V_{BE}(\text{on})}{R_B} \tag{5.23}$$

Implicit in Equation (5.23) is that $V_{BB} > V_{BE}(\text{on})$, which means that $I_B > 0$. When $V_{BB} < V_{BE}(\text{on})$, the transistor is cut off and $I_B = 0$.

In the collector–emitter portion of the circuit, we can write

$$I_C = \beta I_B \tag{5.24}$$

and

$$V_{CC} = I_C R_C + V_{CE} \tag{5.25(a)}$$

or

$$V_{CE} = V_{CC} - I_C R_C \tag{5.25(b)}$$

In Equation (5.25(b)), we are also implicitly assuming that $V_{CE} > V_{BE}(\text{on})$, which means that the B–C junction is reverse biased and the transistor is biased in the forward-active mode.

Considering Figure 5.19(b), we can see that the power dissipated in the transistor is given by

$$P_T = I_B V_{BE}(\text{on}) + I_C V_{CE} \qquad \textbf{(5.26(a))}$$

In most cases, $I_C \gg I_B$ and $V_{CE} > V_{BE}(\text{on})$ so that a good first approximation of the power dissipated is given as

$$P_T \cong I_C V_{CE} \qquad \textbf{(5.26(b))}$$

The principal condition where this approximation is not valid is for a transistor biased in the saturation mode (discussed later).

EXAMPLE 5.3

Objective: Calculate the base, collector, and emitter currents and the C–E voltage for a common-emitter circuit. Calculate the transistor power dissipation.

For the circuit shown in Figure 5.19(a), the parameters are: $V_{BB} = 4$ V, $R_B = 220$ kΩ, $R_C = 2$ kΩ, $V_{CC} = 10$ V, $V_{BE}(\text{on}) = 0.7$ V, and $\beta = 200$. Figure 5.20(a) shows the circuit without explicitly showing the voltage sources.

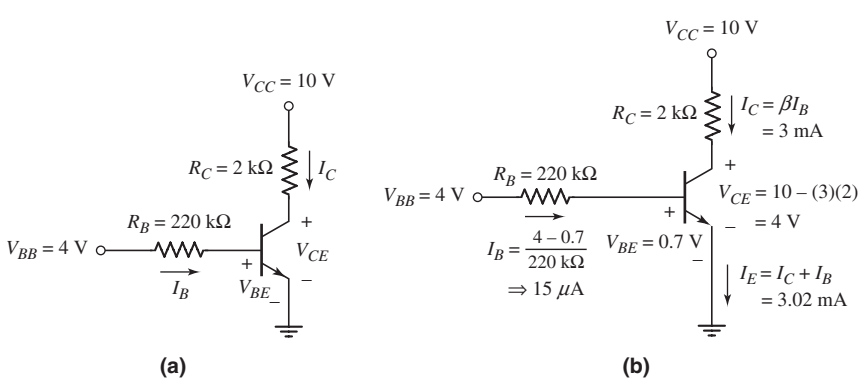

Figure 5.20 Circuit for Example 5.3: (a) circuit and (b) circuit showing current and voltage values

Solution: Referring to Figure 5.20(b), the base current is found as

$$I_B = \frac{V_{BB} - V_{BE}(\text{on})}{R_B} = \frac{4 - 0.7}{220} \Rightarrow 15\ \mu\text{A}$$

The collector current is

$$I_C = \beta I_B = (200)(15\ \mu\text{A}) \Rightarrow 3\ \text{mA}$$

and the emitter current is

$$I_E = (1 + \beta) \cdot I_B = (201)(15\mu\text{A}) \Rightarrow 3.02\,\text{mA}$$

From Equation (5.25(b)), the collector-emitter voltage is

$$V_{CE} = V_{CC} - I_C R_C = 10 - (3)(2) = 4\,\text{V}$$

The power dissipated in the transistor is found to be

$$P_T = I_B V_{BE}(\text{on}) + I_C V_{CE} = (0.015)(0.7) + (3)(4) \cong I_C V_{CE}$$

or

$$P_T \cong 12 \text{ mW}$$

Comment: Since $V_{BB} > V_{BE}(\text{on})$ and $V_{CE} > V_{BE}(\text{on})$, the transistor is indeed biased in the forward-active mode. As a note, in an actual circuit, the voltage across a B–E junction may not be exactly 0.7 V, as we have assumed using the piecewise linear approximation. This may lead to slight inaccuracies between the calculated currents and voltages and the measured values. Also note that, if we take the difference between I_E and I_C, which is the base current, we obtain $I_B = 20\,\mu\text{A}$ rather than $15\,\mu\text{A}$. The difference is the result of roundoff error in the emitter current.

EXERCISE PROBLEM

Ex 5.3: The circuit elements in Figure 5.20(a) are changed to $V_{CC} = 3.3$ V, $V_{BB} = 2$ V, $R_C = 3.2\,\text{k}\Omega$, and $R_B = 430\,\text{k}\Omega$. The transistor parameters are $\beta = 150$ and $V_{BE} = 0.7$ V. Calculate I_B, I_C, V_{CE}, and the power dissipated in the transistor. (Ans. $I_B = 3.02\,\mu\text{A}$, $I_C = 0.453$ mA, $V_{CE} = 1.85$ V, $P = 0.838$ mW)

Figure 5.21(a) shows a common-emitter circuit with a pnp bipolar transistor, and Figure 5.21(b) shows the dc equivalent circuit. In this circuit, the emitter is at ground potential, which means that the polarities of the V_{BB} and V_{CC} power supplies must be reversed compared to those in the npn circuit. The analysis proceeds exactly as before, and we can write

$$I_B = \frac{V_{BB} - V_{EB}(\text{on})}{R_B} \tag{5.27}$$

$$I_C = \beta I_B \tag{5.28}$$

and

$$V_{EC} = V_{CC} - I_C R_C \tag{5.29}$$

We can see that Equations (5.27), (5.28), and (5.29) for the pnp bipolar transistor in the common-emitter configuration are exactly the same as Equations (5.23), (5.24), and (5.25(b)) for the npn bipolar transistor in a similar circuit, if we properly define the current directions and voltage polarities.

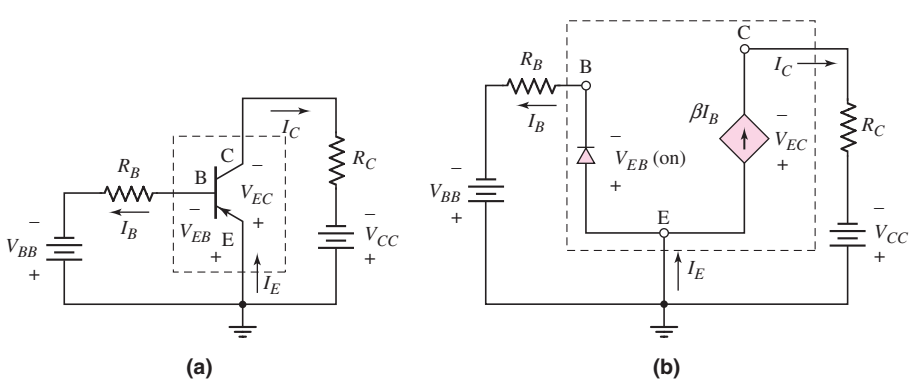

Figure 5.21 (a) Common-emitter circuit with pnp transistor and (b) dc equivalent circuit. Transistor equivalent circuit is shown within the dotted lines with piecewise linear transistor parameters.

In many cases, the pnp bipolar transistor will be reconfigured in a circuit so that positive voltage sources, rather than negative ones, can be used. We see this in the following example.

EXAMPLE 5.4

Objective: Analyze the common-emitter circuit with a pnp transistor.

For the circuit shown in Figure 5.22(a), the parameters are: $V_{BB} = 1.5$ V, $R_B = 580$ kΩ, $V^+ = 5$ V, $V_{EB}(\text{on}) = 0.6$ V, and $\beta = 100$. Find I_B, I_C, I_E, and R_C such that $V_{EC} = \left(\frac{1}{2}\right)V^+$.

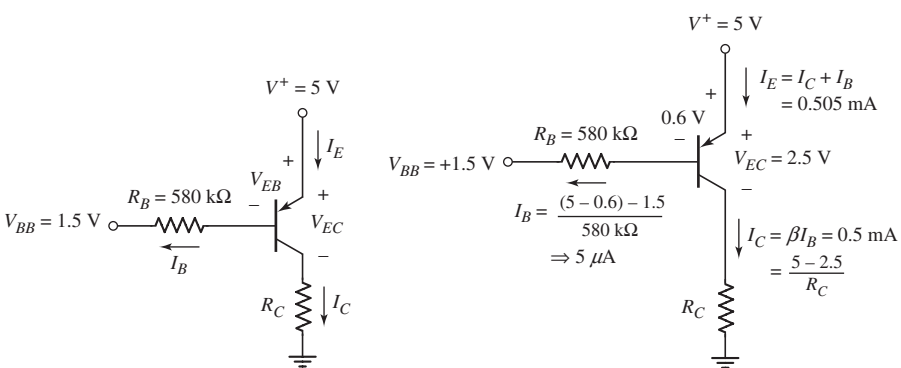

Figure 5.22 Circuit for Example 5.4; (a) circuit and (b) circuit showing current and voltage values

Solution: Writing a Kirchhoff voltage law equation around the E–B loop, we find the base current to be

$$I_B = \frac{V^+ - V_{EB}(\text{on}) - V_{BB}}{R_B} = \frac{5 - 0.6 - 1.5}{580} \Rightarrow 5\mu\text{A}$$

The collector current is

$$I_C = \beta I_B = (100)(5\mu\text{A}) \Rightarrow 0.5\,\text{mA}$$

and the emitter current is

$$I_E = (1 + \beta)I_B = (101)(5\mu\text{A}) \Rightarrow 0.505\,\text{mA}$$

For a C–E voltage of $V_{EC} = \frac{1}{2}V^+ = 2.5$ V, R_C is

$$R_C = \frac{V^+ - V_{EC}}{I_C} = \frac{5 - 2.5}{0.5} = 5\,\text{k}\Omega$$

Comment: In this case, the difference between V^+ and V_{BB} is greater than the transistor turn-on voltage, or $(V^+ - V_{BB}) > V_{EB}(\text{on})$. Also, because $V_{EC} > V_{EB}(\text{on})$, the pnp bipolar transistor is biased in the forward-active mode.

Discussion: In this example, we used an emitter-base turn-on voltage of $V_{EB}(\text{on}) = 0.6$ V, whereas previously we used a value of 0.7 V. We must keep in mind that the turn-on voltage is an approximation and the actual base–emitter voltage will depend on the type of transistor used and the current level. In most situations, choosing a value of 0.6 V or 0.7 V will make only minor differences. However, most people tend to use the value of 0.7 V.

EXERCISE PROBLEM

Ex 5.4: The circuit elements in Figure 5.22(a) are $V^+ = 3.3$ V, $V_{BB} = 1.2$ V, $R_B = 400\,\text{k}\Omega$, and $R_C = 5.25\,\text{k}\Omega$. The transistor parameters are $\beta = 80$ and $V_{EB}(\text{on}) = 0.7$ V. Determine I_B, I_C, and V_{EC}. (Ans. $I_B = 3.5\,\mu\text{A}$, $I_C = 0.28$ mA, $V_{EC} = 1.83$ V)

The dc equivalent circuits, such as those given in Figures 5.19(b) and 5.21(b), are useful initially in analyzing transistor circuits. From this point on, however, we will not explicitly draw the equivalent circuit. We will simply analyze the circuit using the transistor circuit symbols, as in Figures 5.20 and 5.22.

COMPUTER ANALYSIS EXERCISE

PS 5.1: (a) Verify the results of Example 5.3 with a PSpice analysis. Use a standard transistor. (b) Repeat the analysis for $R_B = 180\,\text{k}\Omega$. (c) Repeat the analysis for $R_B = 260\,\text{k}\Omega$. What can be said about R_B limiting the base current?

5.2.2 Load Line and Modes of Operation

The load line can help us visualize the characteristics of a transistor circuit. For the common-emitter circuit in Figure 5.20(a), we can use a graphical technique for both the B–E and C–E portions of the circuit. Figure 5.23(a) shows the piecewise linear characteristics for the B–E junction and the input load line. The input load line is

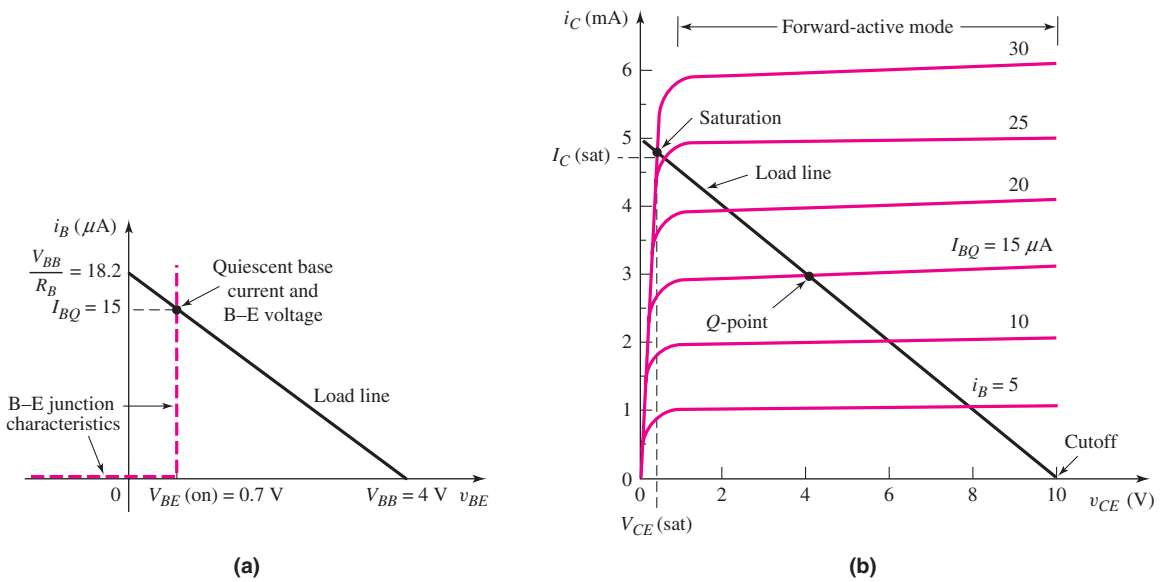

Figure 5.23 (a) Base–emitter junction piecewise linear i–v characteristics and the input load line, and (b) common-emitter transistor characteristics and the collector–emitter load line showing the Q-point for the circuit shown in Example 5.3 (Figure 5.20)

obtained from Kirchhoff's voltage law equation around the B–E loop, written as follows:

$$I_B = \frac{V_{BB}}{R_B} - \frac{V_{BE}}{R_B} \tag{5.30}$$

Both the load line and the quiescent base current change as either or both V_{BB} and R_B change. The load line in Figure 5.23(a) is essentially the same as the load line characteristics for diode circuits, as shown in Chapter 1.

For the C–E portion of the circuit in Figure 5.20(a), the load line is found by writing Kirchhoff's voltage law equation around the C–E loop. We obtain

$$V_{CE} = V_{CC} - I_C R_C \tag{5.31(a)}$$

which can be written in the form

$$I_C = \frac{V_{CC}}{R_C} - \frac{V_{CE}}{R_C} = 5 - \frac{V_{CE}}{2}(\text{mA}) \tag{5.31(b)}$$

Equation (5.31(b)) is the load line equation, showing a linear relationship between the collector current and collector–emitter voltage. Since we are considering the dc analysis of the transistor circuit, this relationship represents the dc load line. The ac load line is presented in the next chapter.

Figure 5.23(b) shows the transistor characteristics for the transistor in Example 5.3, with the load line superimposed on the transistor characteristics. The two end points of the load line are found by setting $I_C = 0$, yielding $V_{CE} = V_{CC} = 10$ V, and by setting $V_{CE} = 0$, yielding $I_C = V_{CC}/R_C = 5$ mA.

The quiescent point, or Q-point, of the transistor is given by the dc collector current and the collector–emitter voltage. The Q-point is the intersection of the load line and the I_C versus V_{CE} curve corresponding to the appropriate base current. The Q-point also represents the simultaneous solution to two expressions. The load line is useful in visualizing the bias point of the transistor. In the figure, the Q-point shown is for the transistor in Example 5.3.

As previously stated, if the power supply voltage in the base circuit is smaller than the turn-on voltage, then $V_{BB} < V_{BE}(\text{on})$ and $I_B = I_C = 0$, and the transistor is in the cutoff mode. In this mode, all transistor currents are zero, neglecting leakage currents, and for the circuit shown in Figure 5.20(a), $V_{CE} = V_{CC} = 10$ V.

As V_{BB} increases ($V_{BB} > V_{BE}(\text{on})$), the base current I_B increases and the Q-point moves up the load line. As I_B continues to increase, a point is reached where the collector current I_C can no longer increase. At this point, the transistor is biased in the **saturation mode;** that is, the transistor is said to be in saturation. The B–C junction becomes forward biased, and the relationship between the collector and base currents is no longer linear. The transistor C–E voltage in saturation, $V_{CE}(\text{sat})$, is less than the B–E cut-in voltage. The forward-biased B–C voltage is always less than the forward-biased B–E voltage, so the C–E voltage in saturation is a small positive value. Typically, $V_{CE}(\text{sat})$ is in the range of 0.1 to 0.3 V.

EXAMPLE 5.5

Objective: Calculate the currents and voltages in a circuit when the transistor is driven into saturation.

For the circuit shown in Figure 5.24, the transistor parameters are: $\beta = 100$, and $V_{BE}(\text{on}) = 0.7$ V. If the transistor is biased in saturation, assume $V_{CE}(\text{sat}) = 0.2$ V.

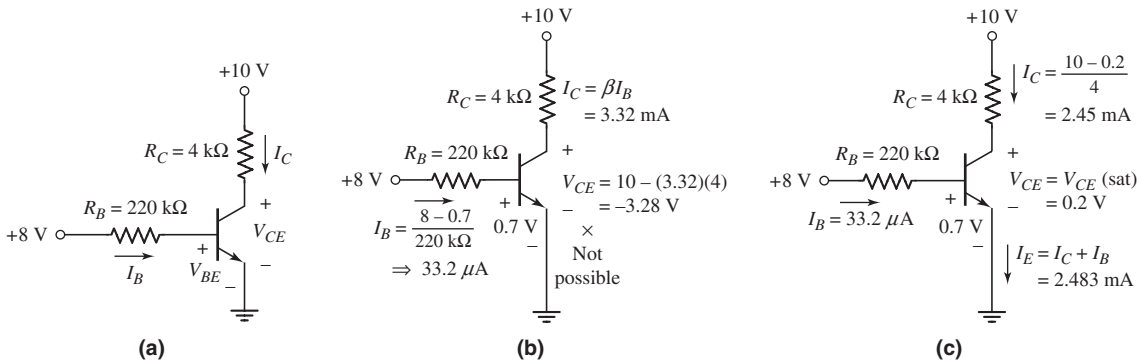

Figure 5.24 Circuit for Example 5.5: (a) circuit; (b) circuit showing current and voltage values, assuming the transistor is biased in the forward-active mode (an incorrect assumption); and (c) circuit showing current and voltage values, assuming the transistor is biased in the saturation mode (correct assumption)

Solution: Since +8 V is applied to the input side of R_B, the base–emitter junction is certainly forward biased, so the transistor is turned on. The base current is

$$I_B = \frac{V_{BB} - V_{BE}(\text{on})}{R_B} = \frac{8 - 0.7}{220} \Rightarrow 33.2\ \mu\text{A}$$

If we first assume that the transistor is biased in the active region, then the collector current is

$$I_C = \beta I_B = (100)(33.2\ \mu\text{A}) \Rightarrow 3.32\ \text{mA}$$

The collector–emitter voltage is then

$$V_{CE} = V_{CC} - I_C R_C = 10 - (3.32)(4) = -3.28\ \text{V}$$

However, the collector–emitter voltage of the npn transistor in the common-emitter configuration shown in Figure 5.24(a) cannot be negative. Therefore, our initial assumption of the transistor being biased in the forward-active mode is incorrect. Instead, the transistor must be biased in saturation.

As given in the "objective" statement, set $V_{CE}(\text{sat}) = 0.2$ V. The collector current is

$$I_C = I_C(\text{sat}) = \frac{V_{CC} - V_{CE}(\text{sat})}{R_C} = \frac{10 - 0.2}{4} = 2.45\ \text{mA}$$

Assuming that the B–E voltage is still equal to $V_{BE}(\text{on}) = 0.7$ V, the base current is $I_B = 33.2\ \mu$A, as previously determined. If we take the ratio of collector current to base current, then

$$\frac{I_C}{I_B} = \frac{2.45}{0.0332} = 74 < \beta$$

The emitter current is

$$I_E = I_C + I_B = 2.45 + 0.033 = 2.48\ \text{mA}$$

The power dissipated in the transistor is found to be

$$P_T = I_B V_{BE}(\text{on}) + I_C V_{CE} = (0.0332)(0.7) + (2.45)(0.2)$$

or

$$P_T = 0.513\ \text{mW}$$

Comment: When a transistor is driven into saturation, we use $V_{CE}(\text{sat})$ as another piecewise linear parameter. In addition, when a transistor is biased in the saturation mode, we have $I_C < \beta I_B$. This condition is very often used to prove that a transistor is indeed biased in the saturation mode.

EXERCISE PROBLEM

Ex 5.5: Consider the pnp circuit in Figure 5.22(a). Assume transistor parameters of $V_{EB}(\text{on}) = 0.7$ V, V_{EC} (sat) $= 0.2$ V, and $\beta = 110$. Assume circuit parameters of $V^+ = 3.3$ V, $R_C = 5$ kΩ, and $R_B = 150$ kΩ. Calculate I_B, I_C, and V_{EC} for (a) $V_{BB} = 2$ V and (b) $V_{BB} = 1$ V. (Ans. (a) $I_B = 4\,\mu$A, $I_C = 0.44$ mA, $V_{EC} = 1.1$ V; (b) $I_B = 10.7\,\mu$A, $I_C = 0.62$ mA, $V_{EC} = 0.2$ V)

Problem-Solving Technique: Bipolar DC Analysis

Analyzing the dc response of a bipolar transistor circuit requires knowing the mode of operation of the transistor. In some cases, the mode of operation may not be obvious, which means that we have to guess the state of the transistor, then analyze the circuit to determine if we have a solution consistent with our initial guess. To do this, we can:

1. Assume that the transistor is biased in the forward-active mode in which case $V_{BE} = V_{BE}(\text{on})$, $I_B > 0$, and $I_C = \beta I_B$.
2. Analyze the "linear" circuit with this assumption.
3. Evaluate the resulting state of the transistor. If the initial assumed parameter values and $V_{CE} > V_{CE}(\text{sat})$ are true, then the initial assumption is correct. However, if the calculation shows $I_B < 0$, then the transistor is probably cut off, and if the calculation shows $V_{CE} < 0$, the transistor is likely biased in saturation.
4. If the initial assumption is proven incorrect, then a new assumption must be made and the new "linear" circuit must be analyzed. Step 3 must then be repeated.

Because it is not always clear whether a transistor is biased in the forward-active or saturation mode, we may initially have to make an educated guess as to the state of the transistor and then verify our initial assumption. This is similar to the process we used for the analysis of multidiode circuits. For instance, in Example 5.5, we assumed a forward-active mode, performed the analysis, and showed that $V_{CE} < 0$. However, a negative V_{CE} for an npn transistor in the common-emitter configuration is not possible. Therefore, our initial assumption was disproved, and the transistor was biased in the saturation mode. Using the results of Example 5.5, we also see that when a transistor is in saturation, the ratio of I_C to I_B is always less than β, or

$$I_C/I_B < \beta$$

This condition is true for both the npn and the pnp transistor biased in the saturation mode. When a bipolar transistor is biased in saturation, we may define

$$\frac{I_C}{I_B} \equiv \beta_{\text{Forced}} \tag{5.32}$$

where β_{Forced} is called the "forced beta." We then have that $\beta_{\text{Forced}} < \beta$.

Another mode of operation for a bipolar transistor is the **inverse-active mode.** In this mode, the B–E junction is reverse biased and the B–C junction is forward biased. In effect, the transistor is operating "upside down"; that is, the emitter is acting as the collector and the collector is operating as the emitter. We will postpone discussions on this operating mode until we discuss digital electronic circuits later in this text.

To summarize, the four modes of operation for an npn transistor are shown in Figure 5.25. The four possible combinations of B–E and B–C voltages determine the modes of operation. If $v_{BE} > 0$ (forward-biased junction) and $v_{BC} < 0$ (reverse-biased junction), the transistor is biased in the forward-active mode. If both junctions are zero or reverse biased, the transistor is in cutoff. If both junctions are forward biased, the transistor is in saturation. If the B–E junction is reverse biased and the B–C junction is forward biased, the transistor is in the inverse-active mode.

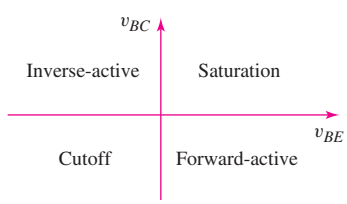

Figure 5.25 Bias conditions for the four modes of operation of an npn transistor

The piecewise linear parameter model of the transistor that we have used in the dc analysis of transistor circuits is adequate for many applications. Another transistor model is known as the **Ebers–Moll model.** This model can be used to describe the transistor in each of its possible operating modes and is used in the SPICE computer simulation program. However, we will not consider the Ebers–Moll model here.

Test Your Understanding

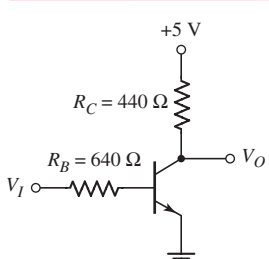

Figure 5.26 Figure for Exercise TYU 5.7 and TYU 5.8

In the following exercise problems, assume $V_{BE}(\text{on}) = 0.7$ V and $V_{CE}(\text{sat}) = 0.2$ V.

TYU 5.7 For the circuit shown in Figure 5.26, assume $\beta = 50$. Determine V_O, I_B, and I_C for: (a) $V_I = 0.2$ V, and (b) $V_I = 3.6$ V. Then, calculate the power dissipated in the transistor for the two conditions. (Ans. (a) $I_B = I_C = 0$, $V_O = 5$ V, $P = 0$; (b) $I_B = 4.53$ mA, $I_C = 10.9$ mA, $P = 5.35$ mW)

TYU 5.8 For the circuit shown in Figure 5.26, let $\beta = 50$, and determine V_I such that $V_{BC} = 0$. Calculate the power dissipated in the transistor. (Ans. $V_I = 0.825$ V, $P = 6.98$ mW)

5.2.3 Voltage Transfer Characteristics

A plot of the voltage transfer characteristics (output voltage versus input voltage) can also be used to visualize the operation of a circuit or the state of a transistor. The following example considers both an npn and a pnp transistor circuit.

EXAMPLE 5.6

Objective: Develop the voltage transfer curves for the circuits shown in Figures 5.27(a) and 5.27(b).

Assume npn transistor parameters of $V_{BE}(\text{on}) = 0.7$ V, $\beta = 120$, $V_{CE}(\text{sat}) = 0.2$ V, and $V_A = \infty$, and pnp transistor parameters of $V_{EB}(\text{on}) = 0.7$ V, $\beta = 80$, $V_{EC}(\text{sat}) = 0.2$ V, and $V_A = \infty$.

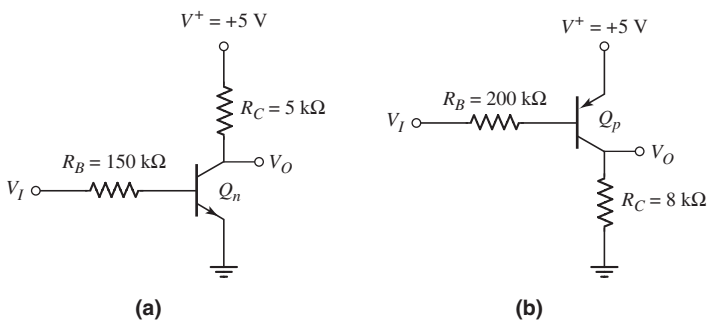

Figure 5.27 Circuits for Example 5.6; (a) npn circuit and (b) pnp circuit

Solution (npn Transistor Circuit): For $V_I \leq 0.7$ V, the transistor Q_n is cut off, so that $I_B = I_C = 0$. The output voltage is then $V_O = V^+ = 5$ V.

For $V_I > 0.7$ V, the transistor Q_n turns on and is initially biased in the forward-active mode. We have

$$I_B = \frac{V_I - 0.7}{R_B}$$

and

$$I_C = \beta I_B = \frac{\beta(V_I - 0.7)}{R_B}$$

Then

$$V_O = 5 - I_C R_C = 5 - \frac{\beta(V_I - 0.7)R_C}{R_B}$$

This equation is valid for $0.2 \leq V_O \leq 5$ V. When $V_O = 0.2$ V, the transistor Q_n goes into saturation. When $V_O = 0.2$ V, the input voltage is found from

$$0.2 = 5 - \frac{(120)(V_I - 0.7)(5)}{150}$$

which yields $V_I = 1.9$ V. For $V_I \geq 1.9$ V, the transistor Q_n remains biased in the saturation region.

The voltage transfer curve is shown in Figure 5.28(a).

Solution (pnp transistor circuit): For $4.3 \leq V_I \leq 5$ V, the transistor Q_p is cut off, so that $I_B = I_C = 0$. The output voltage is then $V_O = 0$.

For $V_I < 4.3$ V, the transistor Q_p turns on and is biased in the forward-active mode. We have

$$I_B = \frac{(5 - 0.7) - V_I}{R_B}$$

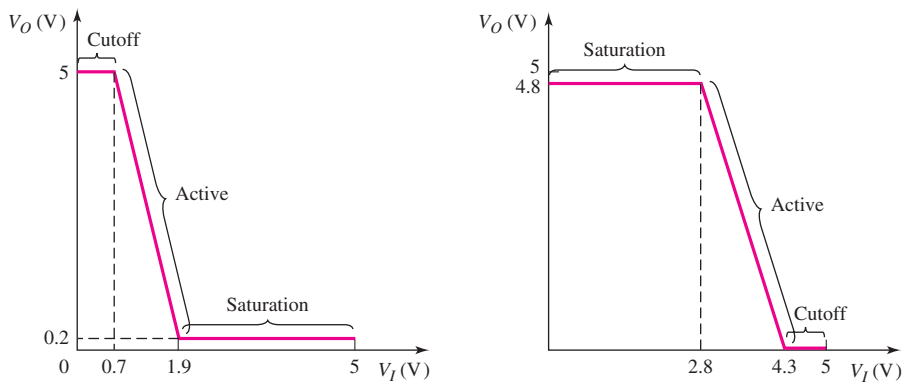

Figure 5.28 Voltage transfer characteristics for (a) npn circuit in Figure 5.27(a) and (b) pnp circuit in Figure 5.27(b)

and

$$I_C = \beta I_B = \beta\left[\frac{(5-0.7)-V_I}{R_B}\right]$$

The output voltage is then

$$V_O = I_C R_C = \beta R_C\left[\frac{(5-0.7)-V_I}{R_B}\right]$$

This equation is valid for $0 \leq V_O \leq 4.8$ V. When $V_O = 4.8$ V, the transistor Q_p goes into saturation.

When $V_O = 4.8$ V, the input voltage is found from

$$4.8 = (80)(8)\left[\frac{(5-0.7)-V_I}{200}\right]$$

which yields $V_I = 2.8$ V. For $V_I \leq 2.8$ V, the transistor Q_p remains biased in the saturation mode.

The voltage transfer curve is shown in Figure 5.28(b).

Computer Simulation: Figure 5.29 shows the voltage transfer characteristics from a PSpice simulation using a standard 2N3904 transistor. One result that may be

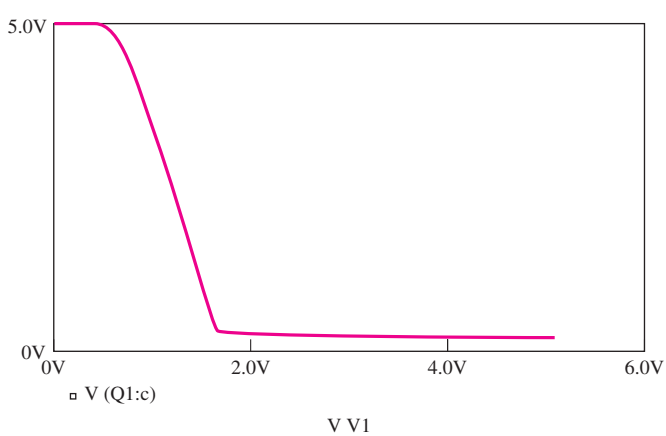

Figure 5.29 Voltage transfer characteristic for the circuit in Figure 5.27(a) generated by a PSpice simulation

observed from the computer simulation is that the output voltage in the forward-active mode is not exactly a linear function of input voltage as the hand analysis suggested. In addition, the base-emitter voltage when $v_I = 1.3$ V is $v_{BE} = 0.649$ V in the computer analysis results rather than the assumed value of 0.7 V in the hand analysis. However, the hand analysis gives a good first approximation.

Comment: As shown in this example, the voltage transfer characteristics are determined by finding the range of input voltage values that biases the transistor in cutoff, the forward-active mode, or the saturation mode.

EXERCISE PROBLEM

Ex 5.6: The circuit elements in Figure 5.27(a) are changed to $R_B = 200$ kΩ, $R_C = 4$ kΩ, and $V^+ = 9$ V. The transistor parameters are $\beta = 100$, $V_{BE}(\text{on}) = 0.7$ V, and $V_{CE}(\text{sat}) = 0.2$ V. Plot the voltage transfer characteristics for $0 \le V_I \le 9$ V. (Ans. For $0 \le V_I \le 0.7$ V, Q_n is cut off, $V_O = 9$ V; For $V_I \ge 5.1$ V, Q_n is in saturation, $V_O = 0.2$ V)

COMPUTER ANALYSIS EXERCISE

PS 5.2: Using a PSpice simulation, plot the voltage transfer characteristics of the circuit shown in Figure 5.27(b). Use a standard transistor. What is the value of v_{EB} when the transistor is biased in the forward-active region?

5.2.4 Commonly Used Bipolar Circuits: dc Analysis

There are a number of other bipolar transistor circuit configurations, in addition to the common-emitter circuits shown in Figures 5.20 and 5.22, that are commonly used. Several examples of such circuits are presented in this section. BJT circuits tend to be very similar in terms of dc analysis procedures, so that the same basic analysis approach will work regardless of the appearance of the circuit. We continue our dc analysis and design of bipolar circuits to increase our proficiency and to become more comfortable with these types of circuits.

EXAMPLE 5.7

Objective: Calculate the characteristics of a circuit containing an emitter resistor.

For the circuit shown in Figure 5.30(a), let $V_{BE}(\text{on}) = 0.7$ V and $\beta = 75$. Note that the circuit has both positive and negative power supply voltages.

Solution (Q-point values): Writing Kirchhoff's voltage law equation around the B–E loop, we have

$$V_{BB} = I_B R_B + V_{BE}(\text{on}) + I_E R_E + V^- \tag{5.33}$$

Assuming the transistor is biased in the forward-active mode, we can write $I_E = (1 + \beta)\, I_B$. We can then solve Equation (5.33) for the base current:

$$I_B = \frac{V_{BB} - V_{BE}(\text{on}) - V^-}{R_B + (1 + \beta)R_E} = \frac{1 - 0.7 - (-1.8)}{560 + (76)(3)} \Rightarrow 2.665\ \mu\text{A}$$

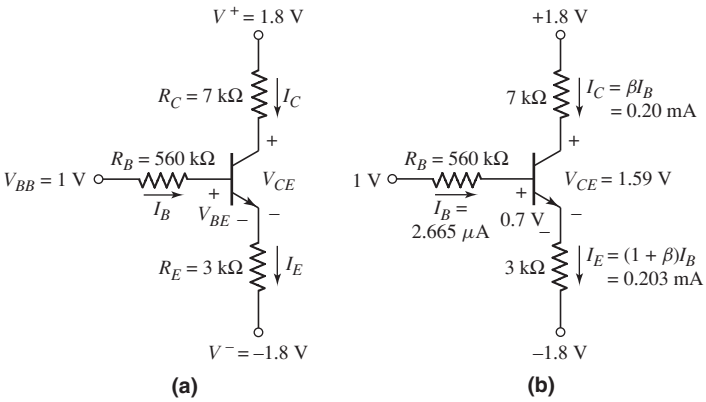

Figure 5.30 Circuit for Example 5.7: (a) circuit and (b) circuit showing current and voltage values

The collector and emitter currents are

$$I_C = \beta I_B = (75)(2.665\,\mu\text{A}) \Rightarrow 0.20\,\text{mA}$$

and

$$I_E = (1+\beta)\,I_B = (76)(2.665\,\mu\text{A}) \Rightarrow 0.203\,\text{mA}$$

From Figure 5.30(b), the collector–emitter voltage is

$$V_{CE} = V^+ - I_C R_C - I_E R_E - V^- = 1.8 - (0.20)(7) - (0.203)(3) - (-1.8)$$

or

$$V_{CE} = 1.59\,\text{V}$$

Solution (load line): We again use Kirchhoff's voltage law around the C–E loop. From the relationship between the collector and emitter currents, we find

$$V_{CE} = (V^+ - V^-) - I_C\left[R_C + \left(\frac{1+\beta}{\beta}\right)R_E\right]$$
$$= [1.8 - (-1.8)] - I_C\left[7 + \left(\frac{76}{75}\right)(3)\right]$$

or

$$V_{CE} = 3.6 - I_C(10.04)$$

The load line and the calculated Q-point are shown in Figure 5.31. A few transistor characteristics of I_C versus V_{CE} are superimposed on the figure.

Comment: Since the C–E voltage is 1.59 V, $V_{CE} > V_{BE}(\text{on})$ and the transistor is biased in the forward-active mode, as initially assumed. We will see, later in the chapter, the value of including an emitter resistor in a circuit.

EXERCISE PROBLEM

Ex 5.7: The parameters of the circuit shown in Figure 5.30(a) are changed to $V^+ = 3.3$ V, $V^- = -3.3$ V, $V_{BB} = 0$, $R_B = 640\,\text{k}\Omega$, $R_E = 2.4\,\text{k}\Omega$, and $R_C = 10\,\text{k}\Omega$. The transistor parameters are $\beta = 80$ and $V_{BE}(\text{on}) = 0.7$ V. Calculate all transistor currents and V_{CE}. (Ans. $I_B = 3.116\,\mu\text{A}$, $I_C = 0.249\,\text{mA}$, $I_E = 0.252\,\text{mA}$, $V_{CE} = 3.51$ V)

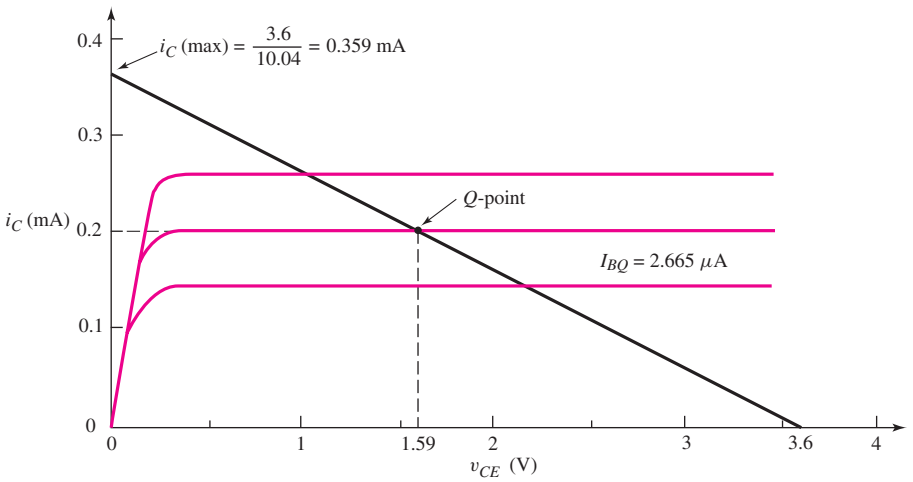

Figure 5.31 Load line and Q-point for the circuit shown in Figure 5.30 for Example 5.7

DESIGN EXAMPLE 5.8

Objective: Design the common-base circuit shown in Figure 5.32 such that $I_{EQ} = 0.50$ mA and $V_{ECQ} = 4.0$ V.

Assume transistor parameters of $\beta = 120$ and $V_{EB}(\text{on}) = 0.7$ V.

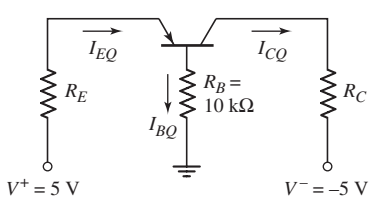

Figure 5.32 Common-base circuit for Example 5.8

Solution: Writing Kirchhoff's voltage law equation around the base–emitter loop (assuming the transistor is biased in the forward-active mode), we have

$$V^+ = I_{EQ}R_E + V_{EB}(\text{on}) + \left(\frac{I_{EQ}}{1+\beta}\right)R_B$$

or

$$5 = (0.5)R_E + 0.7 + \left(\frac{0.5}{121}\right)(10)$$

which yields

$$R_E = 8.52\ \text{k}\Omega$$

We can find

$$I_{CQ} = \left(\frac{\beta}{1+\beta}\right)I_{EQ} = \left(\frac{120}{121}\right)(0.5) = 0.496\ \text{mA}$$

Now, writing Kirchhoff's voltage law equation around the emitter–collector loop, we have

$$V^+ = I_{EQ}R_E + V_{ECQ} + I_{CQ}R_C + V^-$$

or

$$5 = (0.5)(8.52) + 4 + (0.496)R_C + (-5)$$

which yields

$$R_C = 3.51\ \text{k}\Omega$$

Comment: The circuit analysis of the common-base circuit proceeds in the same way as all previous circuits.

EXERCISE PROBLEM

Ex 5.8: Design the common-base circuit shown in Figure 5.33 such that $I_{EQ} = 0.125\,\text{mA}$ and $V_{ECQ} = 2.2\,\text{V}$. The transistor parameters are $\beta = 110$ and $V_{EB}(\text{on}) = 0.7\,\text{V}$. (Ans. $R_E = 18.4\,\text{k}\Omega$, $R_C = 12.1\,\text{k}\Omega$)

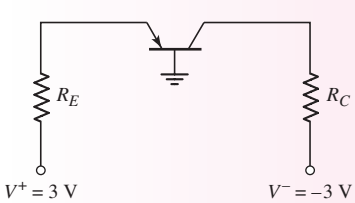

Figure 5.33 Common-base circuit for Exercise Problem Ex 5.8

Test Your Understanding

TYU 5.9 The bias voltages in the circuit shown in Figure 5.34 are $V^+ = 3.3\,\text{V}$ and $V^- = -3.3\,\text{V}$. The measured value of the collector voltage is $V_C = 2.27\,\text{V}$. Determine I_B, I_C, I_E, β, and α. (Ans. $I_B = 2.50\,\mu\text{A}$, $I_C = 0.2575\,\text{mA}$, $I_E = 0.26\,\text{mA}$, $\beta = 103$, $\alpha = 0.99038$)

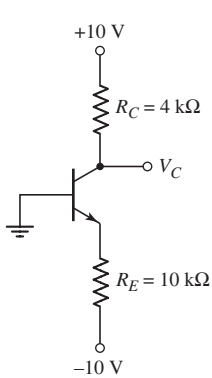

Figure 5.34 Figure for Exercise TYU 5.9

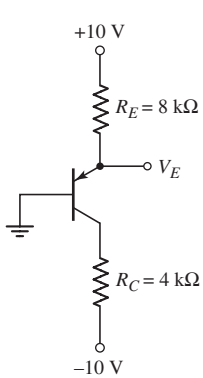

Figure 5.35 Figure for Exercise TYU 5.10

TYU 5.10 The bias voltages in the circuit shown in Figure 5.35 are $V^+ = 5$ V and $V^- = -5$ V. Assume that $\beta = 85$. Determine I_B, I_C, I_E, and V_{EC}. (Ans. $I_B = 6.25\,\mu$A, $I_C = 0.531$ mA, $I_E = 0.5375$ mA, $V_{EC} = 3.575$ V)

DESIGN EXAMPLE 5.9

Objective: Design a pnp bipolar transistor circuit to meet a set of specifications.

Specifications: The circuit configuration to be designed is shown in Figure 5.36(a). The quiescent emitter-collector voltage is to be $V_{ECQ} = 2.5$ V.

Choices: Discrete resistors with tolerances of ± 10 percent are to be used, an emitter resistor with a nominal value of $R_E = 2$ kΩ is to be used, and a transistor with $\beta = 60$ and $V_{EB}(\text{on}) = 0.7$ V is available.

Solution (ideal Q-point value): Writing the Kirchhoff's voltage law equation around the C–E loop, we obtain

$$V^+ = I_{EQ}R_E + V_{ECQ}$$

or

$$5 = I_{EQ}(2) + 2.5$$

which yields $I_{EQ} = 1.25$ mA. The collector current is

$$I_{CQ} = \left(\frac{\beta}{1+\beta}\right) \cdot I_{EQ} = \left(\frac{60}{61}\right)(1.25) = 1.23\,\text{mA}$$

The base current is

$$I_{BQ} = \frac{I_{EQ}}{1+\beta} = \frac{1.25}{61} = 0.0205\,\text{mA}$$

Writing the Kirchhoff's voltage law equation around the E–B loop, we find

$$V^+ = I_{EQ}R_E + V_{EB}(\text{on}) + I_{BQ}R_B + V_{BB}$$

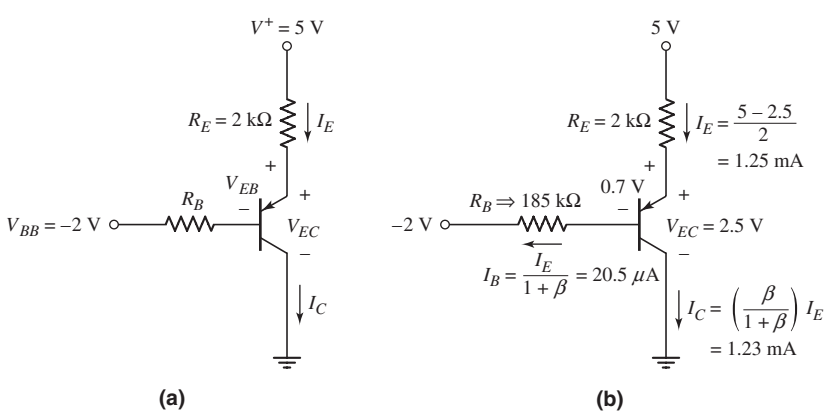

Figure 5.36 Circuit for Design Example 5.9: (a) circuit and (b) circuit showing current and voltage values

or

$$5 = (1.25)(2) + 0.7 + (0.0205)R_B + (-2)$$

which yields $R_B = 185\,\text{k}\Omega$.

Solution (ideal load line): The load line equation is

$$V_{EC} = V^+ - I_E R_E = V^+ - I_C\left(\frac{1+\beta}{\beta}\right)R_E$$

or

$$V_{EC} = 5 - I_C\left(\frac{61}{60}\right)(2) = 5 - I_C(2.03)$$

The load line, using the nominal value of R_E, and the calculated Q-point are shown in Figure 5.37(a).

Trade-offs: As shown in Appendix C, a standard resistor value of 185 kΩ is not available. We will pick a value of 180 kΩ. We will consider R_B and R_E resistor tolerances of ±10 percent.

The quiescent collector current is given by

$$I_{CQ} = \beta\left[\frac{V^+ - V_{EB}(\text{on}) - V_{BB}}{R_B + (1+\beta)R_E}\right] = (60)\left[\frac{6.3}{R_B + (61)R_E}\right]$$

and the load line is given by

$$V_{EC} = V^+ - I_C\left(\frac{1+\beta}{\beta}\right)R_E = 5 - \left(\frac{61}{60}\right)I_C R_E$$

The extreme values of R_E are:

$$2\,\text{k}\Omega - 10\% = 1.8\,\text{k}\Omega \qquad 2\,\text{k}\Omega + 10\% = 2.2\,\text{k}\Omega.$$

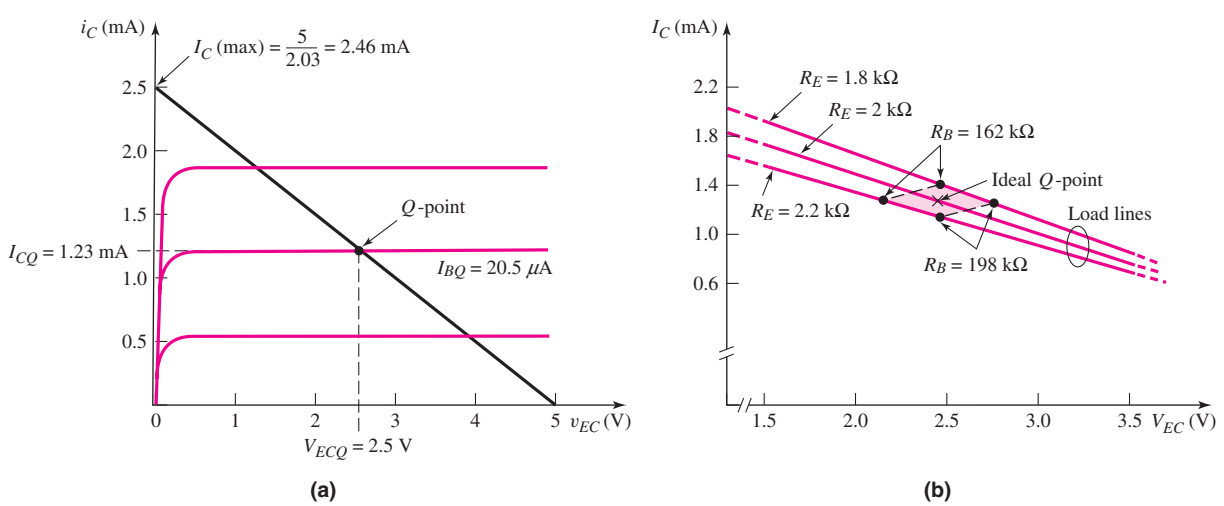

Figure 5.37 (a) Load line and Q-point value for the ideal designed circuit shown in Figure 5.36 used in Example 5.9; (b) load lines and Q-point values for the extreme tolerance values of resistors

The extreme values of R_B are:

$$180\ \text{k}\Omega - 10\% = 162\ \text{k}\Omega \qquad 180\ \text{k}\Omega + 10\% = 198\ \text{k}\Omega.$$

The Q-point values for the extreme values of R_B and R_E are given in the following table.

	R_E	
R_B	1.8 kΩ	2.2 kΩ
162 kΩ	$I_{CQ} = 1.39$ mA $V_{ECQ} = 2.46$ V	$I_{CQ} = 1.28$ mA $V_{ECQ} = 2.14$ V
198 kΩ	$I_{CQ} = 1.23$ mA $V_{ECQ} = 2.75$ V	$I_{CQ} = 1.14$ mA $V_{ECQ} = 2.45$ V

Figure 5.37(b) shows the Q-points for the various possible extreme values of emitter and base resistances. The shaded area shows the region in which the Q-point will occur over the range of resistor values.

Comment: This example shows that an ideal Q-point can be determined based on a set of specifications, but, because of resistor tolerance, the actual Q-point will vary over a range of values. Other examples will consider the tolerances involved in transistor parameters.

EXERCISE PROBLEM

Ex 5.9: The circuit elements in Figure 5.36(a) are $V^+ = 5$ V, $V_{BB} = -2$ V, $R_E = 2$ kΩ, and $R_B = 180$ kΩ. Assume $V_{EB}(\text{on}) = 0.7$ V. Plot the Q-point on the load line for (a) $\beta = 40$, (b) $\beta = 60$, (c) $\beta = 100$, and (d) $\beta = 150$. (Ans. (a) $I_{CQ} = 0.962$ mA, (b) $I_{CQ} = 1.25$ mA, (c) $I_{CQ} = 1.65$ mA, (d) $I_{CQ} = 1.96$ mA)

EXAMPLE 5.10

Objective: Calculate the characteristics of an npn bipolar transistor circuit with a load resistance. The load resistance can represent a second transistor stage connected to the output of a transistor circuit.

For the circuit shown in Figure 5.38(a), the transistor parameters are: $V_{BE}(\text{on}) = 0.7$ V, and $\beta = 100$.

Solution (Q-Point Values): Kirchhoff's voltage law equation around the B–E loop yields

$$I_B R_B + V_{BE}(\text{on}) + I_E R_E + V^- = 0$$

Again assuming $I_E = (1 + \beta) I_B$, we find

$$I_B = \frac{-(V^- + V_{BE}(\text{on}))}{R_B + (1 + \beta) R_E} = \frac{-(-5 + 0.7)}{10 + (101)(5)} \Rightarrow 8.35\ \mu\text{A}$$

The collector and emitter currents are

$$I_C = \beta I_B = (100)(8.35\ \mu\text{A}) \Rightarrow 0.835\ \text{mA}$$

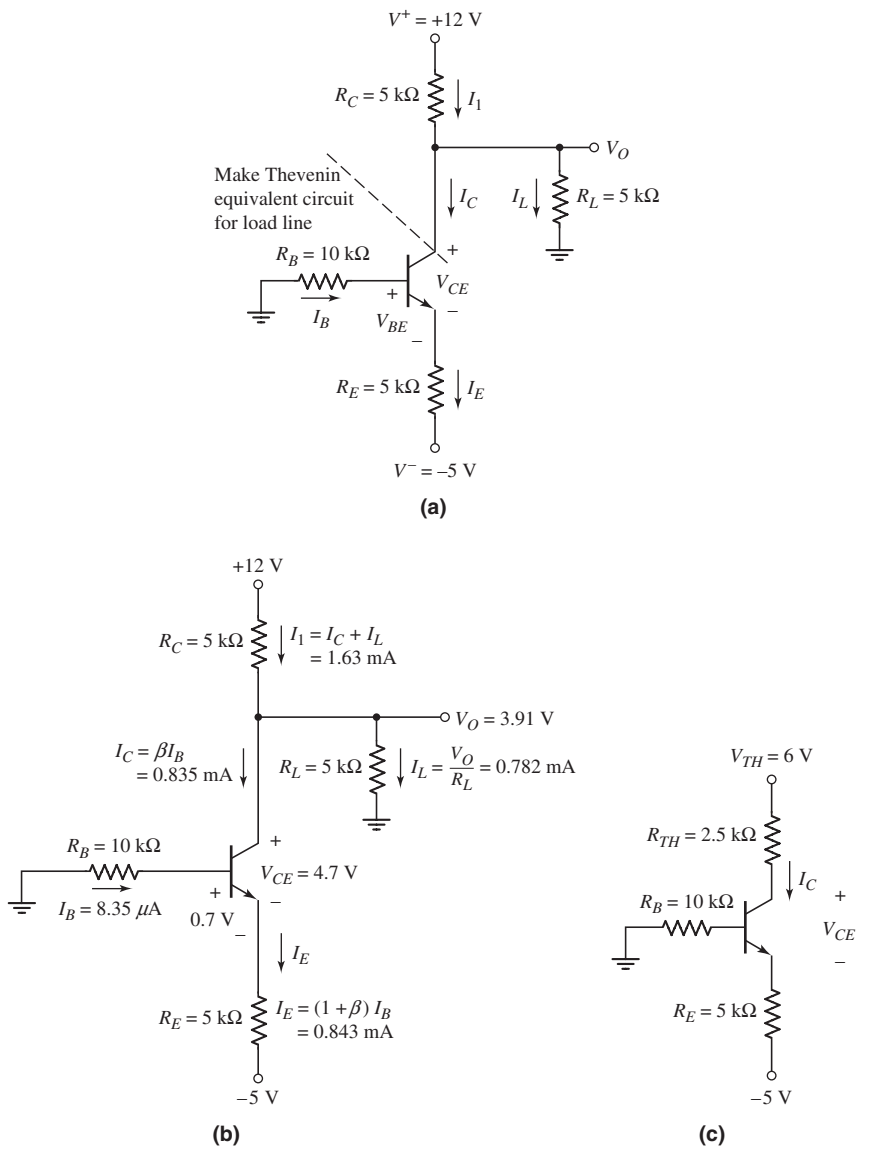

Figure 5.38 Circuit for Example 5.10: (a) circuit; (b) circuit showing current and voltage values; and (c) Thevenin equivalent circuit

and

$$I_E = (1 + \beta)I_B = (101)(8.35\,\mu\text{A}) \Rightarrow 0.843\,\text{mA}$$

At the collector node, we can write

$$I_C = I_1 - I_L = \frac{V^+ - V_O}{R_C} - \frac{V_O}{R_L}$$

or

$$0.835 = \frac{12 - V_O}{5} - \frac{V_O}{5}$$

Solving for V_O, we find $V_O = 3.91$ V. The currents are then $I_1 = 1.62$ mA and $I_L = 0.782$ mA. Referring to Figure 5.38(b), the collector–emitter voltage is

$$V_{CE} = V_O - I_E R_E - (-5) = 3.91 - (0.843)(5) - (-5) = 4.70\,\text{V}$$

Solution (Load Line): The load line equation for this circuit is not as straightforward as for previous circuits. The easiest approach to finding the load line is to make a "Thevenin equivalent circuit" of R_L, R_C, and V^+, as indicated in Figure 5.38(b). (Thevenin equivalent circuits are also covered later in this chapter, in Section 5.4.) The Thevenin equivalent resistance is

$$R_{TH} = R_L \| R_C = 5 \| 5 = 2.5\,\text{k}\Omega$$

and the Thevenin equivalent voltage is

$$V_{TH} = \left(\frac{R_L}{R_L + R_C}\right) \cdot V^+ = \left(\frac{5}{5+5}\right) \cdot (12) = 6\,\text{V}$$

The equivalent circuit is shown in Figure 5.38(c). The Kirchhoff voltage law equation around the C–E loop is

$$V_{CE} = (6 - (-5)) - I_C R_{TH} - I_E R_E = 11 - I_C(2.5) - I_C\left(\frac{101}{100}\right) \cdot (5)$$

or

$$V_{CE} = 11 - I_C(7.55)$$

The load line and the calculated Q-point values are shown in Figure 5.39.

Comment: Remember that the collector current, determined from $I_C = \beta I_B$, is the current into the collector terminal of the transistor; it is not necessarily the current in the collector resistor R_C.

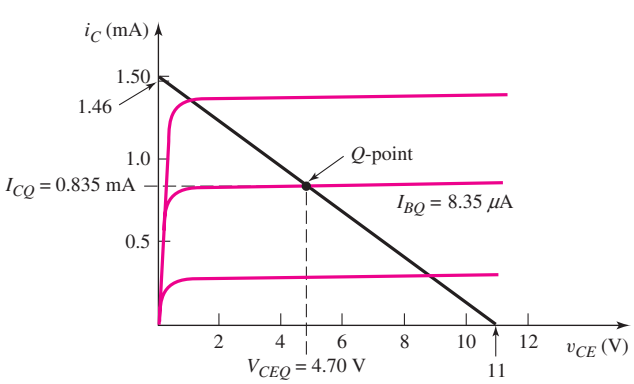

Figure 5.39 Load line and Q-point for the circuit shown in Figure 5.38(a) for Example 5.10

EXERCISE PROBLEM

Ex 5.10: For the transistor shown in the circuit of Figure 5.40, the common-base current gain is $\alpha = 0.9920$. Determine R_E such that the emitter current is limited to $I_E = 1.0$ mA. Also determine I_B, I_C, and V_{BC}. (Ans. $R_E = 3.3$ kΩ, $I_C = 0.992$ mA, $I_B = 8.0\ \mu$A, $V_{BC} = 4.01$ V)

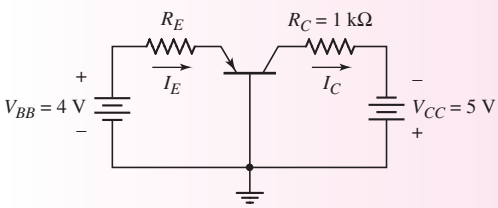

Figure 5.40 Figure for Exercise Ex 5.10

Test Your Understanding

TYU 5.11 For the circuit shown in Figure 5.41, determine I_E, I_B, I_C, and V_{CE}, if $\beta = 75$. (Ans. $I_B = 15.1\ \mu$A, $I_C = 1.13$ mA, $I_E = 1.15$ mA, $V_{CE} = 6.03$ V)

TYU 5.12 Assume $\beta = 120$ for the transistor in Figure 5.42. Determine R_E such that $V_{CE} = 2.2$ V. (Ans. $R_E = 154\ \Omega$)

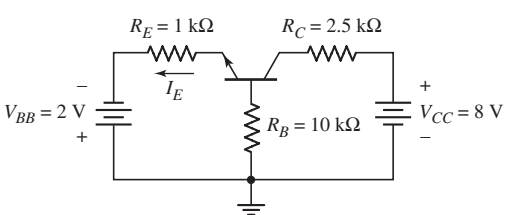

Figure 5.41 Figure for Exercise TYU 5.11

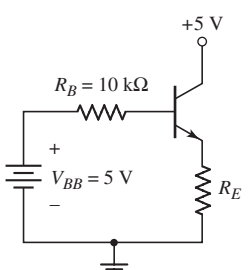

Figure 5.42 Figure for Exercise TYU 5.12

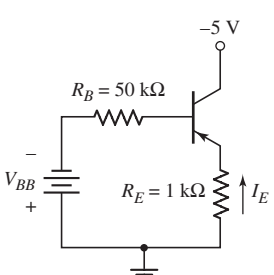

Figure 5.43 Figure for Exercise TYU 5.13

TYU 5.13 For the transistor in Figure 5.43, assume $\beta = 90$. (a) Determine V_{BB} such that $I_E = 1.2$ mA. (b) Find I_C and V_{EC}. (Ans. (a) $V_{BB} = 2.56$ V; (b) $I_C = 1.19$ mA, $V_{EC} = 3.8$ V)

COMPUTER ANALYSIS EXERCISE

PS 5.3: Verify the common-base circuit analysis in Test Your Understanding Exercise TYU 5.11 with a PSpice simulation. Use a standard transistor.

5.3 BASIC TRANSISTOR APPLICATIONS

Objective: • Examine three applications of bipolar transistor circuits: a switch circuit, digital logic circuit, and an amplifier circuit.

Transistors can be used to: switch currents, voltages, and power; perform digital logic functions; and amplify time-varying signals. In this section, we consider the switching properties of the bipolar transistor, analyze a simple transistor digital logic circuit, and then show how the bipolar transistor is used to amplify time-varying signals.

5.3.1 Switch

Figure 5.44 shows a bipolar circuit called an **inverter,** in which the transistor in the circuit is switched between cutoff and saturation. The load, for example, could be a motor, a light-emitting diode or some other electrical device. If $v_I < V_{BE}(\text{on})$, then $i_B = i_C = 0$ and the transistor is cut off. Since $i_C = 0$, the voltage drop across the load is zero, so the output voltage is $v_O = V_{CC}$. Also, since the currents in the transistor are zero, the power dissipation in the transistor is zero. If the load were a motor, the motor would be off with zero current. Likewise, if the load were a light-emitting diode, the light output would be zero with zero current.

If we let $v_I = V_{CC}$ and if the ratio of R_B to R_C, where R_C is the effective resistance of the load, is less than β, then the transistor is usually driven into saturation, which means that

$$i_B \cong \frac{v_I - V_{BE}(\text{on})}{R_B} \tag{5.34}$$

$$i_C = I_C(\text{sat}) = \frac{V_{CC} - V_{CE}(\text{sat})}{R_C} \tag{5.35}$$

and

$$v_O = V_{CE}(\text{sat}) \tag{5.36}$$

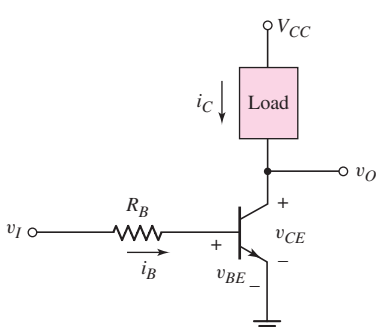

Figure 5.44 An npn bipolar inverter circuit used as a switch

In this case, a collector current is induced that would turn on the motor or the LED, depending on the type of load.

Equation (5.34) assumes that the B–E voltage can be approximated by the turn-on voltage. This approximation will be modified slightly when we discuss bipolar digital logic circuits in Chapter 17.

EXAMPLE 5.11

Objective: Calculate the appropriate resistance values and transistor power dissipation for the two inverter switching configurations shown in Figure 5.45.

Specifications (Figure 5.45(a)): The transistor in the inverter circuit in Figure 5.45(a) is used to turn the light-emitting diode (LED) on and off. The required LED current is $I_{C1} = 12\,\text{mA}$ to produce the specified output light. Assume transistor parameters of $\beta = 80$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, and $V_{CE}\,(\text{sat}) = 0.2\,\text{V}$, and assume the diode cut-in voltage is $V_\gamma = 1.5\,\text{V}$. [Note: LEDs are fabricated with compound semiconductor materials and have a larger cut-in voltage compared to silicon diodes.]

Specifications (Figure 5.45(b)): The inverter circuit in Figure 5.45(b) uses a pnp transistor. In this case, one side of the load (for example a motor) can be connected to ground potential. The required load current is $I_{C2} = 5\,\text{A}$. Assume transistor parameters of $\beta = 40$,$V_{EB}(\text{on}) = 0.7\,\text{V}$, and $V_{EC}(\text{sat}) = 0.2\,\text{V}$.

Solution (Figure 5.45(a)): For $v_{I1} = 0$, transistor Q_1 is cut off so that $I_{B1} = I_{C2} = 0$ and the LED is also off.

For $v_{I1} = 5\,\text{V}$, we require $I_{C1} = 12\,\text{mA}$ and want the transistor to be driven into saturation. Then

$$R_1 = \frac{V^+ - (V_\gamma + V_{CE}(\text{sat}))}{I_{C1}} = \frac{5 - (1.5 + 0.2)}{12} \Rightarrow R_1 = 275\,\Omega$$

We may let $I_{C1}/I_{B1} = 40$. Then $I_{B1} = 12/40 = 0.3\,\text{mA}$. Now

$$R_{B1} = \frac{v_{I1} - V_{BE}(\text{on})}{I_{B1}} = \frac{5 - 0.7}{0.3} = 14.3\,\text{k}\Omega$$

The power dissipation in Q_1 is

$$P_1 = I_{B1}V_{BE}(\text{on}) + I_{C1}V_{CE}(\text{sat}) = (0.3)(0.7) + (12)(0.2) = 2.61\,\text{mW}$$

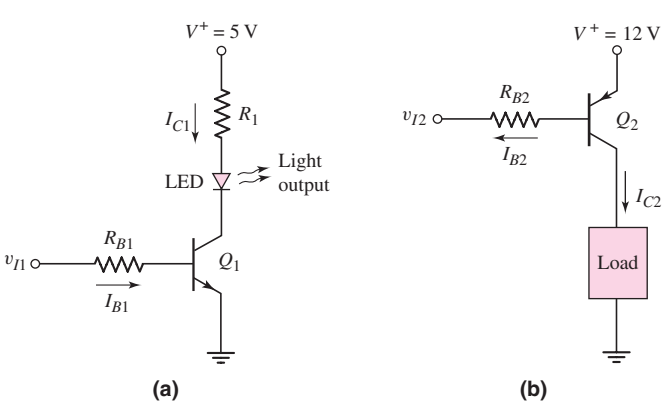

Figure 5.45 Figures for Example 5.11

Solution (Figure 5.45(b)): For $v_{I2} = 12$ V, transistor Q_2 is cut off so that $I_{B2} = I_{C2} = 0$ and the voltage across the load is zero.

For $v_{I2} = 0$, transistor Q_2 is to be driven into saturation so that $V_{EC2} = V_{EC}(\text{sat}) = 0.2$ V. The voltage across the load is 11.8 V, the current is 5 A, which means the effective load resistance is 2.36 Ω

If we let $I_{C2}/I_{B2} = 20$, then $I_{B2} = 5/20 = 0.25$ A. Now

$$R_{B2} = \frac{V^+ - V_{EB}(\text{on}) - v_{I2}}{I_{B2}} = \frac{12 - 0.7 - 0}{0.25} = 45.2\,\Omega$$

The power dissipation in transistor Q_2 is

$$P_2 = I_{B2}V_{EB}(\text{on}) + I_{C2}V_{EC}(\text{sat}) = (0.25)(0.7) + (5)(0.2) = 1.175\,\text{W}$$

Comment: As with most electronic circuit designs, there are some assumptions that need to be made. The assumption to let $I_C/I_B = (1/2)\beta$ in each case ensures that each transistor will be driven into saturation even if variations in circuit parameters occur. At the same time, base currents are limited to reasonable values.

We may note that for the circuit in Figure 5.45(a), a base current of only 0.3 mA induces a load current of 12 mA. For the circuit in Figure 5.45(b), a base current of only 0.25 A induces a load current of 5 A. The advantage of transistor switches is that large load currents can be switched with relatively small base currents.

EXERCISE PROBLEM

Ex 5.11: (a) Redesign the LED circuit in Figure 5.45(a) such that $I_{C1} = 15$ mA and $I_{C1}/I_{B1} = 50$ for $v_I = 5$ V. Use the same Q_1 transistor parameters given in Example 5.11. (b) Redesign the circuit in Figure 5.45(b) such that $I_{C2} = 2$ A and $I_{C2}/I_{B2} = 25$ for $v_I = 0$. Use the same Q_2 transistor parameters as given in Example 5.11. (Ans. (a) $R_1 = 220\,\Omega$, $R_{B1} = 14.3\,\text{k}\Omega$; (b) $R_{B2} = 141\,\Omega$)

When a transistor is biased in saturation, the relationship between the collector and base currents is no longer linear. Consequently, this mode of operation cannot be used for linear amplifiers. On the other hand, switching a transistor between cutoff and saturation produces the greatest change in output voltage, which is especially useful in digital logic circuits, as we will see in the next section.

5.3.2 Digital Logic

Consider the simple transistor inverter circuit shown in Figure 5.46(a). If the input V_I is approximately zero volts, the transistor is cut off and the output V_O is high and equal to V_{CC}. If, on the other hand, the input is high and equal to V_{CC}, the transistor can be driven into saturation, in which case the output is low and equal to V_{CE} (sat).

Now consider the case when a second transistor is connected in parallel, as shown in Figure 5.46(b). When the two inputs are zero, both transistors Q_1 and Q_2 are in cutoff, and $V_O = 5$ V. When $V_1 = 5$ V and $V_2 = 0$, transistor Q_1 can be driven into saturation, and Q_2 remains in cutoff. With Q_1 in saturation, the output voltage is $V_O = V_{CE}(\text{sat}) \cong 0.2$ V. If we reverse the input voltages so that $V_1 = 0$ and $V_2 = 5$ V, then Q_1 is in cutoff, Q_2 can be driven into saturation, and $V_O = V_{CE}(\text{sat}) \cong 0.2$ V. If both inputs are high, meaning $V_1 = V_2 = 5$ V, then both transistors can be driven into saturation, and $V_O = V_{CE}(\text{sat}) \cong 0.2$ V.

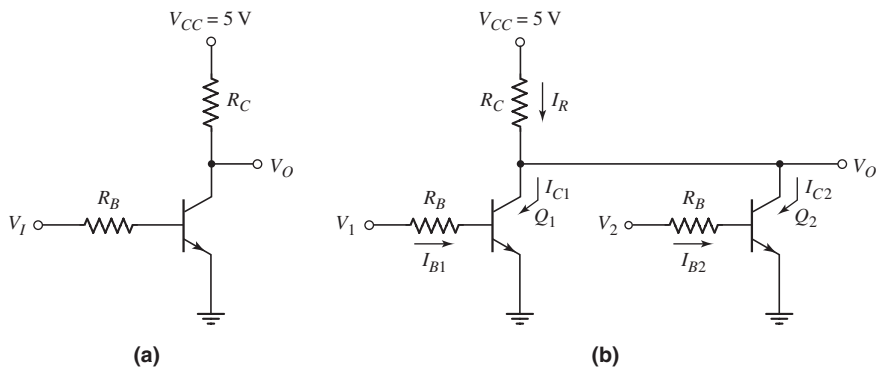

Figure 5.46 A bipolar (a) inverter circuit and (b) NOR logic gate

Table 5.2 shows these various conditions for the circuit in Figure 5.46(b). In a **positive logic system,** meaning that the larger voltage is a logic 1 and the lower voltage is a logic 0, this circuit performs the **NOR logic function.** The circuit of Figure 5.46(b) is then a two-input bipolar NOR logic circuit.

Table 5.2 The bipolar NOR logic circuit response

V_1 (V)	V_2 (V)	V_O (V)
0	0	5
5	0	0.2
0	5	0.2
5	5	0.2

EXAMPLE 5.12

Objective: Determine the currents and voltages in the circuit shown in Figure 5.46(b).

Assume the transistor parameters are: $\beta = 50$, $V_{BE}(\text{on}) = 0.7$ V, and $V_{CE}(\text{sat}) = 0.2$ V. Let $R_C = 1$ kΩ and $R_B = 20$ kΩ. Determine the currents and output voltage for various input conditions.

Solution: The following table indicates the equations and results for this example.

Condition	V_O	I_R	Q_1	Q_2
$V_1 = 0$, $V_2 = 0$	5 V	0	$I_{B1} = I_{C1} = 0$	$I_{B2} = I_{C2} = 0$
$V_1 = 5$ V, $V_2 = 0$	0.2 V	$\dfrac{5 - 0.2}{1} = 4.8$ mA	$I_{B1} = \dfrac{5 - 0.7}{20} = 0.215$ mA $I_{C1} = I_R = 4.8$ mA	$I_{B2} = I_{C2} = 0$
$V_1 = 0$, $V_2 = 5$ V	0.2 V	4.8 mA	$I_{B1} = I_{C1} = 0$	$I_{B2} = 0.215$ mA $I_{C2} = I_R = 4.8$ mA
$V_1 = 5$ V, $V_2 = 5$ V	0.2 V	4.8 mA	$I_{B1} = 0.215$ mA $I_{C1} = \dfrac{I_R}{2} = 2.4$ mA	$I_{B2} = 0.215$ mA $I_{C2} = \dfrac{I_R}{2} = 2.4$ mA

Comment: In this example, we see that whenever a transistor is conducting, the ratio of collector current to base current is always less than β. This shows that the transistor is in saturation, which occurs when either V_1 or V_2 is 5 V.

EXERCISE PROBLEM

Ex 5.12: The transistor parameters in the circuit in Figure 5.46(b) are: $\beta = 40$, $V_{BE}(\text{on}) = 0.7$ V, and $V_{CE}(\text{sat}) = 0.2$ V. Let $R_C = 600\ \Omega$ and $R_B = 950\ \Omega$. Determine the currents and output voltage for: (a) $V_1 = V_2 = 0$; (b) $V_1 = 5$ V, $V_2 = 0$; and (c) $V_1 = V_2 = 5$ V. (Ans. (a) The currents are zero, $V_O = 5$ V; (b) $I_{B2} = I_{C2} = 0$, $I_{B1} = 4.53$ mA, $I_{C1} = I_R = 8$ mA, $V_O = 0.2$ V; (c) $I_{B1} = I_{B2} = 4.53$ mA, $I_{C1} = I_{C2} = 4\text{ mA} = I_R/2$, $V_O = 0.2$ V)

This example and the accompanying discussion illustrate that bipolar transistor circuits can be configured to perform logic functions. In Chapter 17, we will see that this circuit can experience loading effects when load circuits or other digital logic circuits are connected to the output. Therefore, logic circuits must be designed to minimize or eliminate such loading effects.

5.3.3 Amplifier

The bipolar inverter circuit can also be used to amplify a time-varying signal. Figure 5.47(a) shows an inverter circuit including a time-varying voltage source Δv_I in the base circuit. The voltage transfer characteristics are shown in Figure 5.47(b). The dc voltage source V_{BB} is used to bias the transistor in the forward-active region. The Q-point is shown on the transfer characteristics.

The voltage source Δv_I introduces a time-varying signal on the input. A change in the input voltage then produces a change in the output voltage. These time-varying input and output signals are shown in Figure 5.47(b). If the magnitude of the slope of the transfer characteristics is greater than unity, then the time-varying output signal will be larger than the time-varying input signal—thus an amplifier.

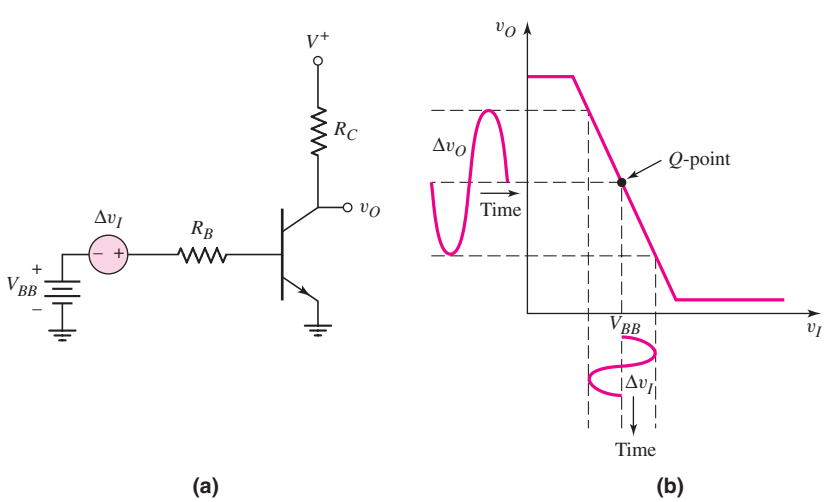

Figure 5.47 (a) A bipolar inverter circuit to be used as a time-varying amplifier; (b) the voltage transfer characteristics

EXAMPLE 5.13

Objective: Determine the amplification factor for the circuit given in Figure 5.48(a). The transistor parameters are $\beta = 120$, $V_{BE}(\text{on}) = 0.7$ V, and $V_A = \infty$.

DC Solution: The voltage transfer characteristics were developed in Example 5.6 for this same circuit. The voltage transfer curve is repeated for convenience in Figure 5.48(b).

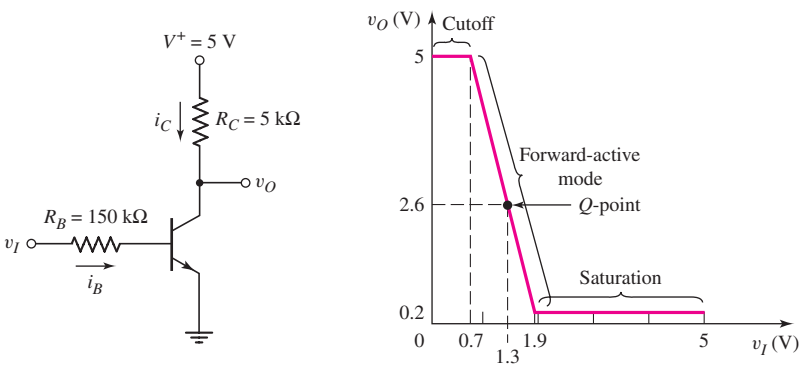

Figure 5.48 (a) A bipolar inverter used as an amplifier; (b) the inverter voltage transfer characteristics

For $0.7 \leq v_I \leq 1.9$ V, the transistor is biased in the forward-active mode and the output voltage is given by

$$v_O = 7.8 - 4v_I$$

Now bias the transistor in the center of the active region with an input voltage of $v_I = V_{BB} = 1.3$ V. The dc output voltage is $v_O = 2.6$ V. The Q-point is shown on the transfer characteristics.

AC Solution: From $v_O = 7.8 - 4v_I$, we can find the change in output voltage with respect to a change in input voltage. We find

$$\Delta v_O = -4\Delta v_I$$

The voltage gain is then

$$A_v = \frac{\Delta v_O}{\Delta v_I} = -4$$

Computer Simulation: A 2 kHz sinusoidal voltage source was placed in the base circuit of Figure 5.48(a). The amplitude of the time-varying input signal was 0.2 V. Figure 5.49 shows the output response of the circuit. A sinusoidal signal is superimposed on a dc value as we expect. The peak-to-peak output signal is approximately 1.75 V. The time-varying amplification factor is then $|A_v| = 1.75/(2)(0.2) = 4.37$. This value agrees quite well with the hand analysis.

Comment: As the input voltage changes, we move along the voltage transfer characteristics as shown in Figure 5.50(b). The negative sign occurs because of the inverting property of the circuit.

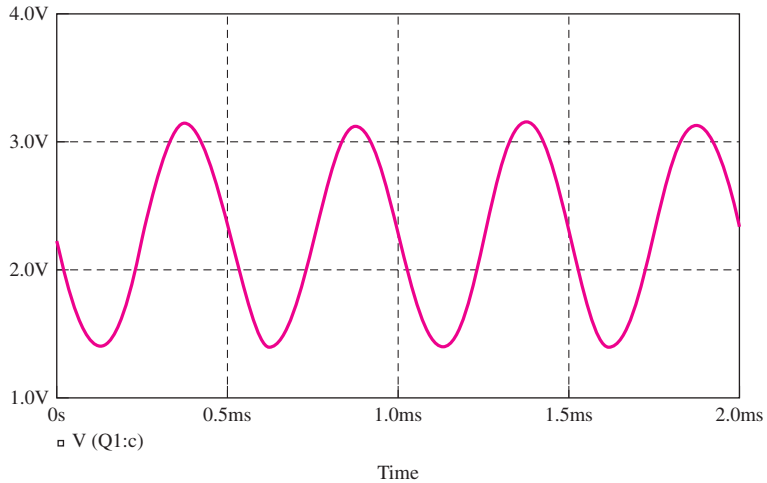

Figure 5.49 Output signal from the circuit shown in Figure 5.48 for input signals of $V_{BB} = 1.3$ V and $\Delta v_I = 0.2 \sin \omega t$ (V)

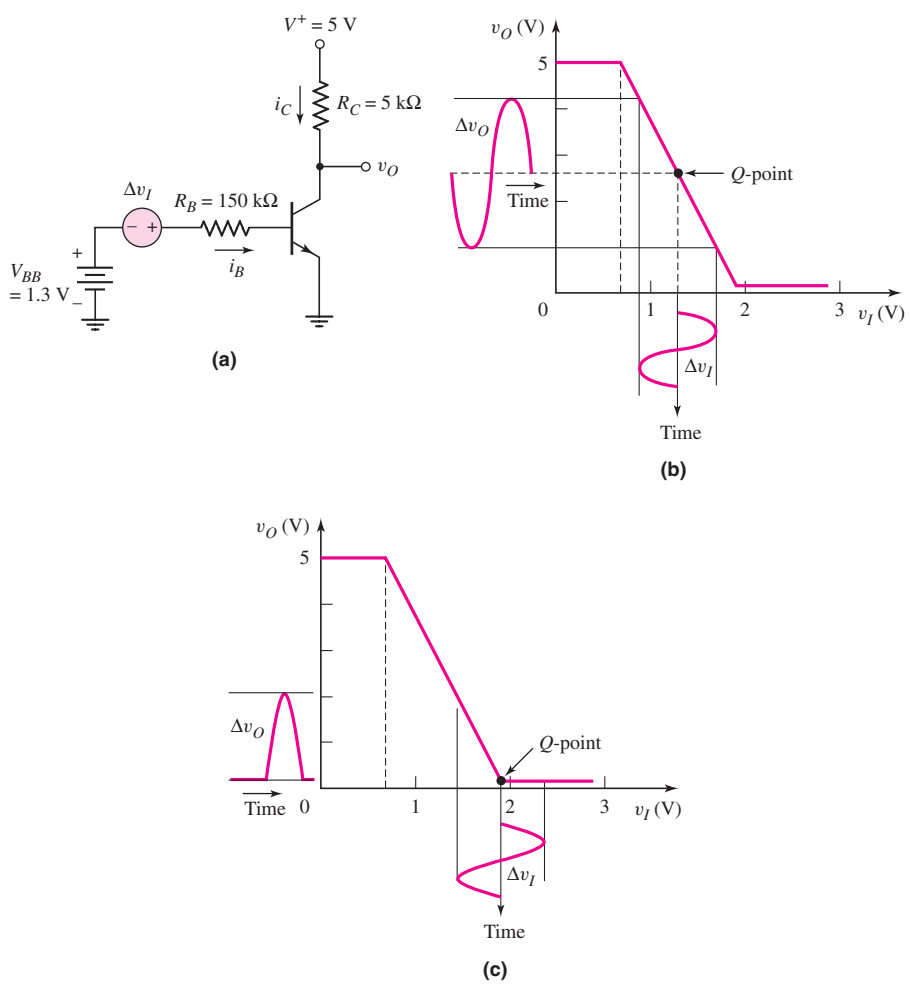

Figure 5.50 (a) The inverter circuit with both a dc and an ac input signal; (b) the dc voltage transfer characteristics, Q-point, and sinusoidal input and output signals; (c) the transfer characteristics showing improper dc biasing

Discussion: In this example, we have biased the transistor in the center of the active region. If the input signal Δv_I is a sinusoidal function as shown in Figure 5.50(b), then the output signal Δv_O is also a sinusoidal signal, which is the desired response for an analog circuit. (This assumes the magnitude of the sinusoidal input signal is not too large.) If the Q-point, or dc biasing, of the transistor were at $v_I = 1.9$ V and $v_O = 0.2$ V, as in Figure 5.50(c), the output response changes. Shown in the figure is a symmetrical sinusoidal input signal. When the input sinusoidal signal is on its positive cycle, the transistor remains biased in saturation and the output voltage does not change. During the negative half of the input signal, the transistor becomes biased in the active region, so a half sinusoidal output response is produced. The output signal is obviously not a replication of the input signal.

This discussion emphasizes the importance of properly biasing the transistor for analog or amplifier applications. The primary objective of this chapter, as stated previously, is to help readers become familiar with transistor circuits, but it is also to enable them to design the dc biasing of transistor circuits that are to be used in analog applications.

EXERCISE PROBLEM

Ex 5.13: Redesign the inverter amplifier circuit shown in Figure 5.48(a) such that the voltage amplification is $\Delta v_O/\Delta v_I = -6.5$. Let $R_B = 80\,\text{k}\Omega$, and assume $\beta = 120$ and $V_{BE}(\text{on}) = 0.7$ V. Determine the Q-point values such that the transistor is biased in the center of the active region. (Ans. For Q-point: $v_O = 2.6$ V, $v_I = 1.069$ V, $I_{BQ} = 4.61\,\mu\text{A}$; $R_C = 4.34\,\text{k}\Omega$)

The small-signal linear amplifier analysis and design are the primary objectives of the next chapter.

Test Your Understanding

TYU 5.14 For the circuit shown in Figure 5.44, assume circuit and transistor parameters of $R_B = 240\ \Omega$, $V_{CC} = 12$ V, $V_{BE}(\text{on}) = 0.7$ V, $V_{CE}(\text{sat}) = 0.1$ V, and $\beta = 75$. Assume that the load is a motor with an effective resistance of $R_C = 5\ \Omega$. Calculate the currents and voltages in the circuit, and the power dissipated in the transistor for (a) $v_I = 0$ and (b) $v_I = 12$ V. (Ans. (a) $i_B = i_C = 0$, $v_O = V_{CC} = 12$ V, $P = 0$; (b) $i_B = 47.1$ mA, $i_C = 2.38$ A, $v_O = 0.1$ V, $P = 0.271$ W)

5.4 BIPOLAR TRANSISTOR BIASING

Objective: • Investigate various biasing schemes of bipolar transistor circuits, including bias-stable biasing and integrated circuit biasing.

As mentioned in the previous section, in order to create a linear amplifier, we must keep the transistor in the forward-active mode, establish a Q-point near the center of the load line, and couple the time-varying input signal to the base. The circuit in Figure 5.47(a) may be impractical for two reasons: (1) the signal source is not connected

to ground, and (2) there may be situations where we do not want a dc base current flowing through the signal source. In this section, we will examine several alternative biasing schemes. These basic biasing circuits illustrate some desirable and some undesirable biasing characteristics. More sophisticated biasing circuits that use additional transistors and that are used in integrated circuits are discussed in Chapter 10.

5.4.1 Single Base Resistor Biasing

The circuit shown in Figure 5.51(a) is one of the simplest transistor circuits. There is a single dc power supply, and the quiescent base current is established through the resistor R_B. The **coupling capacitor** C_C acts as an open circuit to dc, isolating the signal source from the dc base current. If the frequency of the input signal is large enough and C_C is large enough, the signal can be coupled through C_C to the base with little attenuation. Typical values of C_C are generally in the range of 1 to 10 μF, although the actual value depends upon the frequency range of interest (see Chapter 7). Figure 5.51(b) is the dc equivalent circuit; the Q-point values are indicated by the additional subscript Q.

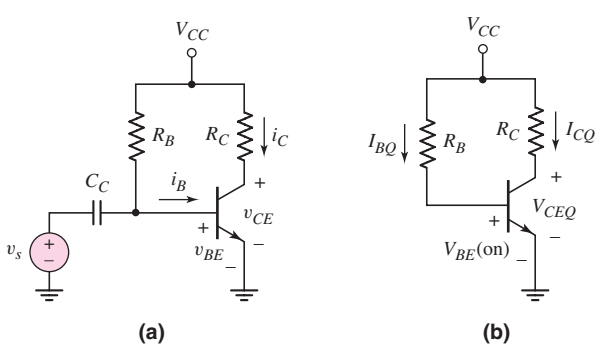

Figure 5.51 (a) Common-emitter circuit with a single bias resistor in the base and (b) dc equivalent circuit

DESIGN EXAMPLE 5.14

Objective: Design a circuit with a single-base resistor to meet a set of specifications.

Specifications: The circuit configuration to be designed is shown in Figure 5.51(b). The circuit is to be biased with $V_{CC} = +12$ V. The transistor quiescent values are to be $I_{CQ} = 1$ mA and $V_{CEQ} = 6$ V.

Choices: The transistor used in the design has nominal values of $\beta = 100$ and $V_{BE}(\text{on}) = 0.7$ V, but the current gain for this type of transistor is assumed to be in the range $50 \leq \beta \leq 150$ because of fairly wide fabrication tolerances. We will assume, in this example, that the designed resistor values are available.

Solution: The collector resistor is found from

$$R_C = \frac{V_{CC} - V_{CEQ}}{I_{CQ}} = \frac{12 - 6}{1} = 6\,\text{k}\Omega$$

The base current is

$$I_{BQ} = \frac{I_{CQ}}{\beta} = \frac{1\,\text{mA}}{100} \Rightarrow 10\,\mu\text{A}$$

and the base resistor is determined to be

$$R_B = \frac{V_{CC} - V_{BE}(\text{on})}{I_{BQ}} = \frac{12 - 0.7}{10\,\mu\text{A}} = 1.13\,\text{M}\Omega$$

The transistor characteristics, load line, and Q-point for this set of conditions are shown in Figure 5.52(a).

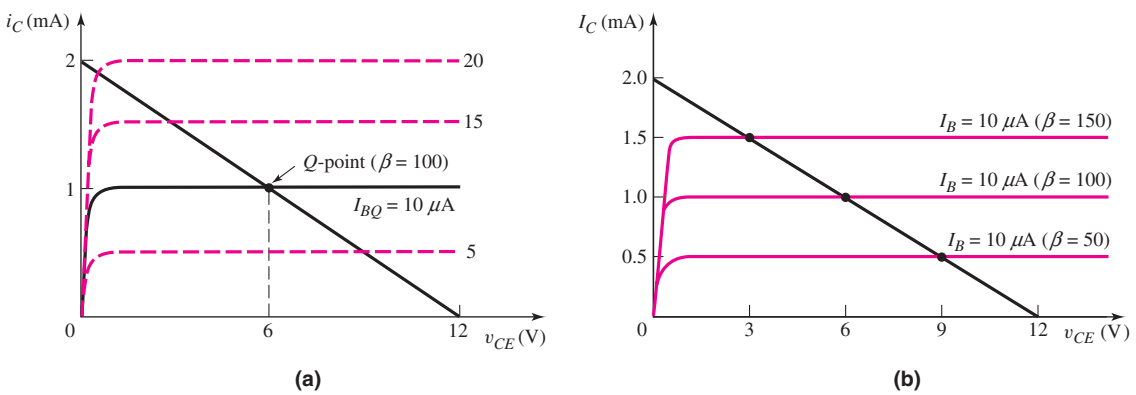

Figure 5.52 (a) Transistor characteristics and load line for the circuit in Figure 5.51 used in Design Example 5.14; (b) load line and changes in the Q-point for $\beta = 50$, 100, and 150. (Note that the base current scale changes compared to the collector current scale.)

Trade-offs: In this example, we will assume that the resistor values are fixed and will investigate the effects of the variation in transistor current gain β.

The base current is given by

$$I_{BQ} = \frac{V_{CC} - V_{BE}(\text{on})}{R_B} = \frac{12 - 0.7}{1.13\,\text{M}\Omega} = 10\,\mu\text{A (unchanged)}$$

The base current for this circuit configuration is independent of the transistor current gain.

The collector current is

$$I_{CQ} = \beta I_{BQ}$$

and the load line is found from

$$V_{CE} = V_{CC} - I_C R_C = 12 - I_C(6)$$

The load line is fixed. However, the Q-point will change. The transistor Q-point values for three values of β are given as:

β	50	100	150
Q-point values	$I_{CQ} = 0.50$ mA $V_{CEQ} = 9$ V	$I_{CQ} = 1$ mA $V_{CEQ} = 6$ V	$I_{CQ} = 1.5$ mA $V_{CEQ} = 3$ V

The various Q-points are plotted on the load line shown in Figure 5.52(b). In this figure, the collector current scale and load line are fixed. The base current scale changes as β changes.

Comment: In this circuit configuration with a single base resistor, the Q-point is not stabilized against variations in β; as β changes, the Q-point varies significantly. In our discussion of the amplifier in Example 5.13 (see Figure 5.50), we noted the importance of the placement of the Q-point. In the following two examples, we will analyze and design bias-stable circuits.

Although a value of 1.13 MΩ for R_B will establish the required base current, this resistance is too large to be used in integrated circuits. The following two examples will also demonstrate a circuit design to alleviate this problem.

EXERCISE PROBLEM

Ex 5.14: Consider the circuit shown in Figure 5.51(b). Assume $V_{CC} = 2.8$ V, $\beta = 150$, and $V_{BE}(\text{on}) = 0.7$ V. Design the circuit such that $I_{CQ} = 0.12$ mA and $V_{CEQ} = 1.4$ V. (Ans. $R_C = 11.7$ kΩ, $R_B = 2.625$ MΩ)

Test Your Understanding

[Note: In the following exercises, assume the B–E cut-in voltage is 0.7 V. Also assume the C–E saturation voltage is 0.2 V.]

TYU 5.15 Consider the circuit shown in Figure 5.53. (a) If $\beta = 120$, determine R_B such that $V_{CEQ} = 2.5$ V. (b) If the current gain varies over the range $80 \leq \beta \leq 160$, determine the variation in V_{CEQ}. (Ans. (a) $R_B = 413$ kΩ, (b) $1.67 \leq V_{CEQ} \leq 3.33$)

TYU 5.16 For the circuit shown in Figure 5.53, let $R_B = 800$ kΩ. If the range of β is between 75 and 150, determine a new value of R_C such that the Q-point will always be in the range $1 \leq V_{CEQ} \leq 4$ V. What will be the actual range of V_{CEQ} for the new value of R_C? (Ans. For $V_{CEQ} = 2.5$ V, $R_C = 4.14$ kΩ; (b) $1.66 \leq V_{CEQ} \leq 3.33$ V)

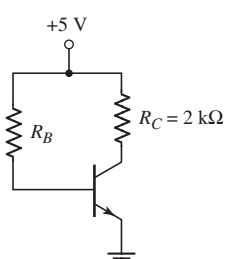

Figure 5.53 Figure for Exercises TYU 5.15 and TYU 5.16

5.4.2 Voltage Divider Biasing and Bias Stability

The circuit in Figure 5.54(a) is a classic example of discrete transistor biasing. (IC biasing is different and will be discussed in Chapter 10.) The single bias resistor R_B in the previous circuit is replaced by a pair of resistors R_1 and R_2, and an emitter resistor R_E is added. The ac signal is still coupled to the base of the transistor through the coupling capacitor C_C.

The circuit is most easily analyzed by forming a **Thevenin equivalent circuit** for the base circuit. The coupling capacitor acts as an open circuit to dc. The equivalent Thevenin voltage is

$$V_{TH} = [R_2/(R_1 + R_2)]V_{CC}$$

and the equivalent Thevenin resistance is

$$R_{TH} = R_1 \| R_2$$

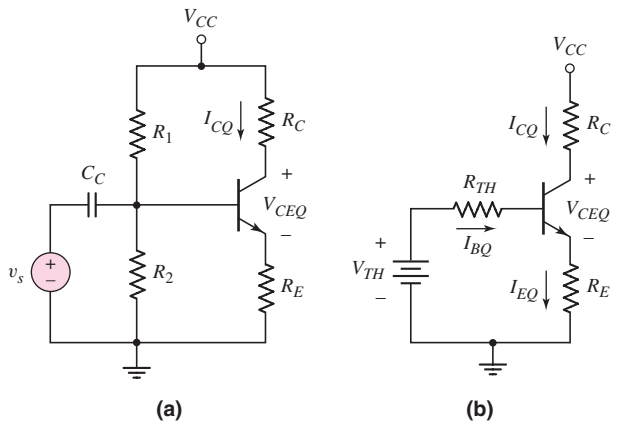

Figure 5.54 (a) A common-emitter circuit with an emitter resistor and voltage divider bias circuit in the base; (b) the dc circuit with a Thevenin equivalent base circuit

where the symbol ‖ indicates the parallel combination of resistors. Figure 5.54(b) shows the equivalent dc circuit. As we can see, this circuit is similar to those we have previously considered.

Applying Kirchhoff's law around the B–E loop, we obtain

$$V_{TH} = I_{BQ}R_{TH} + V_{BE}(\text{on}) + I_{EQ}R_E \tag{5.37}$$

If the transistor is biased in the forward-active mode, then

$$I_{EQ} = (1+\beta)I_{BQ}$$

and the base current, from Equation (5.37), is

$$I_{BQ} = \frac{V_{TH} - V_{BE}(\text{on})}{R_{TH} + (1+\beta)R_E} \tag{5.38}$$

The collector current is then

$$I_{CQ} = \beta I_{BQ} = \frac{\beta(V_{TH} - V_{BE}(\text{on}))}{R_{TH} + (1+\beta)R_E} \tag{5.39}$$

EXAMPLE 5.15

Objective: Analyze a circuit using a voltage divider bias circuit, and determine the change in the Q-point with a variation in β when the circuit contains an emitter resistor.

For the circuit given in Figure 5.54(a), let $R_1 = 56\ \text{k}\Omega$, $R_2 = 12.2\ \text{k}\Omega$, $R_C = 2\ \text{k}\Omega$, $R_E = 0.4\ \text{k}\Omega$, $V_{CC} = 10\ \text{V}$, $V_{BE}(\text{on}) = 0.7\ \text{V}$, and $\beta = 100$.

Solution: Using the Thevenin equivalent circuit in Figure 5.54(b), we have

$$R_{TH} = R_1 \| R_2 = 56 \| 12.2 = 10.0\,\text{k}\Omega$$

and

$$V_{TH} = \left(\frac{R_2}{R_1 + R_2}\right) \cdot V_{CC} = \left(\frac{12.2}{56 + 12.2}\right)(10) = 1.79\,\text{V}$$

Writing the Kirchhoff voltage law equation around the B–E loop, we obtain

$$I_{BQ} = \frac{V_{TH} - V_{BE}(\text{on})}{R_{TH} + (1+\beta)R_E} = \frac{1.79 - 0.7}{10 + (101)(0.4)} \Rightarrow 21.6\,\mu\text{A}$$

The collector current is

$$I_{CQ} = \beta I_{BQ} = (100)(21.6\,\mu\text{A}) \Rightarrow 2.16\,\text{mA}$$

and the emitter current is

$$I_{EQ} = (1+\beta)I_{BQ} = (101)(21.6\,\mu\text{A}) \Rightarrow 2.18\,\text{mA}$$

The quiescent C–E voltage is then

$$V_{CEQ} = V_{CC} - I_{CQ}R_C - I_{EQ}R_E = 10 - (2.16)(2) - (2.18)(0.4) = 4.81\,\text{V}$$

These results show that the transistor is biased in the active region.

If the current gain of the transistor were to decrease to $\beta = 50$ or increase to $\beta = 150$, we obtain the following results:

β	50	100	150
Q-point values	$I_{BQ} = 35.9\ \mu\text{A}$ $I_{CQ} = 1.80\ \text{mA}$ $V_{CEQ} = 5.67\ \text{V}$	$I_{BQ} = 21.6\ \mu\text{A}$ $I_{CQ} = 2.16\ \text{mA}$ $V_{CEQ} = 4.81\ \text{V}$	$I_{BQ} = 15.5\ \mu\text{A}$ $I_{CQ} = 2.32\ \text{mA}$ $V_{CEQ} = 4.40\ \text{V}$

The load line and Q-points are plotted in Figure 5.55. The variation in Q-points for this circuit configuration is to be compared with the variation in Q-point values shown previously in Figure 5.52(b).

For a 3 : 1 ratio in β, the collector current and collector–emitter voltage change by only a 1.29 : 1 ratio.

Comment: The voltage divider circuit of R_1 and R_2 can bias the transistor in its active region using resistor values in the low kilohm range. In contrast, single resistor biasing requires a resistor in the megohm range. In addition, the change in I_{CQ} and V_{CEQ} with a change in β has been substantially reduced compared to the change shown in Figure 5.52(b). Including an emitter resistor R_E has tended to **stabilize** the Q-point. This means that including the emitter resistor helps to stabilize the Q-point with respect to variations in β. Including the resistor R_E introduces negative feedback, as we will see in Chapter 12. Negative feedback tends to stabilize circuits.

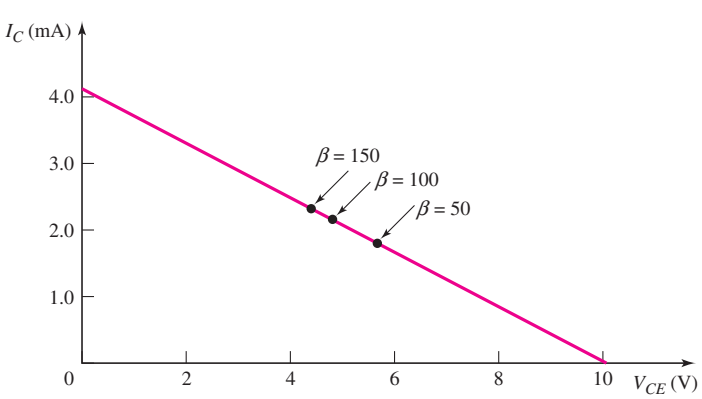

Figure 5.55 Load lines and Q-point values for Example 5.15

EXERCISE PROBLEM

Ex 5.15: For the circuit shown in Figure 5.54(a), let $V_{CC} = 3.3$ V, $R_E = 500\,\Omega$, $R_C = 4\,\text{k}\Omega$, $R_1 = 85\,\text{k}\Omega$, $R_2 = 35\,\text{k}\Omega$, and $\beta = 150$. (a) Determine R_{TH} and V_{TH}. (b) Find I_{BQ}, I_{CQ}, and V_{CEQ}. (c) Repeat part (b) for $\beta = 75$. (Ans. (a) $R_{TH} = 24.8\,\text{k}\Omega$, $V_{TH} = 0.9625$ V; (b) $I_{BQ} = 2.62\,\mu$A, $I_{CQ} = 0.393$ mA, $V_{CEQ} = 1.53$ V; (c) $I_{BQ} = 4.18\,\mu$A, $I_{CQ} = 0.314$ mA, $V_{CEQ} = 1.89$ V)

Considering Equation (5.39), the design requirement for bias stability is $R_{TH} \ll (1+\beta)R_E$. Consequently, the collector current is approximately

$$I_{CQ} \cong \frac{\beta(V_{TH} - V_{BE}(\text{on}))}{(1+\beta)R_E} \tag{5.40}$$

Normally, $\beta \gg 1$; therefore, $\beta/(1+\beta) \cong 1$, and

$$I_{CQ} \cong \frac{(V_{TH} - V_{BE}(\text{on}))}{R_E} \tag{5.41}$$

Now the quiescent collector current is essentially a function of only the dc voltages and the emitter resistance, and the Q-point is stabilized against β variations. However, if R_{TH} is too small, then R_1 and R_2 are small, and excessive power is dissipated in these resistors. The general rule is that a circuit is considered **bias stable** when

$$R_{TH} \cong 0.1(1+\beta)R_E \tag{5.42}$$

DESIGN EXAMPLE 5.16

Objective: Design a bias-stable circuit to meet a set of specifications.

Specifications: The circuit configuration to be designed is shown in Figure 5.54(a). Let $V_{CC} = 5$ V and $R_C = 1$ kΩ. Choose R_E and determine the bias resistors R_1 and R_2 such that the circuit is considered bias stable and that $V_{CEQ} = 3$ V.

Choices: Assume the transistor has nominal values of $\beta = 120$ and $V_{BE}(\text{on}) = 0.7$ V. We will choose standard resistor values and will assume that the transistor current gain varies over the range $60 \le \beta \le 180$.

Design Pointer: Typically, the voltage across R_E should be on the same order of magnitude as $V_{BE}(\text{on})$. Larger voltage drops may mean the supply voltage V_{CC} has to be increased in order to obtain the required voltage across the collector-emitter and across R_C.

Solution: With $\beta = 120$, $I_{CQ} \approx I_{EQ}$. Then, choosing a standard value of 0.51 kΩ for R_E, we find

$$I_{CQ} \cong \frac{V_{CC} - V_{CEQ}}{R_C + R_E} = \frac{5-3}{1+0.51} = 1.32\,\text{mA}$$

The voltage drop across R_E is now $(1.32)(0.51) = 0.673$ V, which is approximately the desired value. The base current is found to be

$$I_{BQ} = \frac{I_{CQ}}{\beta} = \frac{1.32}{120} \Rightarrow 11.0\,\mu\text{A}$$

Using the Thevenin equivalent circuit in Figure 5.54(b), we find

$$I_{BQ} = \frac{V_{TH} - V_{BE}(\text{on})}{R_{TH} + (1+\beta)R_E}$$

For a bias-stable circuit, $R_{TH} = 0.1(1+\beta)R_E$, or

$$R_{TH} = (0.1)(121)(0.51) = 6.17\,\text{k}\Omega$$

Then,

$$I_{BQ} = 11.0\,\mu\text{A} \Rightarrow \frac{V_{TH} - 0.7}{6.17 + (121)(0.51)}$$

which yields

$$V_{TH} = 0.747 + 0.70 = 1.447\,\text{V}$$

Now

$$V_{TH} = \left(\frac{R_2}{R_1 + R_2}\right)V_{CC} = \left(\frac{R_2}{R_1 + R_2}\right)(5) = 1.447\,\text{V}$$

or

$$\left(\frac{R_2}{R_1 + R_2}\right) = \frac{1.447}{5} = 0.2894$$

Also,

$$R_{TH} = \frac{R_1 R_2}{R_1 + R_2} = 6.17\,\text{k}\Omega = R_1\left(\frac{R_2}{R_1 + R_2}\right) = R_1(0.2894)$$

which yields

$$R_1 = 21.3\,\text{k}\Omega \quad \text{and} \quad R_2 = 8.69\,\text{k}\Omega$$

From Appendix C, we can choose standard resistor values of $R_1 = 20$ kΩ and $R_2 = 8.2$ kΩ.

Trade-offs: We will neglect, in this example, the tolerance effects of the resistors (end-of-chapter problems such as Problems 5.18 and 5.40 do include tolerance effects). We will consider the effect on the transistor Q-point values of the common-emitter current gain variation.

Using the standard resistor values, we have

$$R_{TH} = R_1 \| R_2 = 20 \| 8.2 = 5.82\,\text{k}\Omega$$

and

$$V_{TH} = \left(\frac{R_2}{R_1 + R_2}\right)(V_{CC}) = \left(\frac{8.2}{20 + 8.2}\right)(5) = 1.454\,\text{V}$$

The base current is given by

$$I_{BQ} = \left[\frac{V_{TH} - V_{BE}(\text{on})}{R_{TH} + (1+\beta)R_E}\right]$$

while the collector current is $I_{CQ} = \beta I_{BQ}$, and the collector–emitter voltage is given by

$$V_{CEQ} = V_{CC} - I_{CQ}\left[R_C + \left(\frac{1+\beta}{\beta}\right)R_E\right]$$

The Q-point values for three values of β are shown in the following table.

β	60	120	180
Q-point values	$I_{BQ} = 20.4\ \mu A$ $I_{CQ} = 1.23$ mA $V_{CEQ} = 3.13$ V	$I_{BQ} = 11.2\ \mu A$ $I_{CQ} = 1.34$ mA $V_{CEQ} = 2.97$ V	$I_{BQ} = 7.68\ \mu A$ $I_{CQ} = 1.38$ mA $V_{CEQ} = 2.91$ V

Comment: The Q-point in this example is now considered to be stabilized against variations in β, and the voltage divider resistors R_1 and R_2 have reasonable values in the kilohm range. We see that the collector current changes by only -8.2 percent when β changes by a factor of 2 (from 120 to 60), and changes by only $+3.0$ percent when β changes by $+50$ percent (from 120 to 180). Compare these changes to those of the single-base resistor design in Example 5.14.

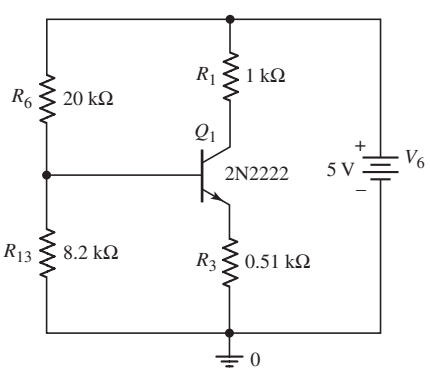

Figure 5.56 PSpice circuit schematic for Design Example 5.16

Computer Simulation: Figure 5.56 shows the PSpice circuit schematic diagram with the standard resistor values and with a standard 2N2222 transistor from the PSpice library for the circuit designed in this example. A dc analysis was performed and the resulting transistor Q-point values are shown. The collector–emitter voltage is $V_{CE} = 2.80$ V, which is close to the design value of 3 V. One reason for the difference is that the standard-valued resistors are not exactly equal to the design values. Another reason for the slight difference is that the effective β of the 2N2222 is 157 compared to the assumed value of 120.

```
**** BIPOLAR JUNCTION TRANSISTORS
NAME       Q_Q1
MODEL      Q2N2222
IB         9.25E-06
IC         1.45E-03
VBE        6.55E-01
VBC       -2.15E+00
VCE        2.80E+00
BETADC     1.57E+02
```

EXERCISE PROBLEM

Ex 5.16: In the circuit shown in Figure 5.54(a), let $V_{CC} = 5$ V, $R_E = 0.2$ kΩ, $R_C = 1$ kΩ, $\beta = 150$, and $V_{BE}(\text{on}) = 0.7$ V. Design a bias-stable circuit such that the Q-point is in the center of the load line. (Ans. $R_1 = 13$ kΩ, $R_2 = 3.93$ kΩ)

Another advantage of including an emitter resistor is that it stabilizes the Q-point with respect to temperature. To explain, we noted in Figure 1.20 that the current in a pn junction increases with increasing temperature, for a constant junction voltage. We then expect the transistor current to increase as the temperature increases. If the current in a junction increases, the junction temperature increases (because of I^2R heating), which in turn causes the current to increase, thereby further increasing the junction temperature. This phenomenon can lead to thermal runaway and to device destruction. However, from Figure 5.54(b), we see that as the current increases, the voltage drop across R_E increases. The Thevenin equivalent voltage and resistance are assumed to be essentially independent of temperature, and the temperature-induced change in the voltage drop across R_{TH} will be small. The net result is that the increased voltage drop across R_E reduces the B–E junction voltage, which then tends to stabilize the transistor current against increases in temperature.

Test Your Understanding

TYU 5.17 The parameters of the circuit shown in Figure 5.54(a) are $V_{CC} = 5$ V, $R_E = 1$ kΩ, $R_C = 4$ kΩ, $R_1 = 440$ kΩ, and $R_2 = 230$ kΩ. The transistor parameters are $\beta = 150$ and $V_{BE}(\text{on}) = 0.7$ V. (a) Find V_{TH} and R_{TH}. (b) Determine I_{CQ} and V_{CEQ}. (c) Repeat parts (a) and (b) for $\beta = 90$. (Ans. (a) $V_{TH} = 1.716$ V, $R_{TH} = 151$ kΩ; (b) $I_{CQ} = 0.505$ mA, $V_{CEQ} = 2.47$ V; (c) $I_{CQ} = 0.378$ mA, $V_{CEQ} = 3.11$ V)

TYU 5.18 Consider the circuit in Figure 5.54(a). The circuit parameters are $V_{CC} = 5$ V and $R_E = 1$ kΩ. The transistor parameters are $\beta = 150$ and $V_{BE}(\text{on}) = 0.7$ V. (a) Design a bias-stable circuit such that $I_{CQ} = 0.40$ mA and $V_{CEQ} = 2.7$ V. (b) Using the results of part (a), determine I_{CQ} and V_{CEQ} for $\beta = 90$. (Ans. (a) $R_1 = 66$ kΩ, $R_2 = 19.6$ kΩ, $R_C = 4.74$ kΩ; (b) $I_{CQ} = 0.376$ mA, $V_{CEQ} = 2.84$ V)

5.4.3 Positive and Negative Voltage Biasing

There are applications in which biasing a transistor with both positive and negative dc voltages is desirable. We will see this especially in Chapter 11 when we are discussing the differential amplifier. Biasing with dual supplies allows us, in some applications, to eliminate the coupling capacitor and allows dc input voltages as input signals. The following example demonstrates this biasing scheme.

EXAMPLE 5.17

Objective: Design a bias-stable pnp transistor circuit to meet a set of specifications.

Specifications: The circuit configuration to be designed is shown in Figure 5.57(a). The transistor Q-point values are to be: $V_{ECQ} = 7$ V, $I_{CQ} \cong 0.5$ mA, and $V_{RE} \cong 1$ V.

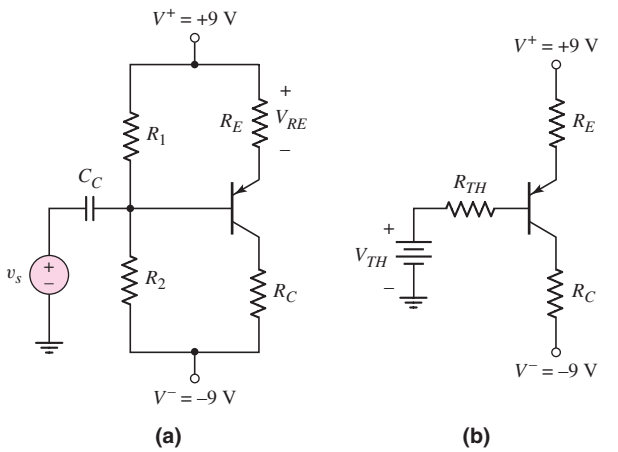

Figure 5.57 (a) Circuit for Example 5.17 and (b) Thevenin equivalent circuit

Choices: Assume transistor parameters of $\beta = 80$ and $V_{EB}(\text{on}) = 0.7$ V. Standard resistor values are to be used in the final design.

Solution: The Thevenin equivalent circuit is shown in Figure 5.57(b). The Thevenin equivalent resistance is $R_{TH} = R_1 \| R_2$ and the Thevenin equivalent voltage, measured with respect to ground, is given by

$$V_{TH} = \left(\frac{R_2}{R_1 + R_R}\right)(V^+ - V^-) + V^-$$

$$= \frac{1}{R_1}\left(\frac{R_1 R_2}{R_1 + R_2}\right)(V^+ - V^-) + V^-$$

For $V_{RE} \cong 1$ V and $I_{CQ} \cong 0.5$ mA, then we can set

$$R_E = \frac{1}{0.5} = 2\,\text{k}\Omega$$

For a bias stable circuit, we want

$$R_{TH} = \frac{R_1 R_2}{R_1 + R_2} = (0.1)(1 + \beta)R_E$$

$$= (0.1)(81)(2) = 16.2\,\text{k}\Omega$$

Then the Thevenin equivalent voltage can be written as

$$V_{TH} = \frac{1}{R_1}(16.2)[9 - (-9)] + (-9) = \frac{1}{R_1}(291.6) - 9$$

The KVL equation around the E–B loop is given by

$$V^+ = I_{EQ}R_E + V_{EB}(\text{on}) + I_{BQ}R_{TH} + V_{TH}$$

The transistor is to be biased in the forward-active mode so that $I_{EQ} = (1 + \beta)I_{BQ}$. We then have

$$V^+ = (1 + \beta)I_{BQ}R_E + V_{EB}(\text{on}) + I_{BQ}R_{TH} + V_{TH}$$

For $I_{CQ} = 0.5$ mA, then $I_{BQ} = 0.00625$ mA so we can write

$$9 = (81)(0.00625)(2) + 0.7 + (0.00625)(16.2) + \frac{1}{R_1}(291.6) - 9$$

We find $R_1 = 18.0\,\text{k}\Omega$. Then, from $R_{TH} = R_1 \| R_2 = 16.2\,\text{k}\Omega$, we find $R_2 = 162\,\text{k}\Omega$.

For $I_{CQ} = 0.5$ mA, then $I_{EQ} = 0.506$ mA. The KVL equation around the E–C loop yields

$$V^+ = I_{EQ}R_E + V_{ECQ} + I_{CQ}R_C + V^-$$

or

$$9 = (0.506)(2) + 7 + (0.50)R_C + (-9)$$

which yields

$$R_C \cong 20\,\text{k}\Omega$$

Trade-offs: All resistor values are standard values except for $R_2 = 162\,\text{k}\Omega$. A standard discrete value of 160 kΩ is available. However, because of the bias-stable design, the Q-point will not change significantly. The change in Q-point values with a change in transistor current gain β is considered in end-of-chapter problems such as Problems 5.31 and 5.34.

Comment: In many cases, specifications such as a collector current level or an emitter–collector voltage value are not absolute, but are given as approximate values. For this reason, the emitter resistor, for example, is determined to be 2 kΩ, which is a standard discrete resistor value. The final bias resistor values are also chosen to be standard values. However, these small changes compared to the calculated resistor values will not change the Q-point values significantly.

EXERCISE PROBLEM

Ex 5.17: Consider the circuit shown in Figure 5.58. The transistor parameters are $\beta = 150$ and $V_{BE}(\text{on}) = 0.7$ V. The circuit parameters are $R_E = 2\,\text{k}\Omega$ and $R_C = 10\,\text{k}\Omega$. Design a bias-stable circuit such that the quiescent output voltage is zero. What are the values of I_{CQ} and V_{CEQ}? (Ans. $I_{CQ} = 0.5$ mA, $V_{CEQ} = 3.99$ V, $R_1 = 167\,\text{k}\Omega$, $R_2 = 36.9\,\text{k}\Omega$)

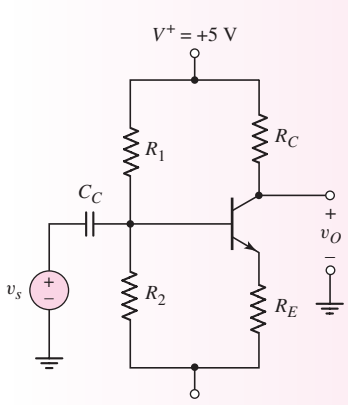

Figure 5.58 Figure for Exercise Ex 5.17

5.4.4 Integrated Circuit Biasing

The resistor biasing of transistor circuits considered up to this point is primarily applied to discrete circuits. For integrated circuits, we would like to eliminate as many resistors as possible since, in general, they require a larger surface area than transistors.

A bipolar transistor can be biased by using a constant-current source I_Q, as shown in Figure 5.59. The advantages of this circuit are that the emitter current is independent of β and R_B, and the collector current and C–E voltage are essentially independent of transistor current gain, for reasonable values of β. The value of R_B can be increased, thus increasing the input resistance at the base, without jeopardizing the bias stability.

The constant current source can be implemented by using transistors as shown in Figure 5.60. The transistor Q_1 is a diode-connected transistor, but still operates in the forward-active mode. The transistor Q_2 must also operate in the forward-active mode ($V_{CE} \geq V_{BE}$(on)).

Current I_1 is called the reference current and is found by writing Kirchhoff's voltage law equation around the R_1–Q_1 loop. We have

$$0 = I_1 R_1 + V_{BE}\,(\text{on}) + V^- \tag{5.43(a)}$$

which yields

$$I_1 = \frac{-(V^- + V_{BE}\,(\text{on}))}{R_1} \tag{5.43(b)}$$

Since $V_{BE1} = V_{BE2}$, the circuit mirrors the reference current in the left branch into the right branch. The circuit of R_1, Q_1, and Q_2 is then referred to as a current mirror.

Summing the currents at the collector of Q_1 gives

$$I_1 = I_{C1} + I_{B1} + I_{B2} \tag{5.44}$$

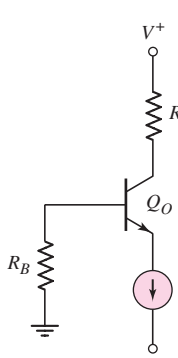

Figure 5.59 Bipolar transistor biased with a constant-current source

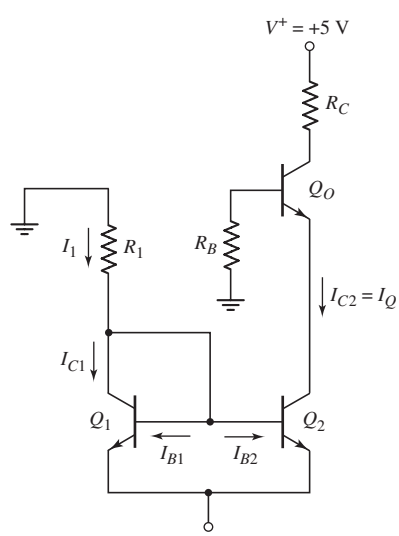

Figure 5.60 Transistor Q_O biased with a constant current source. The transistors Q_1 and Q_2 form a current mirror.

The B–E voltages of Q_1 and Q_2 are equal. If Q_1 and Q_2 are identical transistors and are held at the same temperature, then $I_{B1} = I_{B2}$ and $I_{C1} = I_{C2}$. Equation (5.44) can then be written as

$$I_1 = I_{C1} + 2I_{B2} = I_{C2} + \frac{2I_{C2}}{\beta} = I_{C2}\left(1 + \frac{2}{\beta}\right) \tag{5.45}$$

Solving for I_{C2}, we find

$$I_{C2} = I_Q = \frac{I_1}{\left(1 + \frac{2}{\beta}\right)} \tag{5.46}$$

This current biases the transistor Q_O in the active region.

The circuit with Q_1, Q_2, and R_1 is referred to as a two-transistor current source.

EXAMPLE 5.18

Objective: Determine the currents in a two-transistor current source.

For the circuit in Figure 5.60, the circuit and transistor parameters are: $R_1 = 10\,\text{k}\Omega$, $\beta = 50$, and $V_{BE}(\text{on}) = 0.7\,\text{V}$.

Solution: The reference current is

$$I_1 = \frac{-(V^- + V_{BE}\,(\text{on}))}{R_1} = \frac{-((-5) + 0.7)}{10} = 0.43\,\text{mA}$$

From Equation (5.46), the bias current I_Q is

$$I_{C2} = I_Q = \frac{I_1}{\left(1 + \frac{2}{\beta}\right)} = \frac{0.43}{\left(1 + \frac{2}{50}\right)} = 0.413\,\text{mA}$$

The base currents are then

$$I_{B1} = I_{B2} = \frac{I_{C2}}{\beta} = \frac{0.413}{50} \Rightarrow 8.27\,\mu\text{A}$$

Comment: For relatively large values of current gain β, the bias current I_Q is essentially the same as the reference current I_1.

EXERCISE PROBLEM

Ex 5.18: In the circuit shown in Figure 5.60, the parameters are $V^+ = 3.3\,\text{V}$, $V^- = -3.3\,\text{V}$, and $R_B = 0$. The transistor parameters are $\beta = 60$ and $V_{BE}(\text{on}) = 0.7\,\text{V}$. Design the circuit such that $I_{CQ}(Q_O) = 0.12\,\text{mA}$ and $V_{CEQ}(Q_O) = 1.6\,\text{V}$. What are the values of I_Q and I_1? (Ans. $I_Q = 0.122\,\text{mA}$, $I_1 = 0.126\,\text{mA}$, $R_1 = 20.6\,\text{k}\Omega$, $R_C = 20\,\text{k}\Omega$)

As mentioned, constant-current biasing is used almost exclusively in integrated circuits. As we will see in Part 2 of the text, circuits in integrated circuits use a minimum number of resistors, and transistors are often used to replace these resistors. Transistors take up much less area than resistors on an IC chip, so it's advantageous to minimize the number of resistors.

Test Your Understanding

TYU 5.19 The parameters of the circuit shown in Figure 5.57(a) are $V^+ = 5$ V, $V^- = -5$ V, $R_E = 0.5\,\text{k}\Omega$, and $R_C = 4.5\,\text{k}\Omega$. The transistor parameters are $\beta = 120$ and $V_{EB}(\text{on}) = 0.7$ V. Design a bias-stable circuit such that the Q-point is in the center of the load line. What are the values of I_{CQ} and V_{ECQ}? (Ans. $I_{CQ} = 1\,\text{mA}$, $V_{ECQ} = 5$ V, $R_1 = 6.92\,\text{k}\Omega$, $R_2 = 48.1\,\text{k}\Omega$)

TYU 5.20 For Figure 5.59, the circuit parameters are $I_Q = 0.25\,\text{mA}$, $V^+ = 2.5$ V, $V^- = -2.5$ V, $R_B = 75\,\text{k}\Omega$, and $R_C = 4\,\text{k}\Omega$. The transistor parameters are $I_S = 3 \times 10^{-14}$ A and $\beta = 120$. (a) Determine the dc voltage at the base of the transistor and also V_{CEQ}. (b) Repeat part (a) for $\beta = 60$. (Ans. (a) $V_B = -0.155$ V, $V_{CEQ} = 2.26$V; (b) $V_B = -0.307$ V, $V_{CEQ} = 2.42$ V)

5.5 MULTISTAGE CIRCUITS

Objective: • Consider the dc biasing of multistage or multitransistor circuits.

Most transistor circuits contain more than one transistor. We can analyze and design these multistage circuits in much the same way as we studied single-transistor circuits. As an example, Figure 5.61 shows an npn transistor, Q_1, and a pnp bipolar transistor, Q_2, in the same circuit.

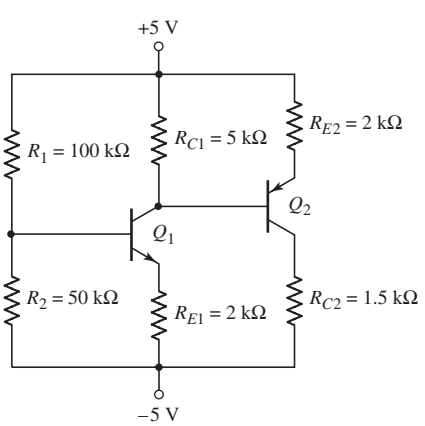

Figure 5.61 A multistage transistor circuit

EXAMPLE 5.19

Objective: Calculate the dc voltages at each node and the dc currents through the elements in a multistage circuit.

For the circuit in Figure 5.61, assume the B–E turn-on voltage is 0.7 V and $\beta = 100$ for each transistor.

Solution: The Thevenin equivalent circuit of the base circuit of Q_1 is shown in Figure 5.62. The various currents and nodal voltages are defined as shown. The Thevenin resistance and voltage are

$$R_{TH} = R_1 \| R_2 = 100 \| 50 = 33.3 \text{ k}\Omega$$

and

$$V_{TH} = \left(\frac{R_2}{R_1 + R_2}\right)(10) - 5 = \left(\frac{50}{150}\right)(10) - 5 = -1.67 \text{ V}$$

Kirchhoff's voltage law equation around the B–E loop of Q_1 is

$$V_{TH} = I_{B1}R_{TH} + V_{BE}\,(\text{on}) + I_{E1}R_{E1} - 5$$

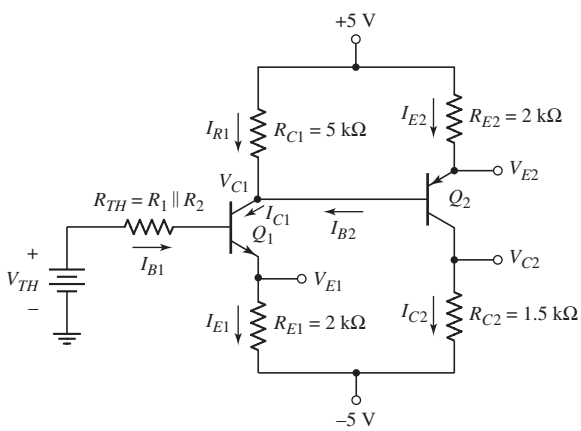

Figure 5.62 Multistage transistor circuit with a Thevenin equivalent circuit in the base of Q_1

Noting that $I_{E1} = (1 + \beta)I_{B1}$, we have

$$I_{B1} = \frac{-1.67 + 5 - 0.7}{33.3 + (101)(2)} \Rightarrow 11.2\,\mu\text{A}$$

Therefore,

$$I_{C1} = 1.12\,\text{mA}$$

and

$$I_{E1} = 1.13\,\text{mA}$$

Summing the currents at the collector of Q_1, we obtain

$$I_{R1} + I_{B2} = I_{C1}$$

which can be written as

$$\frac{5 - V_{C1}}{R_{C1}} + I_{B2} = I_{C1} \tag{5.47}$$

The base current I_{B2} can be written in terms of the emitter current I_{E2}, as follows:

$$I_{B2} = \frac{I_{E2}}{1 + \beta} = \frac{5 - V_{E2}}{(1 + \beta)R_{E2}} = \frac{5 - (V_{C1} + 0.7)}{(1 + \beta)R_{E2}} \tag{5.48}$$

Substituting Equation (5.48) into (5.47), we obtain

$$\frac{5 - V_{C1}}{R_{C1}} + \frac{5 - (V_{C1} + 0.7)}{(1 + \beta)R_{E2}} = I_{C1} = 1.12\,\text{mA}$$

which can be solved for V_{C1} to yield

$$V_{C1} = -0.482\,\text{V}$$

Then,

$$I_{R1} = \frac{5 - (-0.482)}{5} = 1.10\,\text{mA}$$

To find V_{E2}, we have

$$V_{E2} = V_{C1} + V_{EB}(\text{on}) = -0.482 + 0.7 = 0.218\,\text{V}$$

The emitter current I_{E2} is

$$I_{E2} = \frac{5 - 0.218}{2} = 2.39\,\text{mA}$$

Then,

$$I_{C2} = \left(\frac{\beta}{1 + \beta}\right) I_{E2} = \left(\frac{100}{101}\right)(2.39) = 2.37\,\text{mA}$$

and

$$I_{B2} = \frac{I_{E2}}{1 + \beta} = \frac{2.39}{101} \Rightarrow 23.7\,\mu\text{A}$$

The remaining nodal voltages are

$$V_{E1} = I_{E1}R_{E1} - 5 = (1.13)(2) - 5 \Rightarrow V_{E1} = -2.74\,\text{V}$$

and

$$V_{C2} = I_{C2}R_{C2} - 5 = (2.37)(1.5) - 5 = -1.45\,\text{V}$$

We then find that

$$V_{CE1} = V_{C1} - V_{E1} = -0.482 - (-2.74) = 2.26\,\text{V}$$

and that

$$V_{EC2} = V_{E2} - V_{C2} = 0.218 - (-1.45) = 1.67\,\text{V}$$

Comment: These results show that both Q_1 and Q_2 are biased in the forward-active mode, as originally assumed. However, when we consider the ac operation of this circuit as an amplifier in the next chapter, we will see that a better design would increase the value of V_{EC2}.

EXERCISE PROBLEM

Ex 5.19: In the circuit shown in Figure 5.61, determine new values of R_{C1} and R_{C2} such that $V_{CEQ1} = 3.25$ V and $V_{ECQ2} = 2.5$ V. (Ans. $R_{C1} = 4.08$ kΩ, $R_{C2} = 1.97$ kΩ)

EXAMPLE 5.20

Objective: Design the circuit shown in Figure 5.63, called a cascode circuit, to meet the following specifications: $V_{CE1} = V_{CE2} = 2.5$ V, $V_{RE} = 0.7$ V, $I_{C1} \cong I_{C2} \cong 1$ mA, and $I_{R1} \cong I_{R2} \cong I_{R3} \cong 0.10$ mA.

Solution: The initial design will neglect base currents. We can then define $I_{\text{Bias}} = I_{R1} = I_{R2} = I_{R3} = 0.10$ mA. Then

$$R_1 + R_2 + R_3 = \frac{V^+}{I_{\text{Bias}}} = \frac{9}{0.10} = 90\,\text{k}\Omega$$

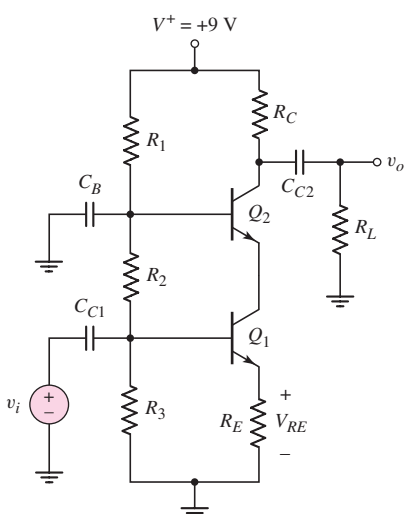

Figure 5.63 A bipolar cascode circuit for Example 5.20

The voltage at the base of Q_1 is

$$V_{B1} = V_{RE} + V_{BE}(\text{on}) = 0.7 + 0.7 = 1.4\,\text{V}$$

Then

$$R_3 = \frac{V_{B1}}{I_{\text{Bias}}} = \frac{1.4}{0.10} = 14\,\text{k}\Omega$$

The voltage at the base of Q_2 is

$$V_{B2} = V_{RE} + V_{CE1} + V_{BE}(\text{on}) = 0.7 + 2.5 + 0.7 = 3.9\,\text{V}$$

Then

$$R_2 = \frac{V_{B2} - V_{B1}}{I_{\text{Bias}}} = \frac{3.9 - 1.4}{0.10} = 25\,\text{k}\Omega$$

We then obtain

$$R_1 = 90 - 25 - 14 = 51\,\text{k}\Omega$$

The emitter resistor R_E can be found as

$$R_E = \frac{V_{RE}}{I_{C1}} = \frac{0.7}{1} = 0.7\,\text{k}\Omega$$

The voltage at the collector of Q_2 is

$$V_{C2} = V_{RE} + V_{CE1} + V_{CE2} = 0.7 + 2.5 + 2.5 = 5.7\,\text{V}$$

Then

$$R_C = \frac{V^+ - V_{C2}}{I_{C2}} = \frac{9 - 5.7}{1} = 3.3\,\text{k}\Omega$$

Comment: By neglecting base currents, the design of this circuit is straightforward. A computer analysis using PSpice, for example, will verify the design or show that small changes need to be made to meet the design specifications.

We will see the cascode circuit again in Section 6.9.3 of the next chapter.

One advantage of the cascode circuit will be determined in Chapter 7. The cascode circuit has a larger bandwidth than just a simple common-emitter amplifier.

EXERCISE PROBLEM

Ex 5.20: For the circuit shown in Figure 5.63, the circuit parameters are $V^+ = 12$ V and $R_E = 2\,\text{k}\Omega$, and the transistor parameters are $\beta = 120$ and $V_{BE}(\text{on}) = 0.7$ V. Redesign the circuit such that $I_{C1} \cong I_{C2} \cong 0.5\,\text{mA}$, $I_{R1} \cong I_{R2} \cong I_{R3} \cong 0.05\,\text{mA}$, and $V_{CE1} \cong V_{CE2} \cong 4\,\text{V}$. (Ans. $R_1 = 126\ \text{k}\Omega$, $R_2 = 80\ \text{k}\Omega$, $R_3 = 34\ \text{k}\Omega$, and $R_C = 6\ \text{k}\Omega$)

COMPUTER ANALYSIS EXERCISE

PS 5.4: (a) Verify the cascode circuit design in Example 5.20 using a PSpice simulation. Use standard transistors. (b) Repeat part (a) using standard resistor values.

5.6 DESIGN APPLICATION: DIODE THERMOMETER WITH A BIPOLAR TRANSISTOR

Objective: • Incorporate a bipolar transistor in a design application that enhances the simple diode thermometer design discussed in Chapter 1.

Specifications: The electronic thermometer is to operate over a temperature range of 0 to 100 °F.

Design Approach: The output-diode voltage developed in the diode thermometer in Figure 1.48 is to be applied to the base–emitter junction of an npn bipolar transistor to enhance the voltage over the temperature range. The bipolar transistor will be held at a constant temperature.

Choices: Assume an npn bipolar transistor with $I_S = 10^{-12}$ A is available.

Solution: From the design in Chapter 1, the diode voltage is given by

$$V_D = 1.12 - 0.522\left(\frac{T}{300}\right)$$

where T is in kelvins.

Consider the circuit shown in Figure 5.64. We assume that the diode is in a variable temperature environment while the rest of the circuit is held at room temperature. Neglecting the bipolar transistor base current, we have

$$V_D = V_{BE} + I_C R_E \tag{5.49}$$

We can write

$$I_C = I_S e^{V_{BE}/V_T} \tag{5.50}$$

so that Equation (5.49) becomes

$$\frac{V_D - V_{BE}}{R_E} = I_S e^{V_{BE}/V_T} \tag{5.51}$$

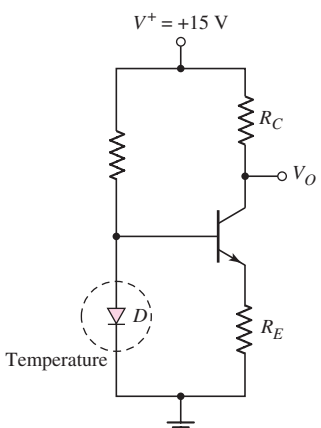

Figure 5.64 Design application circuit to measure output voltage of diode versus temperature

and

$$V_O = 15 - I_C R_C \tag{5.52}$$

From Chapter 1, we have the following:

T (°F)	V_D (V)
0	0.6760
40	0.6372
80	0.5976
100	0.5790

If we assume that $I_S = 10^{-12}$ A for the transistor, then from Equations (5.50), (5.51), and (5.52), we find

T (°F)	V_{BE} (V)	I_C (mA)	V_O (V)
0	0.5151	0.402	4.95
40	0.5092	0.320	7.00
80	0.5017	0.240	9.00
100	0.4974	0.204	9.90

Comment: Figure 5.65(a) shows the diode voltage versus temperature and Figure 5.65(b) now shows the output voltage versus temperature from the bipolar transistor circuit. We can see that the transistor circuit provides a voltage gain. This voltage gain is the desired characteristic of the transistor circuit.

Discussion: We can see from the equations that the collector current is not a linear function of the base–emitter voltage or diode voltage. This effect implies that the transistor output voltage is also not exactly a linear function of temperature. The line drawn in Figure 5.65(b) is a good linear approximation. We will obtain a better circuit design using operational amplifiers in Chapter 9.

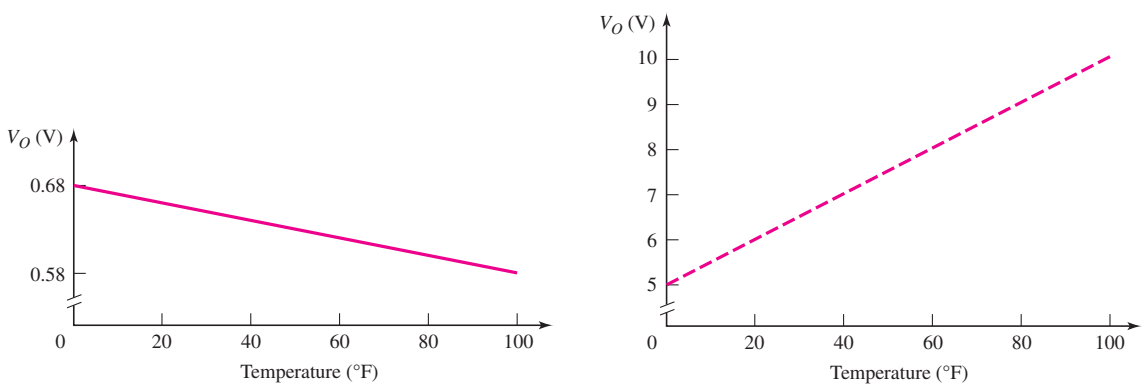

Figure 5.65 (a) Diode voltage versus temperature and (b) circuit output voltage versus temperature

5.7 SUMMARY

- In this chapter, we considered the structure, characteristics, and properties of the bipolar transistor. Both npn and pnp complementary bipolar transistors can be formed. The defining transistor action is that the voltage across two terminals (base and emitter) controls the current in the third terminal (collector).
- The four modes of operation are: forward-active, cutoff, saturation, and inverse-active. In the forward-active mode, the B–E junction is forward biased, the B–C junction is reverse biased, and the collector and base currents are related by the common-emitter current gain β. When the transistor is cut off, all currents are zero. In the saturation mode, the collector current is no longer a function of base current.
- The dc analysis and design techniques of bipolar transistor circuits were emphasized in this chapter. We continued to use the piecewise linear model of the pn junction in these analyses and designs. Techniques to design a transistor circuit with a stable Q-point were developed.
- An introduction to dc biasing of integrated circuits using constant current circuits was presented.

- Basic applications of the transistor include switching currents and voltages, performing digital logic functions, and amplifying time-varying signals. The amplifying characteristics of bipolar transistor circuits are considered in detail in the next chapter.
- An introduction to dc biasing in mutistage circuits was given.
- As an application, the bipolar transistor was incorporated in a circuit design that enhances the simple diode thermometer discussed in Chapter 1.

CHECKPOINT

After studying this chapter, the reader should have the ability to:

- ✓ Understand and describe the structure and general current–voltage characteristics for both the npn and pnp bipolar transistors.
- ✓ Apply the piecewise linear model to the dc analysis and design of various bipolar transistor circuits, including the understanding of the load line.
- ✓ Define the four modes of operation of a bipolar transistor.
- ✓ Qualitatively understand how a transistor circuit can be used to switch currents and voltages, to perform digital logic functions, and to amplify time-varying signals.
- ✓ Design the dc biasing of a transistor circuit to achieve specified dc currents and voltages, and to stabilize the Q-point against transistor parameter variations.
- ✓ Apply the dc analysis and design techniques to multistage transistor circuits.

REVIEW QUESTIONS

1. Describe the basic structure and operation of npn and pnp bipolar transistors.
2. What are the bias voltages that need to be applied to an npn bipolar transistor such that the transistor is biased in the forward-active mode?
3. Define the conditions for cutoff, forward-active mode, and saturation mode for a pnp bipolar transistor.
4. Define common-base current gain and common-emitter current gain.
5. Discuss the difference between the ac and dc common-emitter current gains.
6. State the relationships between collector, emitter, and base currents in a bipolar transistor biased in the forward-active mode.
7. Define Early voltage and collector output resistance.
8. Describe a simple common-emitter circuit with an npn bipolar transistor and discuss the relation between collector–emitter voltage and input base current.
9. Describe the parameters that define a load line. Define Q-point.
10. What are the steps used to analyze the dc response of a bipolar transistor circuit?
11. Describe how an npn transistor can be used to switch an LED diode on and off.
12. Describe a bipolar transistor NOR logic circuit.
13. Describe how a transistor can be used to amplify a time-varying voltage.
14. Discuss the advantages of using resistor voltage divider biasing compared to a single base resistor.
15. How can the Q-point be stabilized against variations in transistor parameters?
16. What is the principal difference between biasing techniques used in discrete transistor circuits and integrated circuits?

PROBLEMS

[Note: In the following problems, unless otherwise stated, assume $V_{BE}(\text{on}) = 0.7$ V and $V_{CE}(\text{sat}) = 0.2$ V for npn transistors, and assume $V_{EB}(\text{on}) = 0.7$ V and $V_{EC}(\text{sat}) = 0.2$ V for pnp transistors.]

Section 5.1 Basic Bipolar Junction Transistor

5.1 (a) In a bipolar transistor biased in the forward-active region, the base current is $i_B = 2.8\,\mu$A and the emitter current is $i_E = 325\,\mu$A. Determine β, α, and i_C. (b) Repeat part (a) if $i_B = 20\,\mu$A and $i_E = 1.80$ mA.

5.2 (a) A bipolar transistor is biased in the forward-active mode. The collector current is $i_C = 726\,\mu$A and the emitter current is $i_E = 732\,\mu$A. Determine β, α, and i_B. (b) Repeat part (a) if $i_C = 2.902$ mA and $i_E = 2.961$ mA.

5.3 (a) The range of β for a particular type of transistor is $110 \le \beta \le 180$. Determine the corresponding range of α. (b) If the base current is 50 μA, determine the range of collector current.

5.4 (a) A bipolar transistor is biased in the forward-active mode. The measured parameters are $i_E = 1.25$ mA and $\beta = 150$. Determine i_B, i_C, and α. (b) Repeat part (a) for $i_E = 4.52$ mA and $\beta = 80$.

5.5 (a) For the following values of common-base current gain α, determine the corresponding common-emitter current gain β:

α	0.90	0.950	0.980	0.990	0.995	0.9990
β						

(b) For the following values of common-emitter current gain β, determine the corresponding common-base current gain α:

β	20	50	100	150	220	400
α						

5.6 An npn transistor with $\beta = 80$ is connected in a common-base configuration as shown in Figure P5.6. (a) The emitter is driven by a constant-current source with $I_E = 1.2$ mA. Determine I_B, I_C, α, and V_C. (b) Repeat part (a) for $I_E = 0.80$ mA. (c) Repeat parts (a) and (b) for $\beta = 120$.

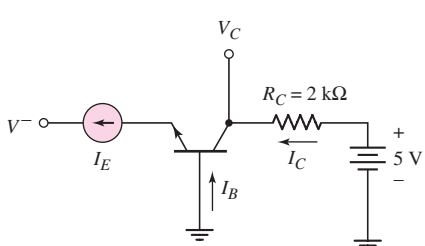

Figure P5.6

5.7 The emitter current in the circuit in Figure P5.6 is $I_E = 0.80\,\text{mA}$. The transistor parameters are $\alpha = 0.9910$ and $I_{EO} = 5 \times 10^{-14}\,\text{A}$. Determine I_B, I_C, V_{BE}, and V_C.

5.8 A pnp transistor with $\beta = 60$ is connected in a common-base configuration as shown in Figure P5.8. (a) The emitter is driven by a constant-current source with $I_E = 0.75\,\text{mA}$. Determine I_B, I_C, α, and V_C. (b) Repeat part (a) if $I_E = 1.5\,\text{mA}$. (c) Is the transistor biased in the forward-active mode for both parts (a) and (b)? Why or why not?

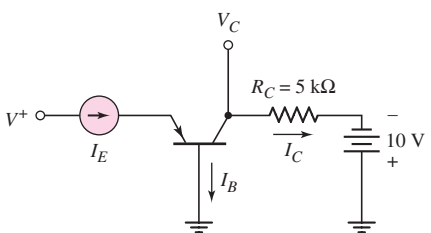

Figure P5.8

5.9 (a) The pnp transistor shown in Figure P5.8 has a common-base current gain $\alpha = 0.9860$. Determine the emitter current such that $V_C = -1.2\,\text{V}$. What is the base current? (b) Using the results of part (a) and assuming $I_{EO} = 2 \times 10^{-15}\,\text{A}$, determine V_{EB}.

5.10 An npn transistor has a reverse-saturation current of $I_S = 5 \times 10^{-15}\,\text{A}$ and a current gain of $\beta = 125$. The transistor is biased at $v_{BE} = 0.615\,\text{V}$. Determine i_B, i_C, and i_E.

5.11 Two pnp transistors, fabricated with the same technology, have different junction areas. Both transistors are biased with an emitter-base voltage of $v_{EB} = 0.650\,\text{V}$ and have emitter currents of 0.50 and 12.2 mA. Find I_{EO} for each device. What are the relative junction areas?

5.12 The collector currents in two transistors, A and B, are both $i_C = 275\,\mu\text{A}$. For transistor A, $I_{SA} = 8 \times 10^{-16}\,\text{A}$. The base–emitter area of transistor B is 4 times that of transistor A. Determine I_{SB} and the base–emitter voltage of each transistor.

5.13 A BJT has an Early voltage of 80 V. The collector current is $I_C = 0.60\,\text{mA}$ at a collector–emitter voltage of $V_{CE} = 2\,\text{V}$. (a) Determine the collector current at $V_{CE} = 5\,\text{V}$. (b) What is the output resistance?

5.14 The open-emitter breakdown voltage of a B–C junction is $BV_{CBO} = 60\,\text{V}$. If $\beta = 100$ and the empirical constant is $n = 3$, determine the C–E breakdown voltage in the open-base configuration.

5.15 In a particular circuit application, the minimum required breakdown voltages are $BV_{CBO} = 220\,\text{V}$ and $BV_{CEO} = 56\,\text{V}$. If $n = 3$, determine the maximum allowed value of β.

5.16 A particular transistor circuit design requires a minimum open-base breakdown voltage of $BV_{CEO} = 50\,\text{V}$. If $\beta = 50$ and $n = 3$, determine the minimum required value of BV_{CBO}.

Section 5.2 DC Analysis of Transistor Circuits

5.17 For all the transistors in Figure P5.17, $\beta = 75$. The results of some measurements are indicated on the figures. Find the values of the other labeled currents, voltages, and/or resistor values.

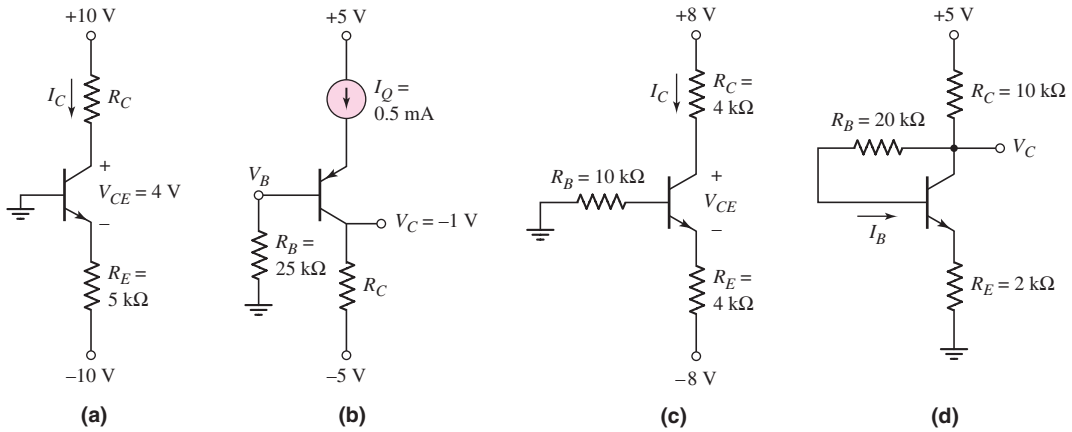

Figure P5.17

5.18 The emitter resistor values in the circuits show in Figures P5.17(a) and (c) may vary by ±5 percent from the given value. Determine the range of calculated parameters.

5.19 Consider the two circuits in Figure P5.19. The parameters of each transistor are $I_S = 5 \times 10^{-16}$ A and $\beta = 90$. Determine V_{BB} in each circuit such that $V_{CE} = 1.10$ V.

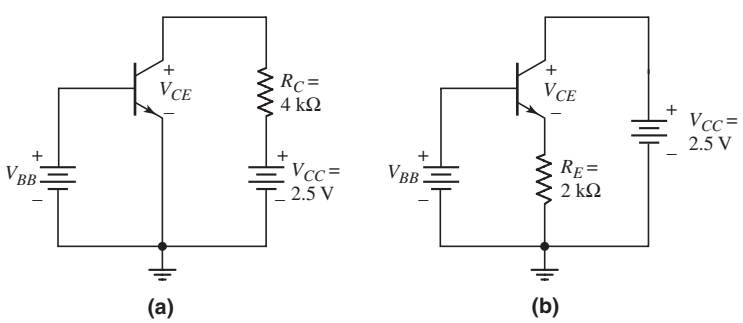

Figure P5.19

5.20 The current gain for each transistor in the circuits shown in Figure P5.20 is $\beta = 120$. For each circuit, determine I_C and V_{CE}.

5.21 Consider the circuits in Figure P5.21. For each transistor, $\beta = 120$. Determine I_C and V_{EC} for each circuit.

5.22 (a) The circuit and transistor parameters for the circuit shown in Figure 5.20(a) are $V_{CC} = 3$ V, $V_{BB} = 1.3$ V, and $\beta = 100$. Redesign the circuit such that $I_{BQ} = 5\,\mu$A and $V_{CEQ} = 1.5$ V. (b) Using the results of part (a), determine the variation in V_{CEQ} if β is in the range $75 \leq \beta \leq 125$.

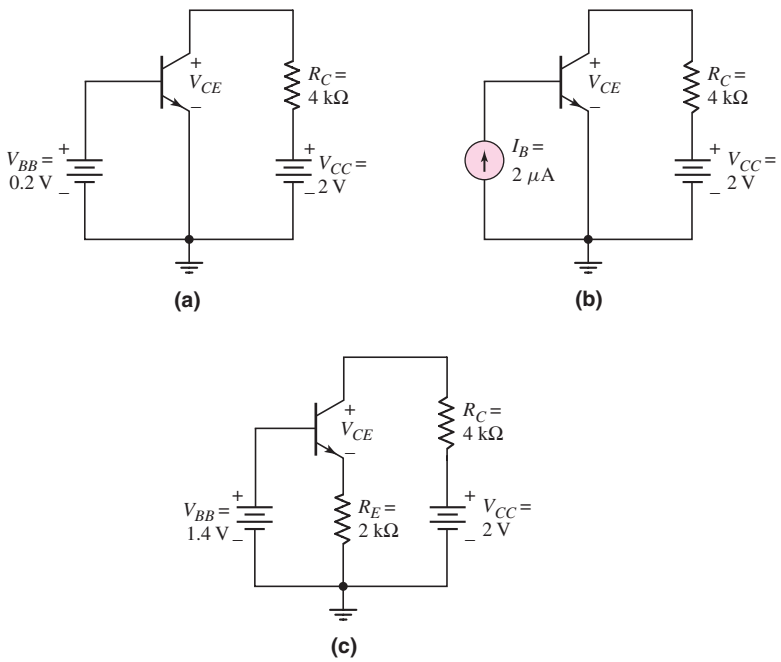

Figure P5.20

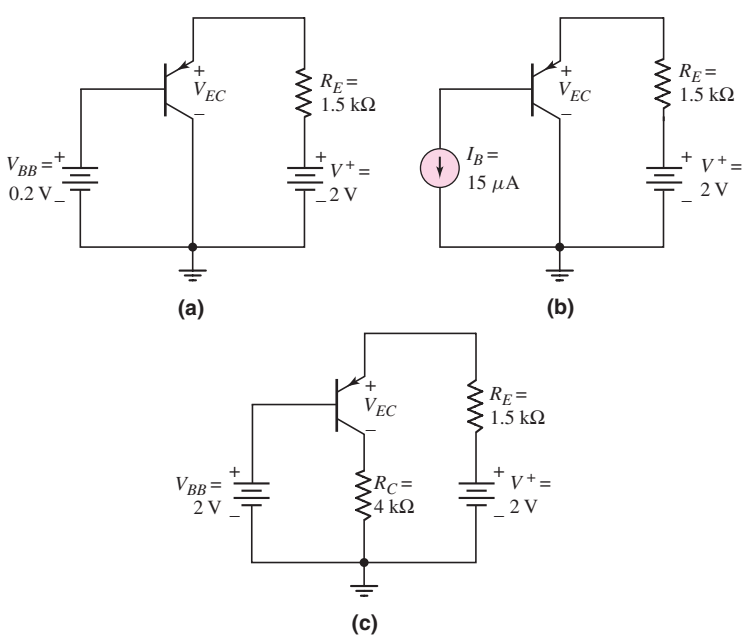

Figure P5.21

5.23 In the circuits shown in Figure P5.23, the values of measured parameters are shown. Determine β, α, and the other labeled currents and voltages. Sketch the dc load line and plot the Q-point.

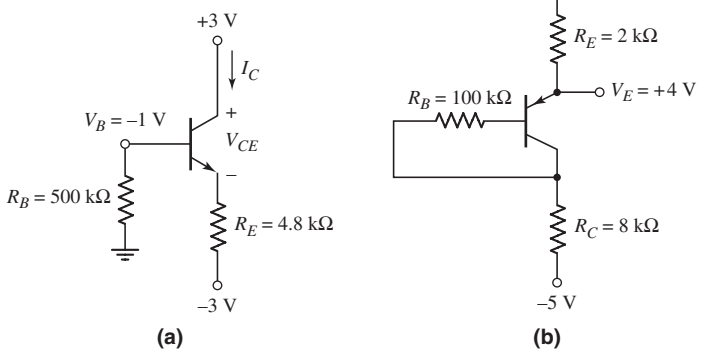

Figure P5.23

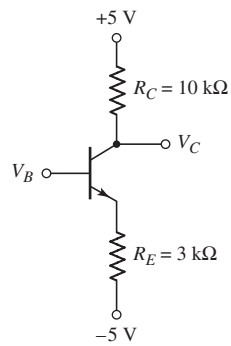

Figure P5.24

5.24 (a) For the circuit in Figure P5.24, determine V_B and I_E such that $V_B = V_C$. Assume $\beta = 90$. (b) What value of V_B results in $V_{CE} = 2$ V?

5.25 (a) The bias voltages in the circuit shown in Figure P5.25 are changed to $V^+ = 3.3$ V and $V^- = -3.3\,V$. The measured value of emitter voltage is $V_E = 0.85$ V. Determine I_E, I_C, β, α, and V_{EC}. (b) Using the results of part (a), determine V_E and V_{EC} if β increases by 10 percent.

5.26 The transistor shown in Figure P5.26 has $\beta = 120$. Determine I_C and V_{EC}. Plot the load line and the Q-point.

5.27 The transistor in the circuit shown in Figure P5.27 is biased with a constant current in the emitter. If $I_Q = 1$ mA, determine V_C and V_E. Assume $\beta = 50$.

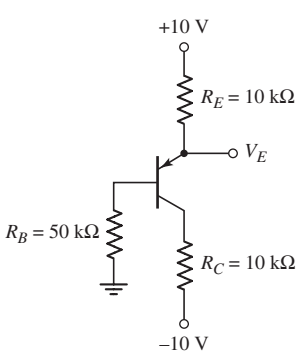

Figure P5.25

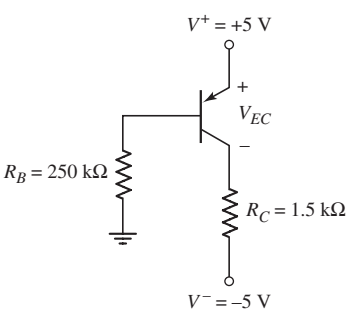

Figure P5.26

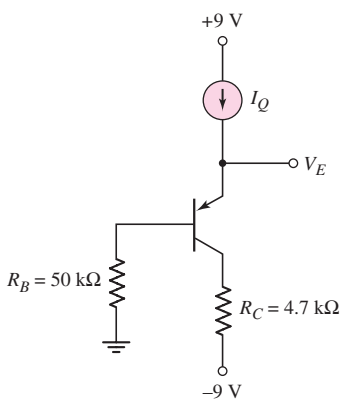

Figure P5.27

5.28 In the circuit in Figure P5.27, the constant current is $I = 0.5$ mA. If $\beta = 50$, determine the power dissipated in the transistor. Does the constant current source supply or dissipate power? What is the value?

5.29 For the circuit shown in Figure P5.29, if $\beta = 200$ for each transistor, determine: (a) I_{E1}, (b) I_{E2}, (c) V_{C1}, and (d) V_{C2}.

5.30 The circuit shown in Figure P5.30 is to be designed such that $I_{CQ} = 0.8$ mA and $V_{CEQ} = 2$ V for the case when (a) $R_E = 0$ and (b) $R_E = 1$ kΩ. Assume $\beta = 80$. (c) The transistor in Figure P5.30 is replaced with one with a value of $\beta = 120$. Using the results of parts (a) and (b), determine the Q-point values I_{CQ} and V_{CEQ}. Which design shows the smallest change in Q-point values?

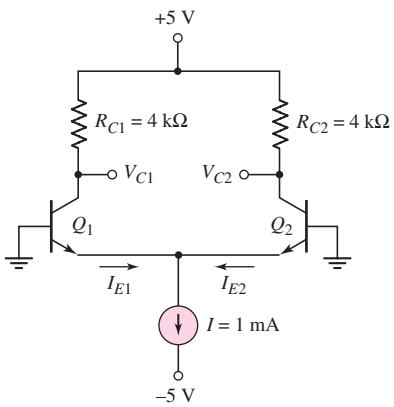

Figure P5.29

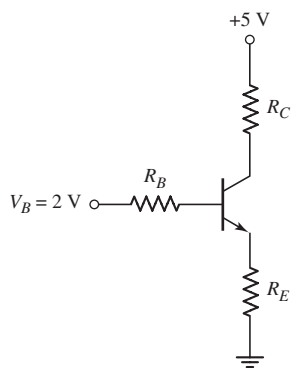

Figure P5.30

D5.31 (a) The bias voltage in the circuit in Figure P5.31 is changed to $V_{CC} = 9$ V. The transistor current gain is $\beta = 80$. Design the circuit such that $I_{CQ} = 0.25$ mA and $V_{CEQ} = 4.5$ V. (b) If the transistor is replaced by a new one with $\beta = 120$, find the new values of I_{CQ} and V_{CEQ}. (c) Sketch the load line and Q-point for both parts (a) and (b).

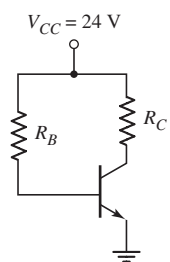

Figure P5.31

5.32 The current gain of the transistor in the circuit shown in Figure P5.32 is $\beta = 150$. Determine I_C, I_E, and V_C for (a) $V_B = 0.2$ V, (b) $V_B = 0.9$ V, (c) $V_B = 1.5$ V, and (d) $V_B = 2.2$ V.

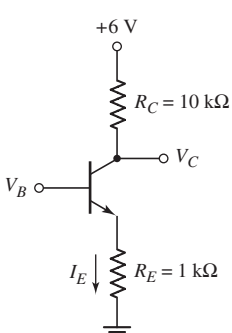

Figure P5.32

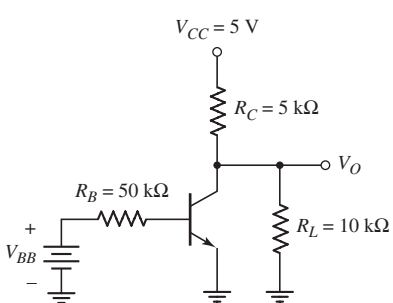

Figure P5.33

5.33 (a) The current gain of the transistor in Figure P5.33 is $\beta = 75$. Determine V_O for: (i) $V_{BB} = 0$, (ii) $V_{BB} = 1$ V, and (iii) $V_{BB} = 2$ V. (b) Verify the results of part (a) with a computer simulation.

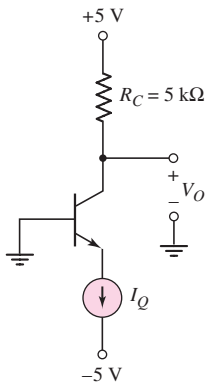

Figure P5.34

5.34 (a) The transistor shown in Figure P5.34 has $\beta = 100$. Determine V_O for (i) $I_Q = 0.1$ mA, (ii) $I_Q = 0.5$ mA, and (iii) $I_Q = 2$ mA. (b) Determine the percent change in V_O for the conditions in part (a) if the current gain increases to $\beta = 150$.

5.35 Assume $\beta = 120$ for the transistor in the circuit shown in Figure P5.34. Determine I_Q such that (a) $V_O = 4$ V, (b) $V_O = 2$ V, and (c) $V_O = 0$.

5.36 For the circuit shown in Figure P5.27, calculate and plot the power dissipated in the transistor for $I_Q = 0$, 0.5, 1.0, 1.5, 2.0, 2.5, and 3.0 mA. Assume $\beta = 50$.

5.37 Consider the common-base circuit shown in Figure P5.37. Assume the transistor alpha is $\alpha = 0.9920$. Determine I_E, I_C, and V_{BC}.

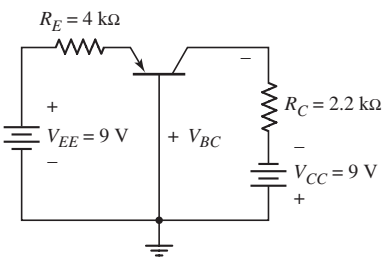

Figure P5.37

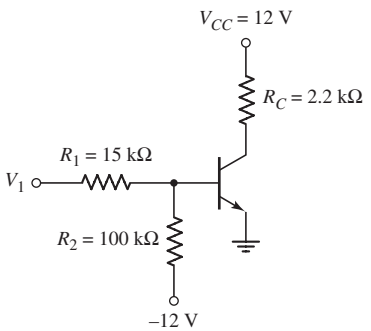

Figure P5.38

5.38 (a) For the transistor in Figure P5.38, $\beta = 80$. Determine V_1 such that $V_{CEQ} = 6$ V. (b) Determine the range in V_1 that produces $3 \leq V_{CEQ} \leq 9$ V.

5.39 Let $\beta = 25$ for the transistor in the circuit shown in Figure P5.39. Determine the range of V_1 such that $1.0 \leq V_{CE} \leq 4.5$ V. Sketch the load line and show the range of the Q-point values.

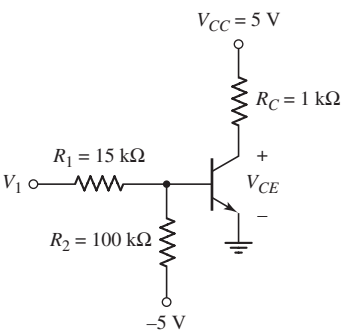

Figure P5.39

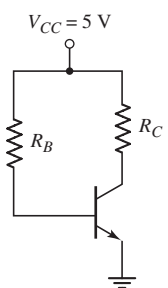

Figure P5.40

D5.40 (a) The circuit shown in Figure P5.40 is to be designed such that $I_{CQ} = 0.5$ mA and $V_{CEQ} = 2.5$ V. Assume $\beta = 120$. Sketch the load line and plot the Q-point. (b) Pick standard values of resistors that are close to the designed values. Assume that the standard resistor values vary by ± 10

percent. Plot the load lines and Q-point values for the maximum and minimum values of R_B and R_C values (four Q-point values).

5.41 The circuit shown in Figure P5.41 is sometimes used as a thermometer. Assume the transistors Q_1 and Q_2 in the circuit are identical. Writing the emitter currents in the form $I_E = I_{EO} \exp(V_{BE}/V_T)$, derive the expression for the output voltage V_O as a function of temperature T.

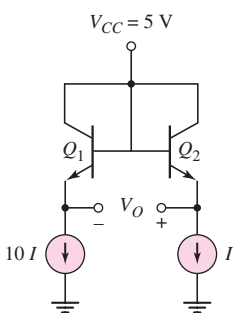

Figure P5.41

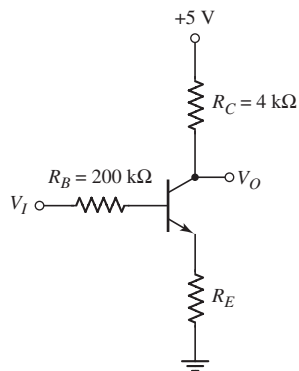

Figure P5.42

5.42 The transistor in Figure P5.42 has $\beta = 120$. (a) Determine V_I that produces $V_O = 4$ V for (i) $R_E = 0$ and (ii) $R_E = 1$ kΩ. (b) Repeat part (a) for $V_O = 2.5$ V. (c) Determine V_O for $V_I = 3.5$ V and for $R_E = 1$ kΩ.

5.43 The common-emitter current gain of the transistor in Figure P5.43 is $\beta = 80$. Plot the voltage transfer characteristics over the range $0 \leq V_I \leq 5$ V.

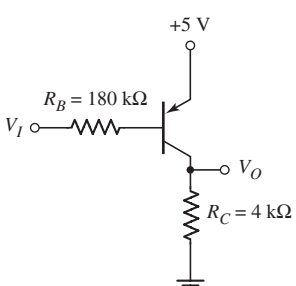

Figure P5.43

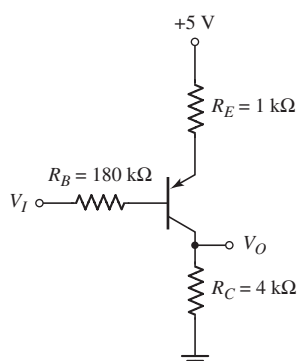

Figure P5.44

5.44 For the circuit shown in Figure P5.44, plot the voltage transfer characteristics over the range $0 \leq V_I \leq 5$ V. Assume $\beta = 100$.

Section 5.3 Basic Transistor Applications

5.45 The transistor in the circuit shown in Figure P5.45 has a current gain of $\beta = 40$. Determine R_B such that $V_O = 0.2$ V and $I_C/I_B = 20$ when $V_I = 5$ V.

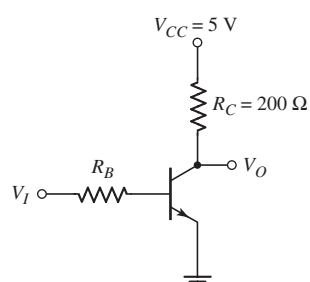

Figure P5.45

5.46 Consider the circuit in Figure P5.46. For the transistor, $\beta = 50$. Find I_B, I_C, I_E, and V_O for (a) $V_I = 0$, (b) $V_I = 2.5$ V, and (c) $V_I = 5$ V.

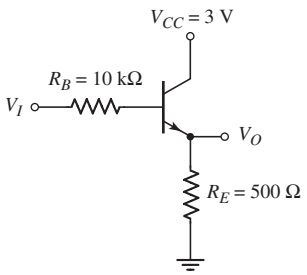

Figure P5.46

5.47 The current gain for the transistor in the circuit in Figure P5.47 is $\beta = 60$. Determine R_B such that $V_O = 8.8$ V when $V_I = 5$ V and $I_C/I_B = 25$.

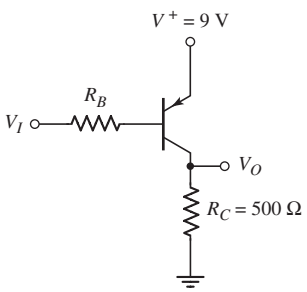

Figure P5.47

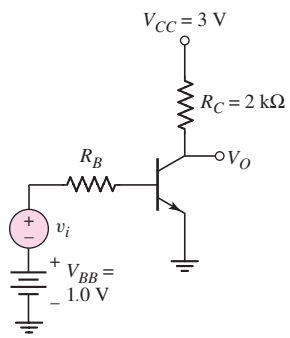

Figure P5.48

5.48 Consider the amplifier circuit shown in Figure P5.48. Assume a transistor current gain of $\beta = 120$. The voltage V_{BB} establishes the Q-point, and the voltage v_i is a time-varying signal that produces a variation in the base current, which in turn produces a variation in the collector current and hence a variation in the output voltage v_o. (a) Determine R_B such that $V_{CEQ} = 1.6$ V. (b) Determine the maximum variation in the output voltage such that the transistor does not enter cutoff or saturation. (c) What is the voltage gain $\Delta v_o/\Delta v_i$ of the amplifier? (d) What is the maximum variation in the voltage v_i such that the transistor does not enter cutoff or saturation?

Section 5.4 Bipolar Transistor Biasing

D5.49 For the transistor in the circuit shown in Figure P5.49, assume $\beta = 120$. Design the circuit such that $I_{CQ} = 0.15$ mA and $R_{TH} = 200$ kΩ. What is the value of V_{CEQ}?

5.50 Reconsider Figure P5.49. The transistor current gain is $\beta = 150$. The circuit parameters are changed to $R_{TH} = 120$ kΩ and $R_E = 1$ kΩ. Determine the values of R_C, R_1, and R_2 such that $V_{CEQ} = 1.5$ V and $I_{CQ} = 0.20$ mA.

5.51 The current gain of the transistor shown in the circuit of Figure P5.51 is $\beta = 100$. Determine V_B and I_{EQ}.

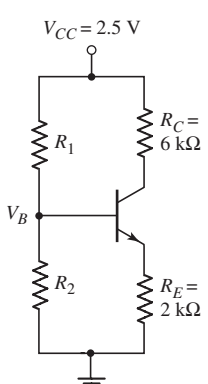

Figure P5.49

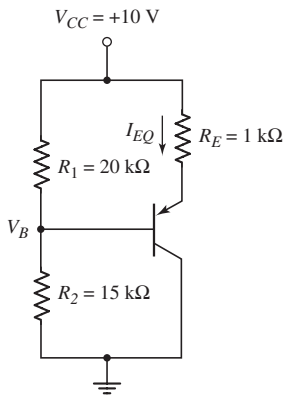

Figure P5.51

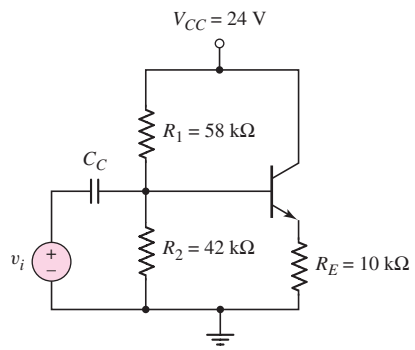

Figure P5.52

5.52 For the circuit shown in Figure P5.52, let $\beta = 125$. (a) Find I_{CQ} and V_{CEQ}. Sketch the load line and plot the Q-point. (b) If the resistors R_1 and R_2 vary by ± 5 percent, determine the range in I_{CQ} and V_{CEQ}. Plot the various Q-points on the load line.

5.53 Consider the circuit shown in Figure P5.53. (a) Determine I_{BQ}, I_{CQ}, and V_{CEQ} for $\beta = 80$. (b) What is the percent change in I_{CQ} and V_{CEQ} if β is changed to $\beta = 120$?

5.54 (a) Redesign the circuit shown in Figure P5.49 using $V_{CC} = 9$ V such that the voltage drop across R_C is $(\frac{1}{3})V_{CC}$ and the voltage drop across R_E is $(\frac{1}{3})V_{CC}$. Assume $\beta = 100$. The quiescent collector current is to be $I_{CQ} = 0.4$ mA, and the current through R_1 and R_2 should be approximately $0.2I_{CQ}$. (b) Replace each resistor in part (a) with the closest standard value (Appendix C). What is the value of I_{CQ} and what are the voltage drops across R_C and R_E?

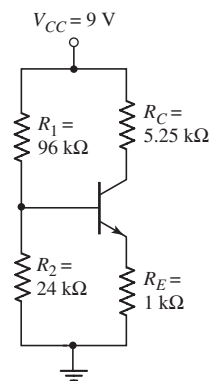

Figure P5.53

5.55 For the circuit shown in Figure P5.55, let $\beta = 100$. (a) Find R_{TH} and V_{TH} for the base circuit. (b) Determine I_{CQ} and V_{CEQ}. (c) Draw the load line and plot the Q-point. (d) If the resistors R_C and R_E vary by ± 5 percent, determine the range in I_{CQ} and V_{CEQ}. Draw the load lines corresponding to the maximum and minimum resistor values and plot the Q-points.

5.56 Consider the circuit shown in Figure P5.56. (a) Determine R_{TH}, V_{TH}, I_{BQ}, I_{CQ}, and V_{ECQ} for $\beta = 90$. (b) Determine the percent change in I_{CQ} and V_{ECQ} if β is changed to $\beta = 150$.

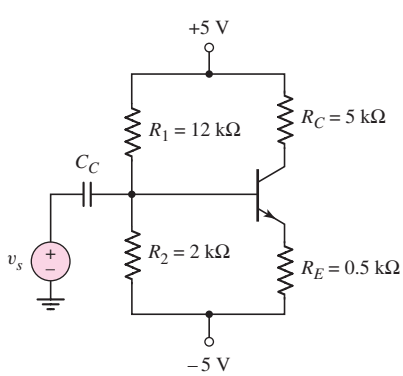

Figure P5.55

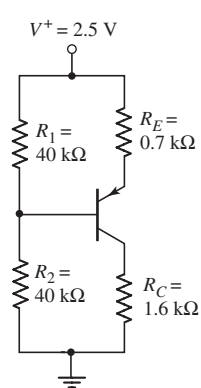

Figure P5.56

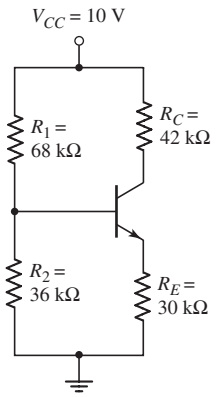

Figure P5.57

5.57 (a) Determine the Q-point values for the circuit in Figure P5.57. Assume $\beta = 50$. (b) Repeat part (a) if all resistor values are reduced by a factor of 3. (c) Sketch the load lines and plot the Q-point values for parts (a) and (b).

5.58 (a) Determine the Q-point values for the circuit in Figure P5.58. Assume $\beta = 50$. (b) Repeat part (a) if all resistor values are reduced by a factor of 3. (c) Sketch the load lines and plot the Q-point values for parts (a) and (b).

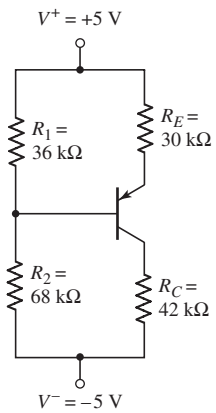

Figure P5.58

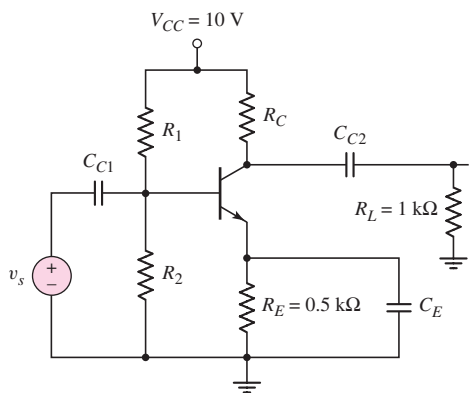

Figure P5.59

D5.59 (a) For the circuit shown in Figure P5.59, design a bias-stable circuit such that $I_{CQ} = 0.8$ mA and $V_{CEQ} = 5$ V. Let $\beta = 100$. (b) Using the results of part (a), determine the percentage change in I_{CQ} if β is in the range $75 \leq \beta \leq 150$. (c) Repeat parts (a) and (b) if $R_E = 1$ kΩ.

D5.60 Design a bias-stable circuit in the form of Figure P5.59 with $\beta = 120$ such that $I_{CQ} = 0.8$ mA, $V_{CEQ} = 5$ V, and the voltage across R_E is approximately 0.7 V.

D5.61 Using the circuit in Figure P5.61, design a bias-stable amplifier such that the Q-point is in the center of the load line. Let $\beta = 125$. Determine I_{CQ}, V_{CEQ}, R_1, and R_2.

D5.62 For the circuit shown in Figure P5.61, the bias voltages are changed to $V^+ = 3$ V and $V^- = -3$ V. (a) Design a bias-stable circuit for $\beta = 120$

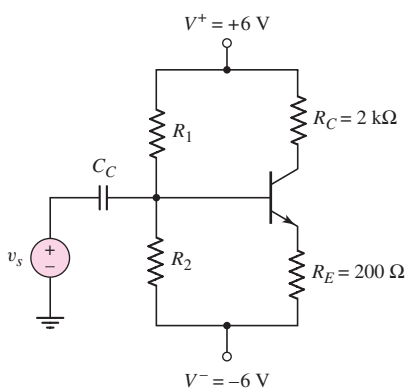

Figure P5.61

such that $V_{CEQ} = 2.8$ V. Determine I_{CQ}, R_1, and R_2. (b) If the resistors R_1 and R_2 vary by ± 5 percent, determine the range in I_{CQ} and V_{CEQ}. Plot the various Q-points on the load line.

5.63 (a) A bias-stable circuit with the configuration shown in Figure P5.61 is to be designed such that $I_{CQ} = (3 \pm 0.1)$ mA and $V_{CEQ} \cong 5$ V using a transistor with $75 \leq \beta \leq 150$. (b) Sketch the load line and plot the range of Q-point values for part (a).

D5.64 (a) For the circuit shown in Figure P5.64, assume that the transistor current gain is $\beta = 90$ and that the circuit parameter is $R_{TH} = 2.4\,\text{k}\Omega$. Design the circuit such that $V_{ECQ} = 1.5$ V. Find I_{BQ}, I_{CQ}, R_1, and R_2. (b) Determine the values of I_{BQ}, I_{CQ}, and V_{ECQ} if the current gain is changed to $\beta = 130$.

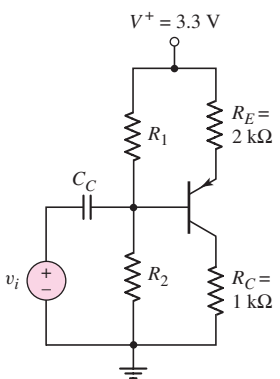

Figure P5.64

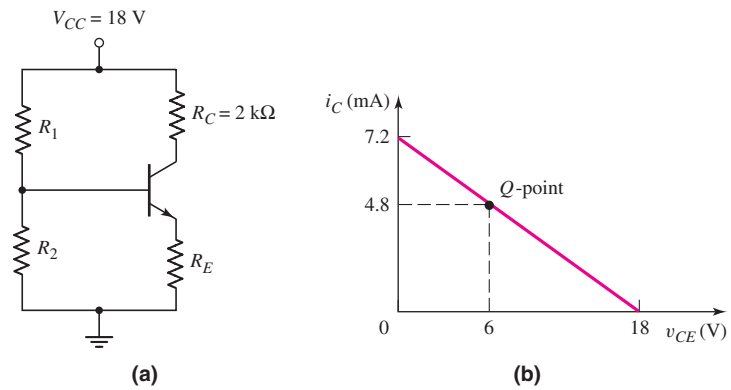

Figure P5.65

5.65 The dc load line and Q-point of the circuit in Figure P5.65(a) are shown in Figure P5.65(b). For the transistor, $\beta = 120$. Find R_E, R_1, and R_2 such that the circuit is bias stable.

D5.66 The range of β for the transistor in the circuit in Figure P5.66 is $80 \leq \beta \leq 120$. Design a bias-stable circuit such that the nominal Q-point values are $I_{CQ} = 0.2$ mA and $V_{CEQ} = 1.6$ V. The value of I_{CQ} must fall in the range $0.19 \leq I_{CQ} \leq 0.21$ mA. Determine R_E, R_1, and R_2.

D5.67 The nominal Q-point of the circuit in Figure P5.67 is $I_{CQ} = 1$ mA and $V_{CEQ} = 5$ V, for $\beta = 60$. The current gain of the transistor is in the range

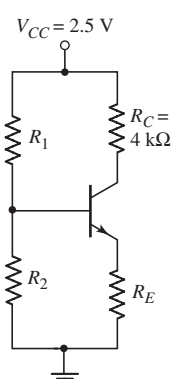

Figure P5.66

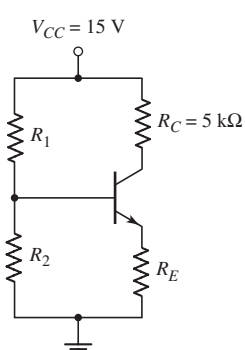

Figure P5.67

$45 \le \beta \le 75$. Design a bias-stable circuit such that I_{CQ} does not vary by more than 5 percent from its nominal value.

D5.68 (a) For the circuit in Figure P5.67, the value of V_{CC} is changed to 3 V. Let $R_C = 5R_E$ and $\beta = 120$. Redesign a bias-stable circuit such that $I_{CQ} = 100\ \mu$A and $V_{CEQ} = 1.4$ V. (b) Using the results of part (a), determine the dc power dissipation in the circuit.

D5.69 For the circuit in Figure P5.69, let $\beta = 100$ and $R_E = 3$ kΩ. Design a bias-stable circuit such that $V_E = 0$.

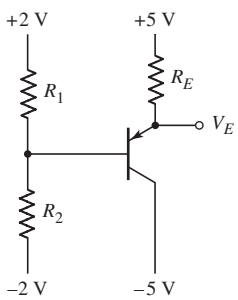

Figure P5.69

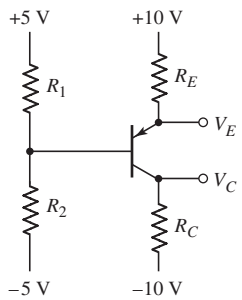

Figure P5.70

5.70 For the circuit in Figure P5.70, let $R_C = 2.2$ kΩ, $R_E = 2$ kΩ, $R_1 = 10$ kΩ, $R_2 = 20$ kΩ, and $\beta = 60$. (a) Find R_{TH} and V_{TH} for the base circuit. (b) Determine I_{BQ}, I_{CQ}, V_E, and V_C.

D5.71 Design the circuit in Figure P5.70 to be bias stable and to provide nominal Q-point values of $I_{CQ} = 0.5$ mA and $V_{ECQ} = 8$ V. Let $\beta = 60$. The maximum current in R_1 and R_2 is to be limited to 40 μA.

D5.72 Consider the circuit shown in Figure P5.72. (a) The nominal transistor current gain is $\beta = 80$. Design a bias-stable circuit such that $I_{CQ} = 0.15$ mA and $V_{ECQ} = 2.7$ V. (b) Using the results of part (a), determine the percent change in I_{CQ} and V_{ECQ} if the transistor current gain is in the range $60 \le \beta \le 100$.

5.73 For the circuit in Figure P5.73, let $\beta = 100$. (a) Find V_{TH} and R_{TH} for the base circuit. (b) Determine I_{CQ} and V_{CEQ}.

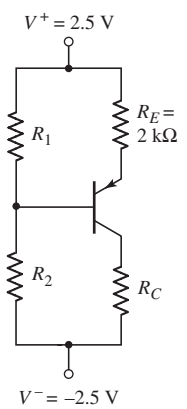

Figure P5.72

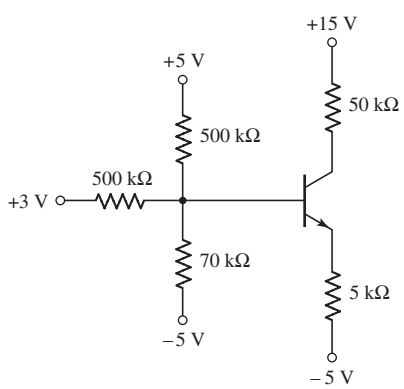

Figure P5.73

D5.74 Design a bias-stable four-resistor bias network for an npn transistor such that $I_{CQ} = 0.8$ mA, $V_{CEQ} = 4$ V, and $V_E = 1.5$ V. The circuit and transistor parameters are $V_{CC} = 10$ V and $\beta = 120$, respectively.

D5.75 (a) Design a four-resistor bias network with the configuration shown in Figure P5.61 to yield Q-point values of $I_{CQ} = 50\ \mu$A and $V_{CEQ} = 5$ V. The bias voltages are $V^+ = +5$ V and $V^- = -5$ V. Assume a transistor with $\beta = 80$ is available. The voltage across the emitter resistor should be approximately 1 V. (b) The transistor in part (a) is replaced by one with $\beta = 120$. Determine the resulting Q-point.

D5.76 (a) Design a four-resistor bias network with the configuration shown in Figure P5.61 to yield Q-point values of $I_{CQ} = 0.50$ mA and $V_{CEQ} = 2.5$ V. The bias voltages are $V^+ = 3$ V and $V^- = -3$ V. The transistor current gain is $\beta = 120$. The voltage across the emitter resistor should be approximately 0.7 V. (b) Replace the designed resistors in part (a) with standard resistors with values closest to the designed values. Determine the resulting Q-point.

D5.77 (a) A four-resistor bias network is to be designed with the configuration shown in Figure P5.77. The Q-point values are to be $I_{CQ} = 100\,\mu$A and $V_{ECQ} = 3$ V. The bias voltages are $V^+ = 3$ V and $V^- = -3$ V. A transistor with $\beta = 110$ is available. The voltage across the emitter resistor should be approximately 0.7 V. (b) The transistor in part (a) is replaced with one with $\beta = 150$. What is the resulting Q-point?

D5.78 (a) Design a four-resistor bias network with the configuration shown in Figure P5.77 such that the Q-point values are $I_{CQ} = 1.2$ mA and $V_{ECQ} = 6$ V. The bias voltages are $V^+ = 9$ V and $V^- = -9$ V. A transistor with $\beta = 75$ is available. The voltage across the emitter resistor should be approximately 1.5 V. (b) Replace the designed resistors in part (a) with standard resistors with values closest to the designed values. Determine the resulting Q-point.

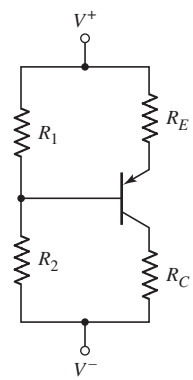

Figure P5.77

Section 5.5 Multistage Circuits

5.79 For each transistor in the circuit in Figure P5.79, $\beta = 120$ and the B–E turn-on voltage is 0.7 V. Determine the quiescent base, collector, and emitter currents in Q_1 and Q_2. Also determine V_{CEQ1} and V_{CEQ2}.

5.80 The parameters for each transistor in the circuit in Figure P5.80 are $\beta = 80$ and $V_{BE}(\text{on}) = 0.7$ V. Determine the quiescent values of base, collector, and emitter currents in Q_1 and Q_2.

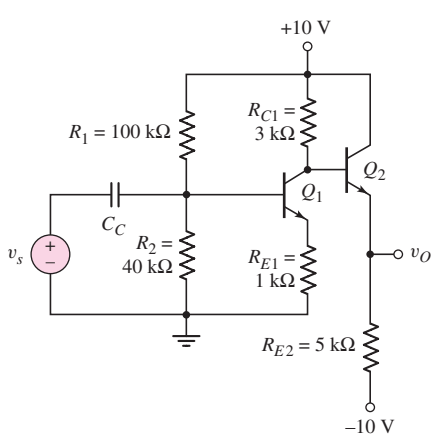

Figure P5.79

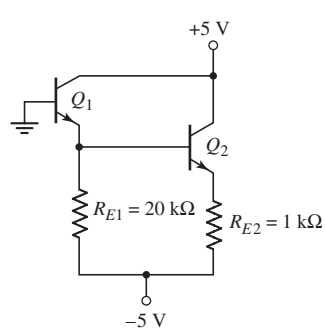

Figure P5.80

D5.81 The bias voltage in the circuit shown in Figure 5.63 is changed to $V^+ = 5$ V. Design the circuit to meet the following specifications: $V_{CE1} = V_{CE2} = 1.2$ V, $V_{RE} = 0.5$ V, $I_{C1} \cong I_{C2} \cong 0.2$ mA, and $I_{R1} \cong I_{R2} \cong I_{R3} \cong 20\,\mu$A.

5.82 Consider the circuit shown in Figure P5.82. The current gain for the npn transistor is $\beta_n = 120$ and for the pnp transistor is $\beta_p = 80$. Determine I_{B1}, I_{C1}, I_{B2}, I_{C2}, V_{CE1}, and V_{EC2}.

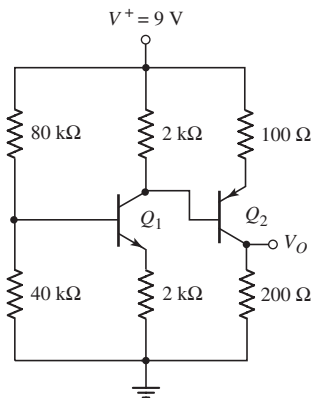

Figure P5.82

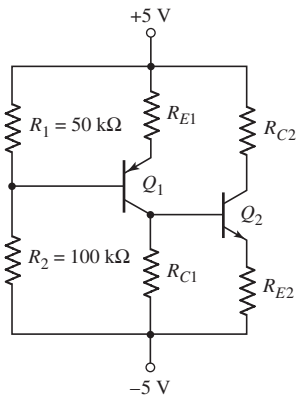

Figure P5.83

5.83 (a) For the transistors in the circuit shown in Figure P5.83, the parameters are: $\beta = 100$ and $V_{BE}(\text{on}) = V_{EB}(\text{on}) = 0.7$ V. Determine R_{C1}, R_{E1}, R_{C2}, and R_{E2} such that $I_{C1} = I_{C2} = 0.8$ mA, $V_{ECQ1} = 3.5$ V, and $V_{CEQ2} = 4.0$ V. (b) Correlate the results of part (a) with a computer simulation.

COMPUTER SIMULATION PROBLEMS

5.84 Using a computer simulation, plot V_{CE} versus V_1 over the range $0 \leq V_I \leq 8$ V for the circuit in Figure 5.24(a). At what voltage does the transistor turn on and at what voltage does the transistor go into saturation?

5.85 Using a computer simulation, verify the results of Example 5.7.

5.86 Consider the circuit and parameters in Example 5.15. Using a computer simulation, determine the change in Q-point values if all resistors vary by ± 5 percent.

5.87 Using a computer simulation, verify the results of Example 5.19.

DESIGN PROBLEMS

[Note: Each design should be correlated with a computer simulation.]

*D5.88 Consider a common-emitter circuit with the configuration shown in Figure 5.54(a). Assume a bias voltage of $V_{CC} = 3.3$ V and assume the transistor current gain is in the range $100 \leq \beta \leq 160$. Design the circuit such that the nominal Q-point is in the center of the load line and that the Q-point values

do not vary by more than ±3 percent. Determine appropriate values for R_1 and R_2.

*D5.89 The emitter-follower circuit shown in Figure P5.89 is biased at $V^+ = 2.5$ V and $V^- = -2.5$ V. Design a bias-stable circuit such that the nominal Q-point values are $I_{CQ} \cong 5$ mA and $V_{CEQ} \cong 2.5$ V. The transistor current gain values are in the range $100 \leq \beta \leq 160$. Select standard 5 percent tolerance resistance values in the final design. What is the range in Q-point values?

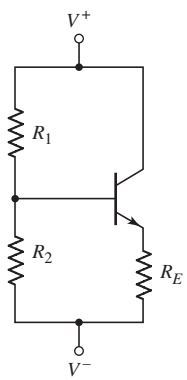

Figure P5.89

*D5.90 The bias voltages for the circuit in Figure 5.57(a) are $V^+ = 3.3$ V and $V^- = -3.3$ V. The transistor current gain is $\beta = 100$. Design a bias-stable circuit such that $I_{CQ} \cong 120\,\mu$A, $V_{RE} \cong 0.7$ V, and $V_{ECQ} \cong 3$ V. Use standard resistor values in the final design.

*D5.91 The multitransistor circuit in Figure 5.61 is to be redesigned. The bias voltages are to be ±3.3 V and the nominal transistor current gains are $\beta = 120$. Design a bias-stable circuit such that $I_{CQ1} = 100\,\mu$A, $I_{CQ2} = 200\,\mu$A, and $V_{CEQ1} \cong V_{ECQ2} \cong 3$ V.