APPENDIX

A

IEEE STANDARD SYMBOLS

The Institute of Electrical and Electronic Engineers (IEEE) has developed a standard set of logic symbols to represent digital electronics circuits. The IEEE standard graphic symbols for logic functions are compatible with standard 617 of International Electrotechnical Commission. Fundamental circuit diagram symbols corresponding to SSI, and MSI ICs describe the logic function of ICs in a consistent and logical manner. But the detail logic function representation of VLSI ICs is impractical, so that symbolic methodology can be used to indicate the functions of major components. Professional digital electronics circuits designer should be familiar with IEEE standard symbols as they are most commonly used in the manufacturer's data sheets during design of digital systems. In this section, IEEE standard symbols have been described to familiar with logic symbols which are commonly used in digital system design.

A.1 INTERNAL LOGIC STATE AND EXTERNAL LOGIC STATE

The IEEE standard can support the notion of bubble to bubble logic design. The internal logic state means that the logic state is existing inside the rectangular symbol outline at the input and output. The external logic state means that the logic state is existing at external input or output. The inversion circle is used at the inputs and outputs of conventional symbols. Figure A.1 shows the Internal and external logic states.

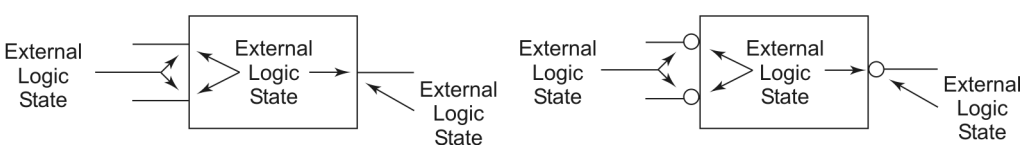


Fig. A.1 *Internal and external logic states*

A.2 LOGIC GATES AND GENERAL QUALIFYING SYMBOLS

The simplest Boolean logic gates have functional symbols that are simply rectangles labelled with appropriate general symbols. Figure A.2 shows the symbols of logic gates. The general symbols for simple AND, OR and EX-OR gates and buffers indicate the number of inputs that must be active in order to activate the output. The functional system includes an alternative to the inversion circle or the polarity indicator. Some general qualifying symbols for digital circuit representation are illustrated in Fig. A.3.

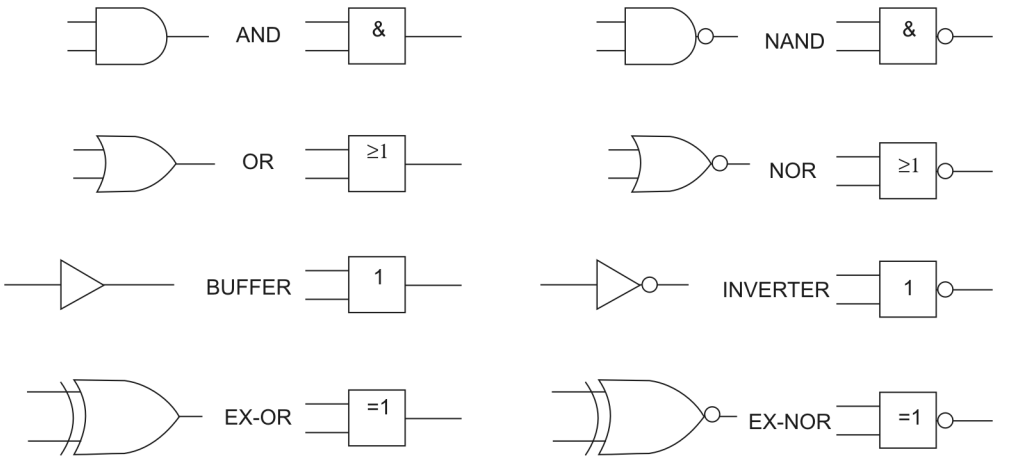


Fig. A.2 *Functional logic symbols of AND, NAND, OR, NOR, Buffer, Inverter, EX-OR and EX-NOR gates*

Symbol	**Function**
&	AND gate
≥1	OR gate
= 1	Exclusive OR
=	Logic identity
2k	An even number of inputs must be active
2k+1	An odd number of inputs must be active
1	The input must be active
⊳ or ⊲	A buffer or element with more than usual output capability. Symbol is oriented in the direction of signal flow
⨍	Schmitt trigger, element with hysteresis
X/Y	Code converter
MUX	Multiplexer
DMUX	Demultiplexer
Σ	Adder
P-Q	Subtracter
CPG	Look-ahead carry generator
π	Multiplier
COMP	Magnitude comparator
ALU	arithmetic logic unit
⎍	Retriggerable monostable

1	Nonretriggerable monostable
SRGm	Shift register, m=number of bits
CTRm	Counter, m=number of bits, cycle length 2^m
CTR DIVm	Counter with cycle length m
RCTRm	Asynchronous ripple counter, cycle length 2^m
	Logic negation at input, External 0 produces internal 1
	Logic negation at output, internal 1 produces External 0
	Active low input equivalent to in positive logic
	Active low output equivalent to in positive logic
	Active low input in the case of right to left signal flow
	Active low output in the case of right to left signal flow
	Signal flow from right to left. If not otherwise indicated, signal flow is from left to right
	Bidirectional signal flow
	Dynamic inputs active on indicated transition **Positive Logic** **Positive Logic** **Polarity Indication** 1→0 0→1 H→L 0→1 1→0 L→H
	Nonlogic connection A label inside the symbol usually defines the nature of this pin
	Input of analog signals
	Input for digital signals

Fig. A.3 *General qualifying symbols*

A.3 DECODERS

The IEEE standard for logic symbols allows a decoder's logic function to be displayed as part of the symbol. The symbols are used as basic concept of internal qualifying symbols, general qualifying symbols, internal values, input weights, output values, and enable input. Individual input and output signals may be labelled with symbols inside the logic-symbol outline to describe the signal characteristics.

The top of a logic symbol may contain an alphanumeric label to denote the general function performed by the device. The decoders and encoders use the standard symbol *X*/*Y*, where *X* is the input code and *Y* is the output code. Each input combination of coder produces an internal value. The internal values of a 3 to 8 decoder are 0 to 7. Each output may have a qualifying label listing the internal values that cause the output to be asserted. In a decoder , each output is asserted for just one internal value. An enable input has the qualifying label *EN* which control the function

of the device. While *EN* is asserted, output is active low available at output terminals. When *EN* is not asserted, an enable input imposes the external high –impedance state on the three-state outputs. The IC 74×138, IC 74×139 and IC 74×328 have active –low outputs.

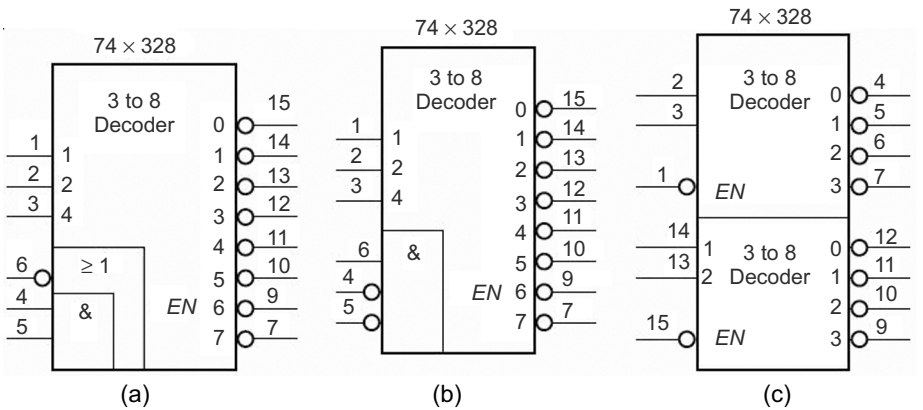


Fig. A.4 *IEEE standard symbol for decoder (a) IC 74x328 (b) IC 74 ×138 (c) IC 74 ×139*

A.4 TRI-STATE BUFFER REGISTER

The IEEE standard Tri-state buffer symbols are illustrated in Fig. A.5. The downward pointing triangle denotes a three state output and an enable input is labelled by *EN*. When *EN*=1, the device is enabled for output and the desired output corresponding to inputs are obtained at output terminals. If the device is disabled, output will be high impedance state (*Z*). The IEEE standard symbols are used for MSI three state buffers. The common control block concept is given in Fig A.6 in which a common block is used with an array of related elements. The inputs to the common control block can control all the elements of the array.

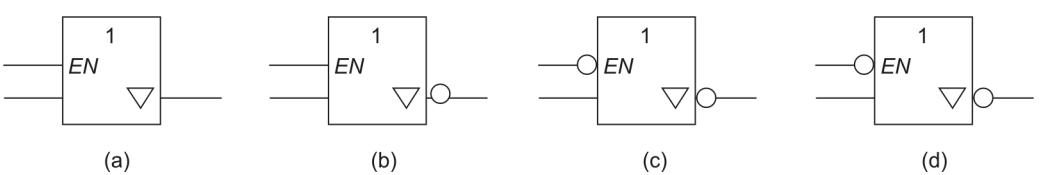


Fig. A.5 *IEEE standard Tri-state buffer symbols (a) non inverting active-high enable (b) inverting active-high enable (c) non-inverting active-low enable (d) inverting active-low enable*

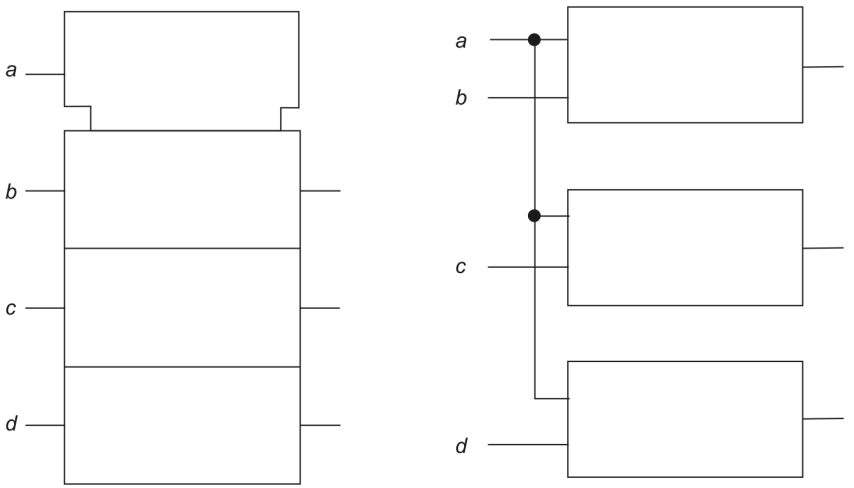


Fig. A.6 *Common control block in IEEE standard symbols*

The IEEE standard symbols for the IC 74 × 541 and IC 74 × 245 are shown in Fig. A.7. In this figure, the enable and direction inputs can be applied to all elements of the device. The common control block controls all identical elements. The other common features of IC 74 × 541 and IC 74 × 245 are hysteresis symbol, right – pointing or left-pointing triangle, arrows and identical elements. Hysteresis symbol represents that inputs have hysteresis. The right-pointing or left-pointing triangle is used to represent amplification signals. In case of three-state buffers, output has more fan-out capacity. The arrows represent the direction of signal flow when it is not strictly left or right. One or two identical elements in the array must be drawn in detail as shown in Fig. A.7. The other elements must be identical to the first element.

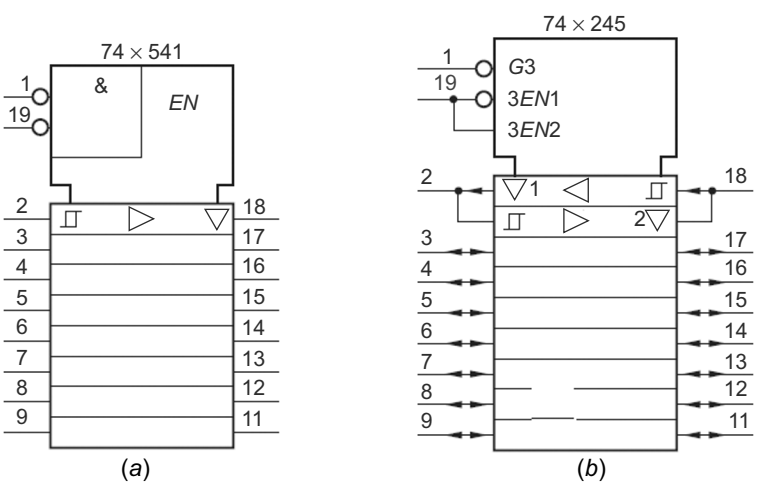


Fig. A.7 *IEEE standard symbols for Tri-state buffer (a) IC 74 × 541 and (b) IC 74 × 245*

A.5 MULTIPLEXERS AND DEMULTIPLEXERS

The IEEE standard symbols for multiplexers and demultiplexers are shown in Fig. A.8 and Fig. A.9 respectively. The general symbol MUX identifies multiplexer. The bit-grouping symbol is represented by a bracket which indicates that a grouped inputs generate an internal value that is a weighted sum. The weight are given by the qualifying labels on the individual inputs and the weights are power of two. In the standard symbol of IC 74×151 multiplexer, the notation $G\frac{0}{7}$ represents AND dependency with 0 to 7 signals. Any one input channel will be selected depending on the weighted input signals and there are two outputs: one is equal to input and other is complement of input.

In IC 74×153, the $G\frac{0}{3}$ represents the bit grouping for selected inputs and the common control block for two different block. Both half of the multiplexer is identical in function to the top as its qualifying labels are not repeated. And each half has an independent EN input.

The IC 74×157 has no bit-grouping, but has a common enable input EN and control dependency signal *G*1. This IC has four sections which are controlled by *G*1. When *G*1=1, pin 3 is selected. If *G*1=0, pin 2 is selected.

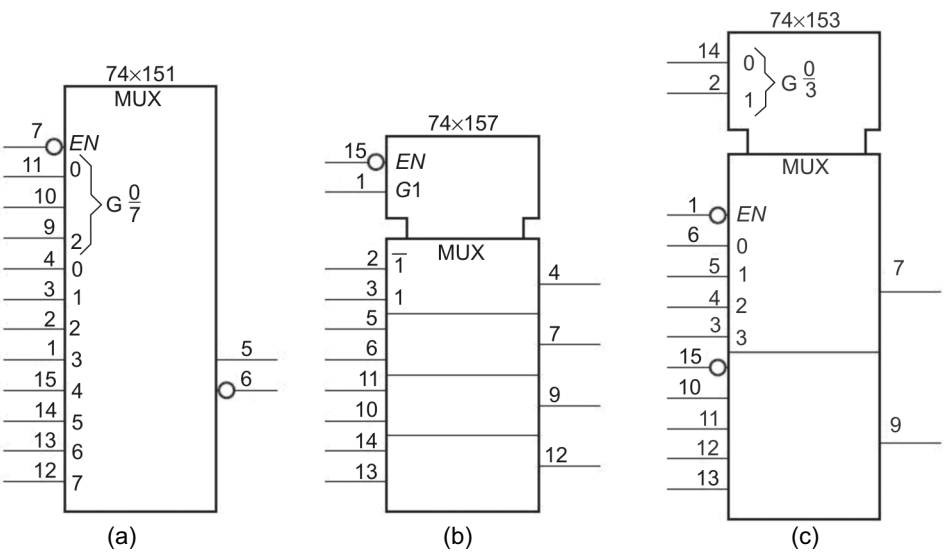


Fig. A.8 *IEEE standard symbols for multiplexers (a) IC 74 ×151, (b) IC 74 ×157 and (c) IC 74 ×153*

The IEEE standard demultiplexer symbols for the MSI demultiplexer ICs are illustrated in Fig. A.9. The notation $G\frac{0}{7}$ represents AND dependency with 0 to 7 signals. Any one output channel will be selected depending on the weighted input signals and there are three inputs. The IC 74×139 consists of two independent demultiplexers. Each demultiplexer has enabled input signal and bit grouping $G\frac{0}{3}$. It is depicted in standard symbol of IC 74×155, there is a common control block which is used to control two different demultiplexer sections. The input labelled 4 has an AND dependency with *G*4 so that the selected output is asserted when only both inputs are asserted.

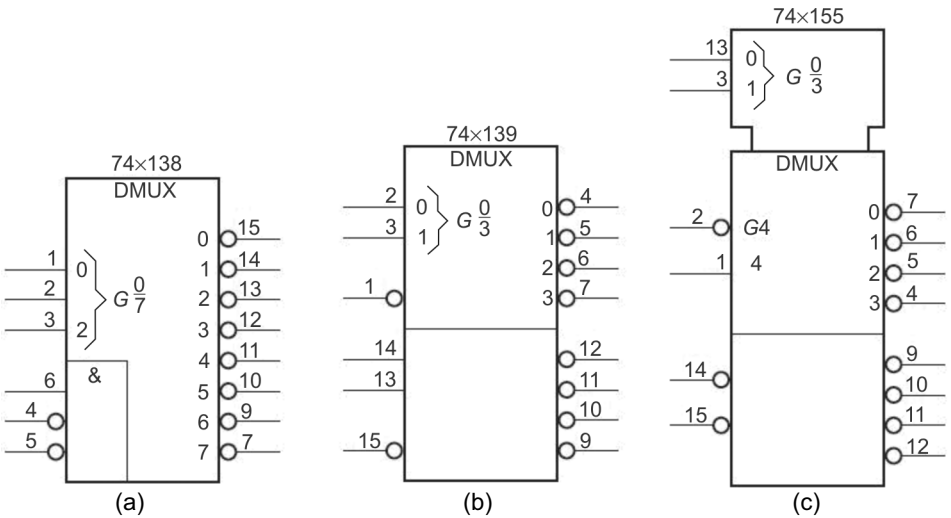


Fig. A.9 *IEEE standard symbols for demultiplexers (a) IC 74 × 138, (b) IC 74 ×139 and (c) IC 74×155*

A.6 ADDERS AND COMPARATORS

IEEE standard symbols for MSI adders and comparators are shown in Fig.A.10. The general qualifying symbol is used to identify an adder or addition function. Figure A.10(a) is the symbol of 4 bit adder IC 74 ×283. The numbers on the addend inputs and sum output indicate the weight of each pin as power of 2. Figure A.10(b) shows the symbol of 4 bit comparator IC 74 × 85. Just like select inputs of multiplexers, the data inputs have qualifying labels which indicate the weights in power of 2.

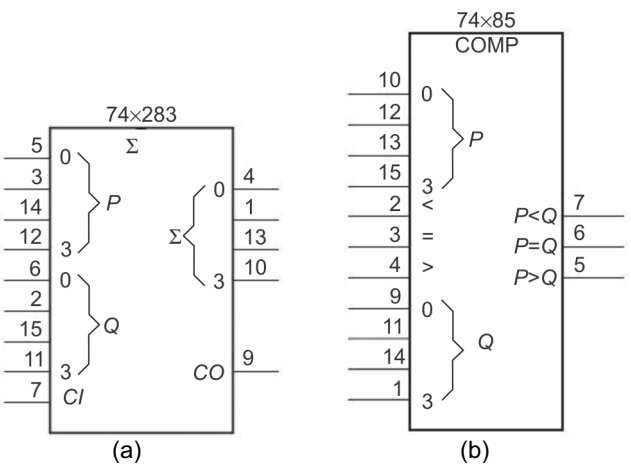


Fig. A.10 *IEEE standard symbols for (a) adders IC 74×283 (b) comparators IC 74×85*

A.7 LATCHES AND FLIP-FLOPS

Figure A.11 shows the IEEE standard symbols for latches and flip-flops. There are some differences between latches and flip-flops. The major difference is that asynchronous preset and clear inputs are available on the left of flip-flops IEEE standard symbols only. The names of these inputs are S (set) and R (reset). The clock input is named as *Ci* , where *i* is an integer. The other inputs are labelled as iD for inputs. Figure A.11(a) represents the IC 74×375 which is a latch. IC 74×74 has two identical elements and it consists of two *D* flip-flops. The *D* flip-flop has *S* (set) and R (reset) and Clock input *C*1. The *D* flip-flops input is represented by 1*D* and output is available in normal and complement form. The IEEE standard symbol of *JK* flip-flop IC 74×112 is illustrated in Fig. A.11(c) which operates on each negative edge triggered clock pulse.

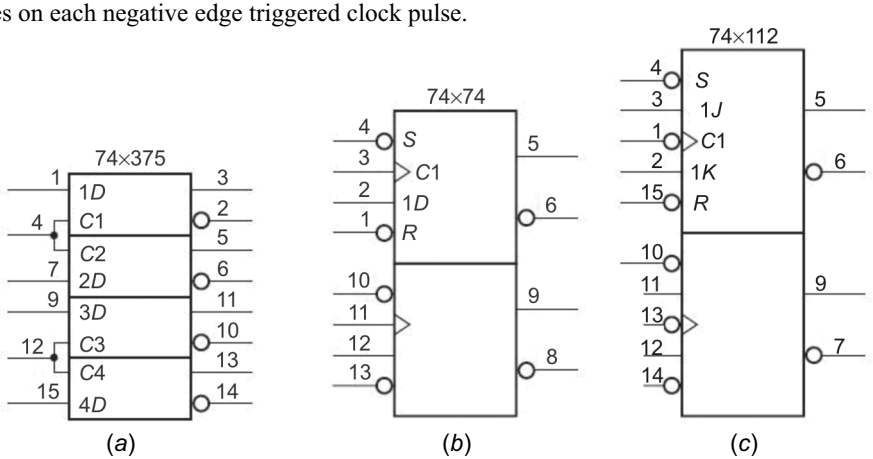
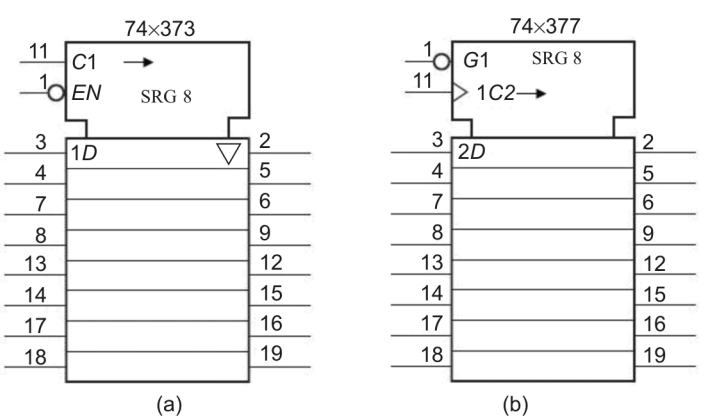


Fig. A.11 *IEEE Standard symbols for (a) D latch IC 74 × 375 (b) D flip-flop IC 74 × 74 (c) JK flip-flop IC 74 × 112*

A.8 SHIFT REGISTER

IEEE Standard symbols for 8 bit shift register with parallel outputs from each bit as shown in Fig.A.12. The upper section of the diagram is control block and the lower section consists of eight flip-flops that make up eight stages of shift register. The qualifying symbol → indicates that the data shifts one stage further away from the control block every time after the rising edge of clock input pulse. The enabling control of the flip-flops by the clock is indicated by control dependency *C*1 and an enable signal *EN*. The downward-pointing triangles indicate tri-state outputs. In IC 74×377, the input *G*1 is used as an enable for inputs bearing the label 1 and the clock input is IC2. The clock input controls all of the inputs bearing the label 2 that is data input lines 2*D*. The qualifying symbol SRGn represents an n-bit shift register. When the device is asserted , an input labelled with a → causes the device shift its data one position left to right and an input labelled with a ← cause a shift in the opposite direction.



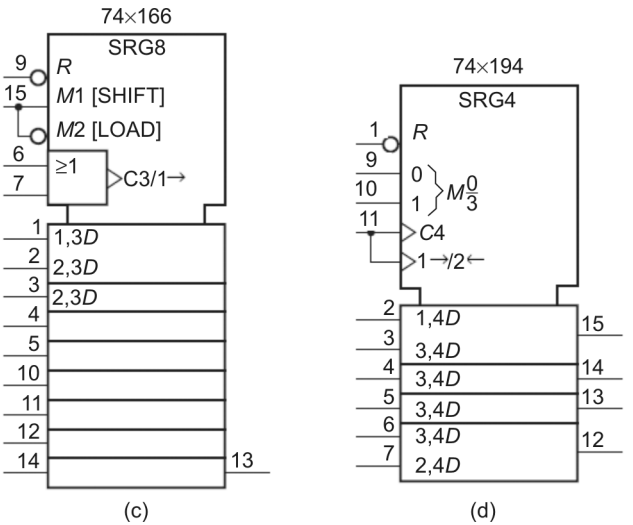


Fig. A.12 *IEEE standard symbols for registers (a) IC 74 × 373 (b) IC 74 × 377 (c) IC 74 × 166 and (d) IC 74 × 194*

A.9 COUNTERS

IEEE standard symbols of counters are shown in Fig. A.13. The general qualifying symbol CTR represents counter and DIV16 indicates that the counter is a divide-by-16 counter and labels [1] to [8] indicate the arithmetic weight of each counter bit. The common control block is used to explain the counter functions and it has the following control signals content input, content output, mode dependency. When the content input signal bearing the label *CT*=*m* is asserted, the value '*m*' is loaded into the device. In the counter symbols, *CT* represents count but in general it indicates content. In content output, an output bearing the label *CT*=*m* is asserted when the content of the device is *m*. In IC 74 × 161, the output 3*CT*=15 is asserted when the counter is in state 15.

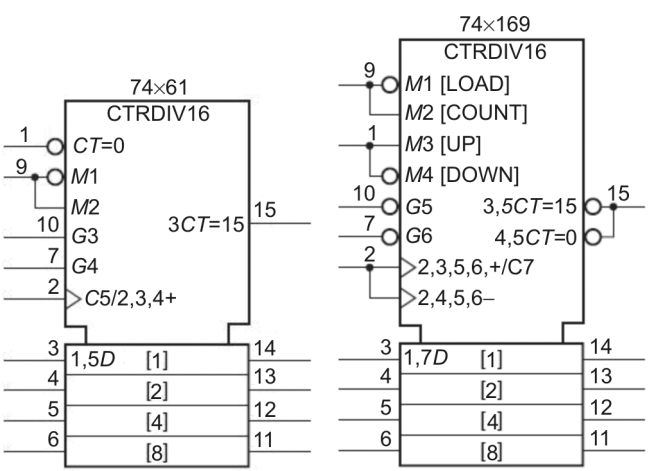


Fig. A.13 *IEEE standard symbol for counters (a) 74 ×161 and (b) 74 ×169*

The mode dependency of counter is indicated by *Mi* which is used as enable function. When *Mi* signal is asserted, counter perform normal operations. But if *Mi* signal is not asserted, the affected signals have no effect on the device's function and ignored.

When the device is asserted, an input labelled with *a* + causes the device to count up once. While input labelled with *a* – causes the device to count down once. The counter counts up on the rising edge of the signal if M_2, G_3 and G_4 are asserted. In IC 74×169, if M_2, M_3, G_5 and G_6 are asserted, counter operates in up counting mode. If M_2, M_4, G_5 and G_6 are asserted, counter operates in down counting mode.

A.10 ADDRESS DEPENDENCY

In programmable logic devices, such as ROM and RAM, any one of the binary array elements (binary words) can be selected by the use of a set of address inputs. This is indicated by a functional logic symbol A, address dependency. The method of Address Dependency is that the address lines allow the element that is selected by the address to function fully and to react the affected inputs. IEEE standard symbols of TMS27128 16KB EPROM and TMS47256 32KB ROM are shown in Fig. A.14. All outputs are tri-stated and EPROM has two control lines and an output enable which gates data to the output lines. When $\bar{E} = 1$, the tri-state output buffers are placed in their high-impedance state (Z). The address dependency indicates that valid address range from 0 to 16383. IEEE standard symbol of TMS47256 32KB ROM is depicted in Fig. A.14. Pin 20 has dual function: one chip enable ($\bar{E}$) and other is power down input (E). This IC has a secondary chip select pin $\bar{S}_1$ which can also be programmed during mask fabrication to be either active high or active low. The address dependency represents the valid address range from 0 to 32767 and the eight affected data outputs.

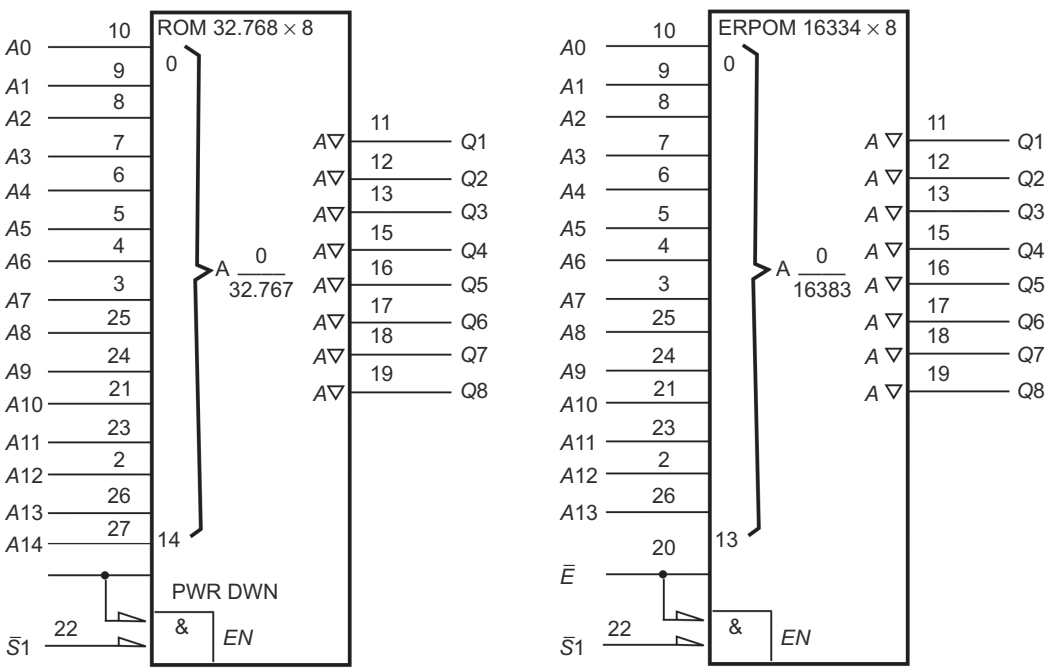


Fig. A.14

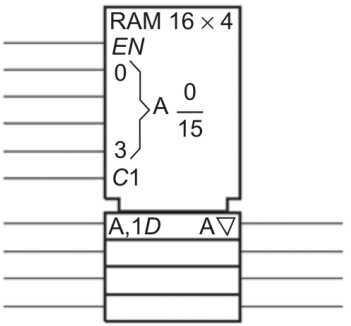


Fig. A.14 *IEEE standard symbol for memory*
(a) TMS27128 16KB EPROM
(b) TMS47256 32KB ROM
(c) RAM 16×4

A.11 ALU

The IEEE symbol for a 4-bit ALU IC 74×181 is shown in Fig. A.15. In common control block, the first five inputs form a mode control word which is represented by *M*. The weights of the mode control bits are powers of 2 and they are designated by a number in the range 0 to 31. As per IEEE standard, a separate table accompanies the logic symbol to define the functions performed in each mode. The output signals *CP*, *CG* and *CO* are enabled in modes 0 to 15. This IC has four individual ALU blocks which are labelled with the weight of the bits.

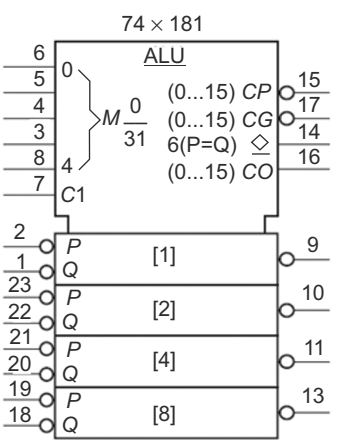


Fig. A.15 *IEEE symbol for ALU IC 74 × 181*