Table 1 8085 Data transfer instruction set summary

Opcode	Operand	Functions	Clock cycle	Number of bytes	Instruction code
MOV	Rd, Rs	Move register to register	4	1	0 1 D D D S S S
MOV	M, Rs	Move register to memory	7	1	0 1 1 1 0 S S S
MOV	Rd, M	Move memory to register	7	1	0 1 D D 1 1 0
MVI	Rd, data	Move immediate register	7	2	0 0 D D D 1 1 0
MVI	M, data	Move immediate memory	10	2	0 0 1 1 0 1 1 0
LDA	16 bit address	Load A direct	13	3	0 0 1 1 1 0 1 0
LDAX	B	Load A indirect	7	1	0 0 0 0 1 0 1 0
LDAX	D	Load A direct	7	1	0 0 0 1 1 0 1 0
LXI	B	Load immediate register Pair B & C	10	3	0 0 0 0 0 0 0 1
LXI	D	Load immediate register Pair D & E	10	3	0 0 0 1 0 0 0 1
LXI	H	Load immediate register Pair H & L	10	3	0 0 1 0 0 0 0 1
LXI	SP	Load immediate stack pointer	10	3	0 0 1 1 0 0 0 1
LHLD	16 bit address	Load H & L direct	16	3	0 0 1 0 1 0 1 0
STA	16 bit address	Load A direct	13	3	0 0 1 1 0 0 1 0
STAX	B	Store A indirect	7	1	0 0 0 0 0 0 1 0
STAX	D	Store A indirect	7	1	0 0 0 1 0 0 1 0
SHLD		Store H & L direct	16	1	0 0 1 0 0 0 1 0
XCHG		Exchange D & E H & L registers	4	1	1 1 1 0 1 0 1 1

Table 2 8085Arithmetic instruction set summary

Opcode	Operand	Functions	Clock cycle	Number of bytes	Instruction code							
ADD	R	Add register to A	4	1	1	0	0	0	0	S	S	S
ADD	M	Add memory to A	7	1	1	0	0	0	0	1	1	0
ADC	R	Add register to A with carry	4	1	1	0	0	0	1	S	S	S
ADC	M	Add memory to A with carry	7	1	1	0	0	0	1	1	1	0
ADI	8-bit data	Add immediate to A	7	2	1	1	0	0	0	1	1	0
ACI	8-bit data	Add immediate to A with carry	7	2	1	1	0	0	1	1	1	0
DAD	B	Add B & C to H & L	10	1	0	0	0	0	1	0	0	1
DAD	D	Add D & E to H & L	10	1	0	0	0	1	1	0	0	1
DAD	H	Add H & L to H & L	10	1	0	0	1	0	1	0	0	1
DAD	SP	Add stack pointer to H & L	10	1	0	0	1	1	1	0	0	1
SUB	R	Subtract register from A	4	1	1	0	0	1	0	S	S	S
SUB	M	Subtract memory from A	7	1	1	0	0	1	0	1	1	0
SBB	R	Subtract register from A with borrow	4	1	1	0	0	1	1	S	S	S
SBB	M	Subtract memory from A with borrow	7	1	1	0	0	1	1	1	1	0
SUI	8-bit data	Subtract immediate from A	7	2	1	1	0	1	0	1	1	0
SBI	8-bit data	Subtract immediate from A with borrow	7	2	1	1	0	1	1	1	1	0
INR	R	Increment register	4	1	0	0	D	D	D	1	0	0
INR	M	Increment memory	10	1	0	0	1	1	0	1	0	0
INX	B	Increment B & C registers	6	1	0	0	0	0	0	0	1	1
INX	D	Increment D & E registers	6	1	0	0	0	1	0	0	1	1
INX	H	Increment H & L registers	6	1	0	0	1	0	0	0	1	1
INX	SP	Increment stack pointer	6	1	0	0	1	1	0	0	1	1
DCR	R	Decrement register	4	1	0	0	D	D	D	1	0	1
DCR	M	Decrement memory	10	1	0	0	1	1	0	1	0	1
DCX	B	Decrement B & C registers	6	1	0	0	0	0	1	0	1	1
DCX	D	Decrement D & E registers	6	1	0	0	0	1	1	0	1	1
DCX	H	Decrement H & L registers	6	1	0	0	1	0	1	0	1	1
DCX	SP	Decrement stack pointer	6	1	0	0	1	1	1	0	1	1
DAA		Decimal adjustment	4	1	0	0	1	0	0	1	1	1

Table 3 8085 Logical instruction set summary

Opcode	Operand	Functions	Clock cycle	Number of bytes	Instruction code							
CMP	R	Compare register with A	4	1	1	0	1	1	1	S	S	S
CMP	M	Compare memory with A	7	1	1	0	0	0	0	1	1	0
CPI	8 bit data	Compare immediate with A	7	2	1	1	1	1	1	1	1	0
ANA	R	AND register with A	4	1	1	0	1	0	0	S	S	S
ANA	M	AND memory with A	7	1	1	0	1	0	0	1	1	0
ANI	8 bit data	AND immediate with A	7	2	1	1	1	0	0	1	1	0
ORA	R	OR register with A	4	1	1	0	1	1	0	S	S	S
ORA	M	OR memory with A	7	1	1	0	1	1	0	1	1	0
ORI	8 bit data	OR immediate with A	7	2	1	1	1	1	0	1	1	0
XRA	R	Exclusive OR register with A	4	1	1	0	1	0	1	S	S	S
XRA	M	Exclusive OR memory with A	7	1	1	0	1	0	1	1	1	0
XRI	8 bit data	Exclusive OR immediate with A	7	2	1	1	1	0	1	1	1	0
RLC		Rotate A left	4	1	0	0	0	0	0	1	1	1
RRC		Rotate A right	4	1	0	0	0	0	1	1	1	1
RAL		Rotate A left with carry	4	1	0	0	0	1	0	1	1	1
RAR		Rotate A right with carry	4	1	0	0	0	1	1	1	1	1
CMA		Complement A	4	1	0	0	1	0	1	1	1	1
CMC		Complement carry	4	1	0	0	1	1	1	1	1	1
STC		Set carry	4	1	0	0	1	1	0	1	1	1

Table 4 8085 JUMP instruction set summary

Opcode	Operand	Functions	Clock cycle	Number of bytes	Instruction code							
JMP	16-bit address	Jump unconditional	10	3	1	1	0	0	0	0	1	1
JC	16-bit address	Jump on Carry	7/10	3	1	1	0	1	1	0	1	0
JNC	16-bit address	Jump on no Carry	7/10	3	1	1	0	1	0	0	1	0
JP	16-bit address	Jump on positive	7/10	3	1	1	1	1	0	0	1	0
JM	16-bit address	Jump on minus	7/10	3	1	1	1	1	1	0	1	0
JZ	16-bit address	Jump on zero	7/10	3	1	1	0	0	1	0	1	0
JNZ	16-bit address	Jump on no zero	7/10	3	1	1	0	0	0	0	1	0
JPE	16-bit address	Jump on parity even	7/10	3	1	1	1	0	1	0	1	0
JPO	16-bit address	Jump on parity odd	7/10	3	1	1	1	0	0	0	1	0

Table 5 8085 CALL and Return instruction set summary

Opcode	Operand	Functions	Clock cycle	Number of bytes	Instruction code							
CALL	16-bit address	Call unconditional	18	3	1	1	0	0	1	1	0	1
CC	16-bit address	Call on Carry	9/18	3	1	1	0	1	1	1	0	0
CNC	16-bit address	Call on no Carry	9/18	3	1	1	0	1	0	1	0	0
CP	16-bit address	Call on positive	9/18	3	1	1	1	1	0	1	0	0
CM	16-bit address	Call on minus	9/18	3	1	1	1	1	1	1	0	0
CZ	16-bit address	Call on zero	9/18	3	1	1	0	0	1	1	0	0
CNZ	16-bit address	Call on no zero	9/18	3	1	1	0	0	0	1	0	0
CPE	16-bit address	Call on parity even	9/18	3	1	1	1	0	1	1	0	0
CPO	16-bit address	Call on parity odd	9/18	3	1	1	1	0	0	1	0	0

RET		Return unconditional	10	1	1	1	0	0	1	0	0	1
RC		Return on Carry	6/12	1	1	1	0	1	1	0	0	0
RNC		Return on no Carry	6/12	1	1	1	0	1	0	0	0	0
RP		Return on positive	6/12	1	1	1	1	1	0	0	0	0
RM		Return on minus	6/12	1	1	1	1	1	1	0	0	0
RZ		Return on zero	6/12	1	1	1	0	0	1	0	0	0
RNZ		Return on no zero	6/12	1	1	1	0	0	0	0	0	0
RPE		Return on parity even	6/12	1	1	1	1	0	1	0	0	0
RPO		Return on parity odd	6/12	1	1	1	1	0	0	0	0	0

Table 6 8085 Stack/PUSH and POP instructions set summary

Opcode	Operand	Functions	Clock cycle	Number of bytes	Instruction code							
PUSH	B	Push register pair Band C on stack	12	1	1	1	0	0	0	1	0	1
PUSH	D	Push register pair D and E on stack	12	1	1	1	0	1	0	1	0	1
PUSH	H	Push register pair H and L on stack	12	1	1	1	1	0	0	1	0	1
PUSH	PSW	Push accumulator A and Flags on stack	12	1	1	1	1	1	0	1	0	1
POP	B	Pop register pair Band C off stack	10	1	1	1	0	0	0	0	0	1
POP	D	Pop register pair D and E off stack	10	1	1	1	0	1	0	0	0	1
POP	H	Pop register pair H and L off stack	10	1	1	1	1	0	0	0	0	1
POP	PSW	Pop accumulator A and Flags off stack	10	1	1	1	1	1	0	0	0	1
XTHL		Exchange top of stack H and L	16	1	1	1	1	0	0	0	1	1
SPHL		H and L to stack pointer	6	1	1	1	1	1	1	0	0	1

Table 7 8085 I/O and machine control instructions set summary

Opcode	Operand	Functions	Clock cycle	Number of bytes	Instruction code							
EI		Enable interrupts	4	1	1	1	1	1	1	0	1	1
DI		Disable interrupts	4	1	1	1	1	1	0	0	1	1
NOP		No-operation	4	1	0	0	0	0	0	0	0	0
HLT		Halt(Power Down)	5	1	0	1	1	1	0	1	1	0
RIM		Read interrupt mask	4	1	0	0	1	0	0	0	0	0
SIM		Set interrupt musk	4	1	0	0	1	1	0	0	0	0
IN		Input	10	1	1	1	0	1	1	0	1	1
OUT		output	10	1	1	1	0	1	0	0	1	1