# Methods of Analysis

*No great work is ever done in a hurry. To develop a great scientific discovery, to print a great picture, to write an immortal poem, to become a minister, or a famous general—to do anything great requires time, patience, and perseverance. These things are done by degrees, "little by little."*

—W. J. Wilmont Buxton

## Enhancing Your Career

### Career in Electronics

One area of application for electric circuit analysis is electronics. The term *electronics* was originally used to distinguish circuits of very low current levels. This distinction no longer holds, as power semiconductor devices operate at high levels of current. Today, electronics is regarded as the science of the motion of charges in a gas, vacuum, or semiconductor. Modern electronics involves transistors and transistor circuits. The earlier electronic circuits were assembled from components. Many electronic circuits are now produced as integrated circuits, fabricated in a semiconductor substrate or chip.

Electronic circuits find applications in many areas, such as automation, broadcasting, computers, and instrumentation. The range of devices that use electronic circuits is enormous and is limited only by our imagination. Radio, television, computers, and stereo systems are but a few.

An electrical engineer usually performs diverse functions and is likely to use, design, or construct systems that incorporate some form of electronic circuits. Therefore, an understanding of the operation and analysis of electronics is essential to the electrical engineer. Electronics has become a specialty distinct from other disciplines within electrical engineering. Because the field of electronics is ever advancing, an electronics engineer must update his/her knowledge from time to time. The best way to do this is by being a member of a professional organization such as the Institute of Electrical and Electronics Engineers (IEEE). With a membership of over 300,000, the IEEE is the largest professional organization in the world. Members benefit immensely from the numerous magazines, journals, transactions, and conference/symposium proceedings published yearly by IEEE. You should consider becoming an IEEE member.
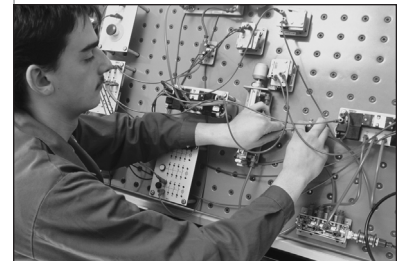


Troubleshooting an electronic circuit board.
© *Michael Rosenfeld/Getty Images*

## 3.1    Introduction

Having understood the fundamental laws of circuit theory (Ohm's law and Kirchhoff's laws), we are now prepared to apply these laws to develop two powerful techniques for circuit analysis: nodal analysis, which is based on a systematic application of Kirchhoff's current law (KCL), and mesh analysis, which is based on a systematic application of Kirchhoff's voltage law (KVL). The two techniques are so important that this chapter should be regarded as the most important in the book. Students are therefore encouraged to pay careful attention.

With the two techniques to be developed in this chapter, we can analyze any linear circuit by obtaining a set of simultaneous equations that are then solved to obtain the required values of current or voltage. One method of solving simultaneous equations involves Cramer's rule, which allows us to calculate circuit variables as a quotient of determinants. The examples in the chapter will illustrate this method; Appendix A also briefly summarizes the essentials the reader needs to know for applying Cramer's rule. Another method of solving simultaneous equations is to use *MATLAB*, a computer software discussed in Appendix E.

Also in this chapter, we introduce the use of *PSpice for Windows*, a circuit simulation computer software program that we will use throughout the text. Finally, we apply the techniques learned in this chapter to analyze transistor circuits.

## 3.2    Nodal Analysis

Nodal analysis provides a general procedure for analyzing circuits using node voltages as the circuit variables. Choosing node voltages instead of element voltages as circuit variables is convenient and reduces the number of equations one must solve simultaneously.

To simplify matters, we shall assume in this section that circuits do not contain voltage sources. Circuits that contain voltage sources will be analyzed in the next section.

In *nodal analysis*, we are interested in finding the node voltages. Given a circuit with $n$ nodes without voltage sources, the nodal analysis of the circuit involves taking the following three steps.

> **Steps to Determine Node Voltages:**
>
> 1. Select a node as the reference node. Assign voltages $v_1$, $v_2, \ldots, v_{n-1}$ to the remaining $n-1$ nodes. The voltages are referenced with respect to the reference node.
> 2. Apply KCL to each of the $n-1$ nonreference nodes. Use Ohm's law to express the branch currents in terms of node voltages.
> 3. Solve the resulting simultaneous equations to obtain the unknown node voltages.

We shall now explain and apply these three steps.

The first step in nodal analysis is selecting a node as the *reference* or *datum node*. The reference node is commonly called the *ground*

Nodal analysis is also known as the *node-voltage method*.

since it is assumed to have zero potential. A reference node is indicated by any of the three symbols in Fig. 3.1. The type of ground in Fig. 3.1(b) is called a *chassis ground* and is used in devices where the case, enclosure, or chassis acts as a reference point for all circuits. When the potential of the earth is used as reference, we use the *earth ground* in Fig. 3.1(a) or (c). We shall always use the symbol in Fig. 3.1(b).

Once we have selected a reference node, we assign voltage designations to nonreference nodes. Consider, for example, the circuit in Fig. 3.2(a). Node 0 is the reference node ($v = 0$), while nodes 1 and 2 are assigned voltages $v_1$ and $v_2$, respectively. Keep in mind that the node voltages are defined with respect to the reference node. As illustrated in Fig. 3.2(a), each node voltage is the voltage rise from the reference node to the corresponding nonreference node or simply the voltage of that node with respect to the reference node.

As the second step, we apply KCL to each nonreference node in the circuit. To avoid putting too much information on the same circuit, the circuit in Fig. 3.2(a) is redrawn in Fig. 3.2(b), where we now add $i_1$, $i_2$, and $i_3$ as the currents through resistors $R_1$, $R_2$, and $R_3$, respectively. At node 1, applying KCL gives

$$I_1 = I_2 + i_1 + i_2 \tag{3.1}$$

At node 2,

$$I_2 + i_2 = i_3 \tag{3.2}$$

We now apply Ohm's law to express the unknown currents $i_1$, $i_2$, and $i_3$ in terms of node voltages. The key idea to bear in mind is that, since resistance is a passive element, by the passive sign convention, current must always flow from a higher potential to a lower potential.

Current flows from **a higher** potential to **a lower** potential in a resistor.

We can express this principle as

$$i = \frac{v_{\text{higher}} - v_{\text{lower}}}{R} \tag{3.3}$$

Note that this principle is in agreement with the way we defined resistance in Chapter 2 (see Fig. 2.1). With this in mind, we obtain from Fig. 3.2(b),

$$i_1 = \frac{v_1 - 0}{R_1} \qquad \text{or} \qquad i_1 = G_1 v_1$$

$$i_2 = \frac{v_1 - v_2}{R_2} \qquad \text{or} \qquad i_2 = G_2(v_1 - v_2) \tag{3.4}$$

$$i_3 = \frac{v_2 - 0}{R_3} \qquad \text{or} \qquad i_3 = G_3 v_2$$

Substituting Eq. (3.4) in Eqs. (3.1) and (3.2) results, respectively, in

$$I_1 = I_2 + \frac{v_1}{R_1} + \frac{v_1 - v_2}{R_2} \tag{3.5}$$

$$I_2 + \frac{v_1 - v_2}{R_2} = \frac{v_2}{R_3} \tag{3.6}$$

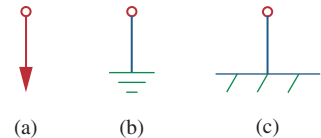The number of nonreference nodes is equal to the number of independent equations that we will derive.



**Figure 3.1**
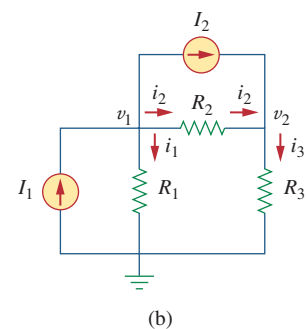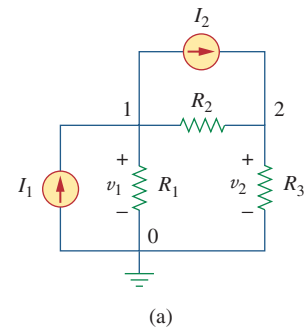Common symbols for indicating a reference node, (a) common ground, (b) ground, (c) chassis ground.



(a)



(b)

**Figure 3.2**
Typical circuit for nodal analysis.

In terms of the conductances, Eqs. (3.5) and (3.6) become

$$I_1 = I_2 + G_1 v_1 + G_2(v_1 - v_2) \qquad \text{(3.7)}$$

$$I_2 + G_2(v_1 - v_2) = G_3 v_2 \qquad \text{(3.8)}$$

The third step in nodal analysis is to solve for the node voltages. If we apply KCL to $n - 1$ nonreference nodes, we obtain $n - 1$ simultaneous equations such as Eqs. (3.5) and (3.6) or (3.7) and (3.8). For the circuit of Fig. 3.2, we solve Eqs. (3.5) and (3.6) or (3.7) and (3.8) to obtain the node voltages $v_1$ and $v_2$ using any standard method, such as the substitution method, the elimination method, Cramer's rule, or matrix inversion. To use either of the last two methods, one must cast the simultaneous equations in matrix form. For example, Eqs. (3.7) and (3.8) can be cast in matrix form as

> Appendix A discusses how to use Cramer's rule.

$$\begin{bmatrix} G_1 + G_2 & -G_2 \\ -G_2 & G_2 + G_3 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} I_1 - I_2 \\ I_2 \end{bmatrix} \qquad \text{(3.9)}$$

which can be solved to get $v_1$ and $v_2$. Equation 3.9 will be generalized in Section 3.6. The simultaneous equations may also be solved using calculators or with software packages such as *MATLAB*, *Mathcad*, *Maple*, and *Quattro Pro*.

## Example 3.1

Calculate the node voltages in the circuit shown in Fig. 3.3(a).

**Solution:**
Consider Fig. 3.3(b), where the circuit in Fig. 3.3(a) has been prepared for nodal analysis. Notice how the currents are selected for the application of KCL. Except for the branches with current sources, the labeling of the currents is arbitrary but consistent. (By consistent, we mean that if, for example, we assume that $i_2$ enters the 4 Ω resistor from the left-hand side, $i_2$ must leave the resistor from the right-hand side.) The reference node is selected, and the node voltages $v_1$ and $v_2$ are now to be determined.

At node 1, applying KCL and Ohm's law gives

$$i_1 = i_2 + i_3 \qquad \Rightarrow \qquad 5 = \frac{v_1 - v_2}{4} + \frac{v_1 - 0}{2}$$

Multiplying each term in the last equation by 4, we obtain

$$20 = v_1 - v_2 + 2v_1$$

or

$$3v_1 - v_2 = 20 \qquad \text{(3.1.1)}$$

At node 2, we do the same thing and get

$$i_2 + i_4 = i_1 + i_5 \qquad \Rightarrow \qquad \frac{v_1 - v_2}{4} + 10 = 5 + \frac{v_2 - 0}{6}$$

Multiplying each term by 12 results in

$$3v_1 - 3v_2 + 120 = 60 + 2v_2$$

or

$$-3v_1 + 5v_2 = 60 \qquad \text{(3.1.2)}$$



(a)



(b)

**Figure 3.3**
For Example 3.1: (a) original circuit, (b) circuit for analysis.

Now we have two simultaneous Eqs. (3.1.1) and (3.1.2). We can solve the equations using any method and obtain the values of $v_1$ and $v_2$.

■ **METHOD 1**    Using the elimination technique, we add Eqs. (3.1.1) and (3.1.2).

$$4v_2 = 80 \quad \Rightarrow \quad v_2 = 20 \text{ V}$$

Substituting $v_2 = 20$ in Eq. (3.1.1) gives

$$3v_1 - 20 = 20 \quad \Rightarrow \quad v_1 = \frac{40}{3} = 13.33 \text{ V}$$

■ **METHOD 2**    To use Cramer's rule, we need to put Eqs. (3.1.1) and (3.1.2) in matrix form as

$$\begin{bmatrix} 3 & -1 \\ -3 & 5 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} 20 \\ 60 \end{bmatrix} \qquad \textbf{(3.1.3)}$$

The determinant of the matrix is

$$\Delta = \begin{vmatrix} 3 & -1 \\ -3 & 5 \end{vmatrix} = 15 - 3 = 12$$

We now obtain $v_1$ and $v_2$ as

$$v_1 = \frac{\Delta_1}{\Delta} = \frac{\begin{vmatrix} 20 & -1 \\ 60 & 5 \end{vmatrix}}{\Delta} = \frac{100 + 60}{12} = 13.33 \text{ V}$$

$$v_2 = \frac{\Delta_2}{\Delta} = \frac{\begin{vmatrix} 3 & 20 \\ -3 & 60 \end{vmatrix}}{\Delta} = \frac{180 + 60}{12} = 20 \text{ V}$$

giving us the same result as did the elimination method.

If we need the currents, we can easily calculate them from the values of the nodal voltages.

$$i_1 = 5 \text{ A}, \qquad i_2 = \frac{v_1 - v_2}{4} = -1.6667 \text{ A}, \qquad i_3 = \frac{v_1}{2} = 6.666 \text{ A}$$

$$i_4 = 10 \text{ A}, \qquad i_5 = \frac{v_2}{6} = 3.333 \text{ A}$$

The fact that $i_2$ is negative shows that the current flows in the direction opposite to the one assumed.

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Obtain the node voltages in the circuit in Fig. 3.4.

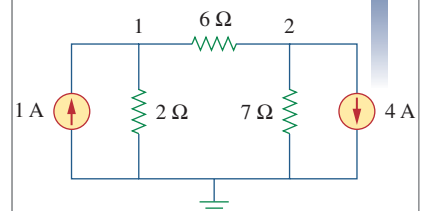**Answer:** $v_1 = -2$ V, $v_2 = -14$ V.

**Practice Problem 3.1**
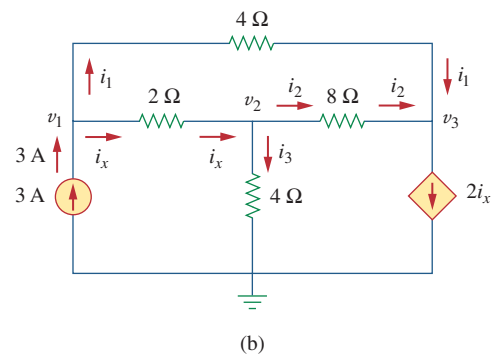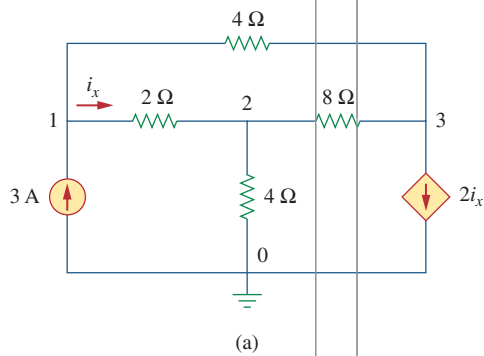


**Figure 3.4**
For Practice Prob. 3.1.

## Example 3.2

Determine the voltages at the nodes in Fig. 3.5(a).

**Solution:**
The circuit in this example has three nonreference nodes, unlike the previous example which has two nonreference nodes. We assign voltages to the three nodes as shown in Fig. 3.5(b) and label the currents.



**Figure 3.5**
For Example 3.2: (a) original circuit, (b) circuit for analysis.

At node 1,

$$3 = i_1 + i_x \qquad \Rightarrow \qquad 3 = \frac{v_1 - v_3}{4} + \frac{v_1 - v_2}{2}$$

Multiplying by 4 and rearranging terms, we get

$$3v_1 - 2v_2 - v_3 = 12 \tag{3.2.1}$$

At node 2,

$$i_x = i_2 + i_3 \qquad \Rightarrow \qquad \frac{v_1 - v_2}{2} = \frac{v_2 - v_3}{8} + \frac{v_2 - 0}{4}$$

Multiplying by 8 and rearranging terms, we get

$$-4v_1 + 7v_2 - v_3 = 0 \tag{3.2.2}$$

At node 3,

$$i_1 + i_2 = 2i_x \qquad \Rightarrow \qquad \frac{v_1 - v_3}{4} + \frac{v_2 - v_3}{8} = \frac{2(v_1 - v_2)}{2}$$

Multiplying by 8, rearranging terms, and dividing by 3, we get

$$2v_1 - 3v_2 + v_3 = 0 \tag{3.2.3}$$

We have three simultaneous equations to solve to get the node voltages $v_1$, $v_2$, and $v_3$. We shall solve the equations in three ways.

■ **METHOD 1**    Using the elimination technique, we add Eqs. (3.2.1) and (3.2.3).

$$5v_1 - 5v_2 = 12$$

or

$$v_1 - v_2 = \frac{12}{5} = 2.4 \tag{3.2.4}$$

Adding Eqs. (3.2.2) and (3.2.3) gives

$$-2v_1 + 4v_2 = 0 \qquad \Rightarrow \qquad v_1 = 2v_2 \tag{3.2.5}$$

Substituting Eq. (3.2.5) into Eq. (3.2.4) yields

$$2v_2 - v_2 = 2.4 \quad \Rightarrow \quad v_2 = 2.4, \qquad v_1 = 2v_2 = 4.8 \text{ V}$$

From Eq. (3.2.3), we get

$$v_3 = 3v_2 - 2v_1 = 3v_2 - 4v_2 = -v_2 = -2.4 \text{ V}$$

Thus,

$$v_1 = 4.8 \text{ V}, \qquad v_2 = 2.4 \text{ V}, \qquad v_3 = -2.4 \text{ V}$$

■ **METHOD 2**   To use Cramer's rule, we put Eqs. (3.2.1) to (3.2.3) in matrix form.

$$\begin{bmatrix} 3 & -2 & -1 \\ -4 & 7 & -1 \\ 2 & -3 & 1 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \end{bmatrix} = \begin{bmatrix} 12 \\ 0 \\ 0 \end{bmatrix} \qquad \textbf{(3.2.6)}$$

From this, we obtain

$$v_1 = \frac{\Delta_1}{\Delta}, \qquad v_2 = \frac{\Delta_2}{\Delta}, \qquad v_3 = \frac{\Delta_3}{\Delta}$$

where $\Delta$, $\Delta_1$, $\Delta_2$, and $\Delta_3$ are the determinants to be calculated as follows. As explained in Appendix A, to calculate the determinant of a 3 by 3 matrix, we repeat the first two rows and cross multiply.

$$\Delta = \begin{vmatrix} 3 & -2 & -1 \\ -4 & 7 & -1 \\ 2 & -3 & 1 \end{vmatrix} = \begin{matrix} \begin{vmatrix} 3 & -2 & -1 \\ -4 & 7 & -1 \\ 2 & -3 & 1 \\ 3 & -2 & -1 \\ -4 & 7 & -1 \end{vmatrix} \end{matrix}$$

$$= 21 - 12 + 4 + 14 - 9 - 8 = 10$$

Similarly, we obtain

$$\Delta_1 = \begin{vmatrix} 12 & -2 & -1 \\ 0 & 7 & -1 \\ 0 & -3 & 1 \\ 12 & -2 & -1 \\ 0 & 7 & -1 \end{vmatrix} = 84 + 0 + 0 - 0 - 36 - 0 = 48$$

$$\Delta_2 = \begin{vmatrix} 3 & 12 & -1 \\ -4 & 0 & -1 \\ 2 & 0 & 1 \\ 3 & 12 & -1 \\ -4 & 0 & -1 \end{vmatrix} = 0 + 0 - 24 - 0 - 0 + 48 = 24$$

$$\Delta_3 = \begin{vmatrix} 3 & -2 & 12 \\ -4 & 7 & 0 \\ 2 & -3 & 0 \\ 3 & -2 & 12 \\ -4 & 7 & 0 \end{vmatrix} = 0 + 144 + 0 - 168 - 0 - 0 = -24$$

Thus, we find

$$v_1 = \frac{\Delta_1}{\Delta} = \frac{48}{10} = 4.8 \text{ V}, \qquad v_2 = \frac{\Delta_2}{\Delta} = \frac{24}{10} = 2.4 \text{ V}$$

$$v_3 = \frac{\Delta_3}{\Delta} = \frac{-24}{10} = -2.4 \text{ V}$$

as we obtained with Method 1.

■ **METHOD 3**   We now use *MATLAB* to solve the matrix. Equation (3.2.6) can be written as

$$\mathbf{AV} = \mathbf{B} \qquad \Rightarrow \qquad \mathbf{V} = \mathbf{A}^{-1}\mathbf{B}$$

where **A** is the 3 by 3 square matrix, **B** is the column vector, and **V** is a column vector comprised of $v_1$, $v_2$, and $v_3$ that we want to determine. We use *MATLAB* to determine **V** as follows:

$$>>A = [3 \quad -2 \quad -1; \quad -4 \quad 7 \quad -1; \quad 2 \quad -3 \quad 1];$$
$$>>B = [12 \quad 0 \quad 0];$$
$$>>V = \text{inv}(A) * B$$

$$V = \begin{matrix} 4.8000 \\ 2.4000 \\ -2.4000 \end{matrix}$$

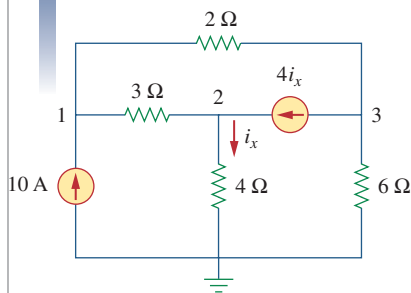Thus, $v_1 = 4.8$ V, $v_2 = 2.4$ V, and $v_3 = -2.4$ V, as obtained previously.

**Figure 3.6**
For Practice Prob. 3.2.

Find the voltages at the three nonreference nodes in the circuit of Fig. 3.6.

**Answer:** $v_1 = 80$ V, $v_2 = -64$ V, $v_3 = 156$ V.

**3.3**        Nodal Analysis with Voltage Sources

We now consider how voltage sources affect nodal analysis. We use the circuit in Fig. 3.7 for illustration. Consider the following two possibilities.

■ **CASE 1**   If a voltage source is connected between the reference node and a nonreference node, we simply set the voltage at the nonreference node equal to the voltage of the voltage source. In Fig. 3.7, for example,

$$v_1 = 10 \text{ V} \tag{3.10}$$

Thus our analysis is somewhat simplified by this knowledge of the voltage at this node.

■ **CASE 2**   If the voltage source (dependent or independent) is connected between two nonreference nodes, the two nonreference nodes
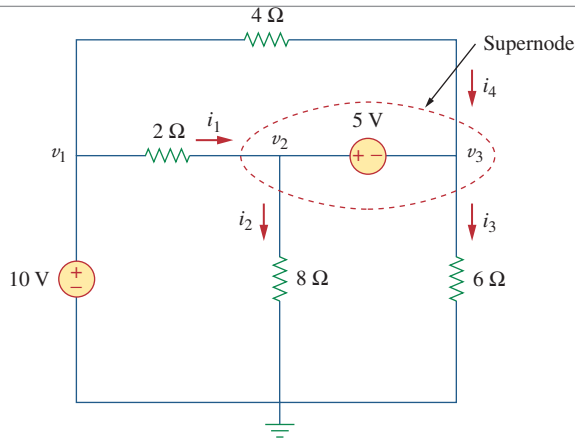
**Figure 3.7**
A circuit with a supernode.

form a *generalized node* or *supernode*; we apply both KCL and KVL to determine the node voltages.

> A **supernode** is formed by enclosing a (dependent or independent) voltage source connected between two nonreference nodes and any elements connected in parallel with it.

In Fig. 3.7, nodes 2 and 3 form a supernode. (We could have more than two nodes forming a single supernode. For example, see the circuit in Fig. 3.14.) We analyze a circuit with supernodes using the same three steps mentioned in the previous section except that the supernodes are treated differently. Why? Because an essential component of nodal analysis is applying KCL, which requires knowing the current through each element. There is no way of knowing the current through a voltage source in advance. However, KCL must be satisfied at a supernode like any other node. Hence, at the supernode in Fig. 3.7,

$$i_1 + i_4 = i_2 + i_3 \qquad \textbf{(3.11a)}$$

or

$$\frac{v_1 - v_2}{2} + \frac{v_1 - v_3}{4} = \frac{v_2 - 0}{8} + \frac{v_3 - 0}{6} \qquad \textbf{(3.11b)}$$

To apply Kirchhoff's voltage law to the supernode in Fig. 3.7, we redraw the circuit as shown in Fig. 3.8. Going around the loop in the clockwise direction gives

$$-v_2 + 5 + v_3 = 0 \qquad \Rightarrow \qquad v_2 - v_3 = 5 \qquad \textbf{(3.12)}$$

From Eqs. (3.10), (3.11b), and (3.12), we obtain the node voltages.
    Note the following properties of a supernode:

1. The voltage source inside the supernode provides a constraint equation needed to solve for the node voltages.
2. A supernode has no voltage of its own.
3. A supernode requires the application of both KCL and KVL.

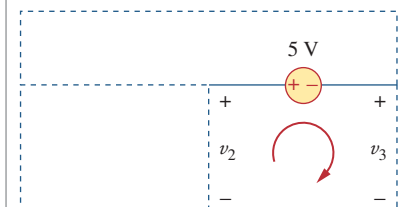> A supernode may be regarded as a closed surface enclosing the voltage source and its two nodes.



**Figure 3.8**
Applying KVL to a supernode.
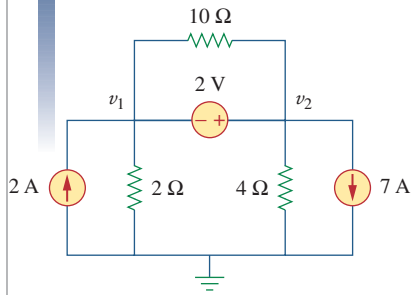
## Example 3.3



**Figure 3.9**
For Example 3.3.

For the circuit shown in Fig. 3.9, find the node voltages.

**Solution:**
The supernode contains the 2-V source, nodes 1 and 2, and the 10-$\Omega$ resistor. Applying KCL to the supernode as shown in Fig. 3.10(a) gives

$$2 = i_1 + i_2 + 7$$

Expressing $i_1$ and $i_2$ in terms of the node voltages

$$2 = \frac{v_1 - 0}{2} + \frac{v_2 - 0}{4} + 7 \quad \Rightarrow \quad 8 = 2v_1 + v_2 + 28$$

or

$$v_2 = -20 - 2v_1 \tag{3.3.1}$$

To get the relationship between $v_1$ and $v_2$, we apply KVL to the circuit in Fig. 3.10(b). Going around the loop, we obtain

$$-v_1 - 2 + v_2 = 0 \quad \Rightarrow \quad v_2 = v_1 + 2 \tag{3.3.2}$$

From Eqs. (3.3.1) and (3.3.2), we write

$$v_2 = v_1 + 2 = -20 - 2v_1$$

or

$$3v_1 = -22 \quad \Rightarrow \quad v_1 = -7.333 \text{ V}$$

and $v_2 = v_1 + 2 = -5.333$ V. Note that the 10-$\Omega$ resistor does not make any difference because it is connected across the supernode.
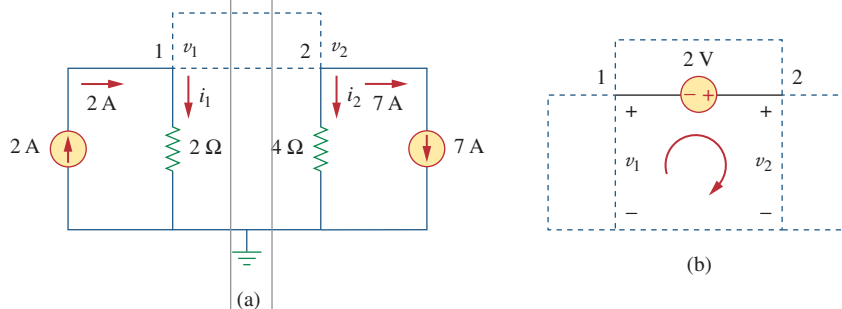


(a)



(b)

**Figure 3.10**
Applying: (a) KCL to the supernode, (b) KVL to the loop.
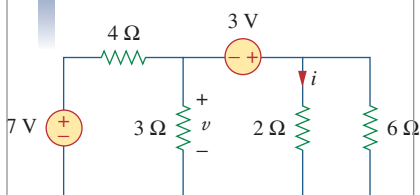
## Practice Problem 3.3



**Figure 3.11**
For Practice Prob. 3.3.

Find $v$ and $i$ in the circuit in Fig. 3.11.

**Answer:** $-0.2$ V, 1.4 A.

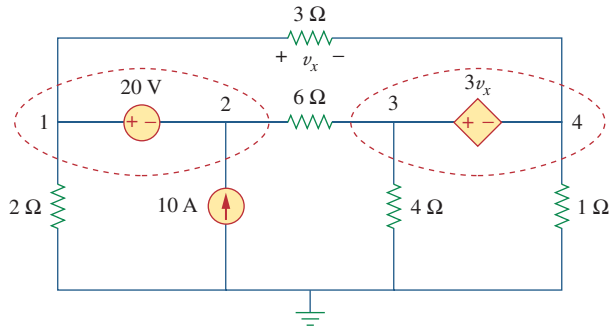Find the node voltages in the circuit of Fig. 3.12.

Example 3.4



**Figure 3.12**
For Example 3.4.

**Solution:**
Nodes 1 and 2 form a supernode; so do nodes 3 and 4. We apply KCL to the two supernodes as in Fig. 3.13(a). At supernode 1-2,

$$i_3 + 10 = i_1 + i_2$$

Expressing this in terms of the node voltages,

$$\frac{v_3 - v_2}{6} + 10 = \frac{v_1 - v_4}{3} + \frac{v_1}{2}$$

or

$$5v_1 + v_2 - v_3 - 2v_4 = 60 \qquad \textbf{(3.4.1)}$$

At supernode 3-4,

$$i_1 = i_3 + i_4 + i_5 \quad \Rightarrow \quad \frac{v_1 - v_4}{3} = \frac{v_3 - v_2}{6} + \frac{v_4}{1} + \frac{v_3}{4}$$
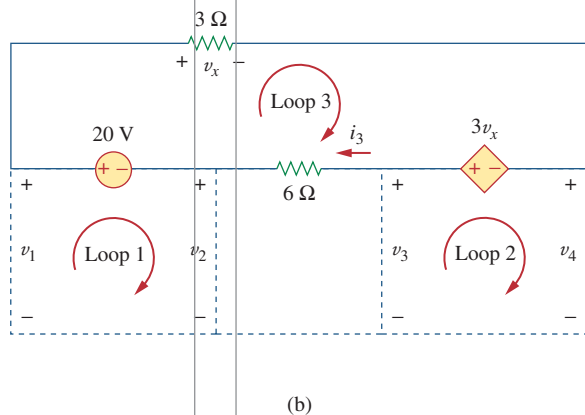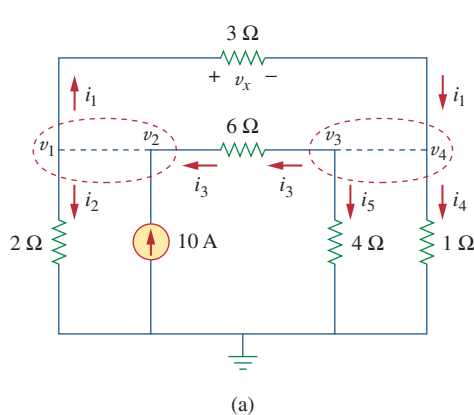
or

$$4v_1 + 2v_2 - 5v_3 - 16v_4 = 0 \qquad \textbf{(3.4.2)}$$



(a)

(b)

**Figure 3.13**
Applying: (a) KCL to the two supernodes, (b) KVL to the loops.