Mixed-Signal Measurement Solutions: Which One Fits Your Application Needs?

Application Note 1424

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Introduction

At one time the boundaries between analog and digital designs were clearly defined. With the increasing complexity and performance levels of system designs, maintaining these boundaries has become more difficult.

Today many designers are working with boards that include a mix of analog and digital components. In addition, high-speed digital signals require significant insight into their analog characteristics as they pertain to signal integrity margins.

Unfortunately, the mixing of these environments can create challenges when it comes to selecting test equipment. Designers need the ability to either time-correlate the signals between analog and digital devices in their designs or view time-correlated analog and digital views of the same signal.

The traditional solution of two stand-alone instruments operating independently – an oscilloscope for analog analysis and a logic analyzer for digital analysis – has become cumbersome and insufficient. The new age of mixed-signal analysis requires solutions that bring the analog and digital worlds together in a seamless fashion.

Agilent Technologies

Introduction

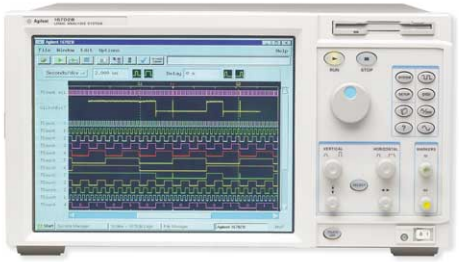
Agilent Technologies offers three solutions that address the mixed-signal environment by providing views of both analog and digital data in a time-correlated fashion.

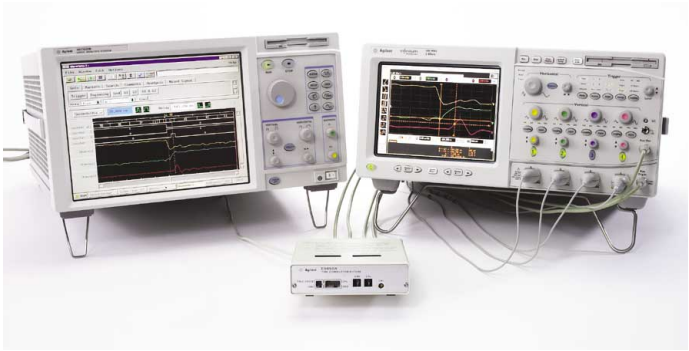
- **The scope-centric solution** – A mixed signal oscilloscope (MSO) uses the physical form factor and system software of a traditional digital oscilloscope. The instrument is enhanced for mixed-signal analysis with the addition of some basic logic analyzer functionality.

- **The logic-centric solution** – An oscilloscope module uses the physical form factor and system software of the host logic analyzer. The mixed-signal capabilities are achieved via the module's basic analog acquisition and analysis capabilities. In addition, newer logic analyzers are also capable of acquiring analog eye diagrams with a feature called eye scan.

- **The extended logic-centric solution** – A stand-alone oscilloscope and a stand-alone logic analyzer connected together via the Agilent E5850A time correlation fixture compose the extended logic-centric solution. The user has access to all of the features and functionality of each instrument. In addition, the instruments are automatically deskewed and data is shared between them so that time-correlated analog and digital data can be viewed.

On the surface, each of these solutions provides the same fundamental benefit – the ability to capture and view time-correlated analog and digital data in the same display. But it is important to look deeper into the specifications, functionality, and intended use models of each solution to fully understand how they differ and how each one is best suited for specific types of applications.





Scope-Centric Solution: The Mixed Signal Oscilloscope

The mixed signal oscilloscope (MSO) was pioneered by Agilent Technologies in 1996 and was quickly adopted as a primary test instrument by designers of microcontroller- and DSP-based embedded systems. Although originally limited by its 100 MHz bandwidth, recent advances in MSO technology with bandwidths up to 1 GHz have made this solution attractive to many users.

An MSO combines either 2 or 4 analog channels with 16 digital channels to provide up to 20 time-correlated data channels. An MSO can be considered a true replacement for a traditional DSO because it contains all of the same analog analysis capabilities including standard time and voltage measurements (e.g., rise/fall times, frequency, overshoot, amplitude, etc.), histograms, waveform math, FFTs, and eye diagrams. In addition to this customary functionality, the MSO adds basic digital timing analysis and deep memory.

As a result of this combined functionality, complex technology can be more easily observed because the MSO provides more channels, more memory, and more triggering capability than any traditional DSO available on the market. As an example, the MSO screen in Figure 1 shows a deep trace of five digital waveforms correlated to a single analog signal.

Use models

An MSO lends itself to two primary use models. The first is a true mixed-signal environment that typically combines slower analog signals with faster digital control signals from microcontrollers or DSPs. The ability to trigger across all channels allows the designer to use the extra digital channels to qualify the trigger and the analog channels to perform the necessary debug analysis. In addition, deep memory allows for long capture of the slower analog signals and high resolution capture at a fast sample rate of the digital signals.

In the second use model, a designer who is interested in viewing the analog characteristics of a digital signal for signal integrity purposes can view a bus using the digital channels and see a time-correlated analog view of any of the signals by probing them with an analog channel.

Strengths and limitations

The strengths of the scope-centric MSO solution consist of tightly time-correlated analog and digital waveforms in a single display, triggering across all channels, and the familiar and easy-to-use DSO user interface and front panel controls. In addition, the single instrument approach saves bench space and greatly simplifies setup tasks. For many simple 8-bit and 16-bit MCU/DSP-based designs, the 16 digital channels are all that are needed to debug the system, and no additional logic analyzer functionality is necessary.

While it is true that the MSO can not be considered a replacement for a full featured logic analyzer because it does not have state analysis, complex multi-sequence triggering, more than 16 digital channels, or the performance specifications of higher end analyzers, it is an excellent complement to this high-end functionality.

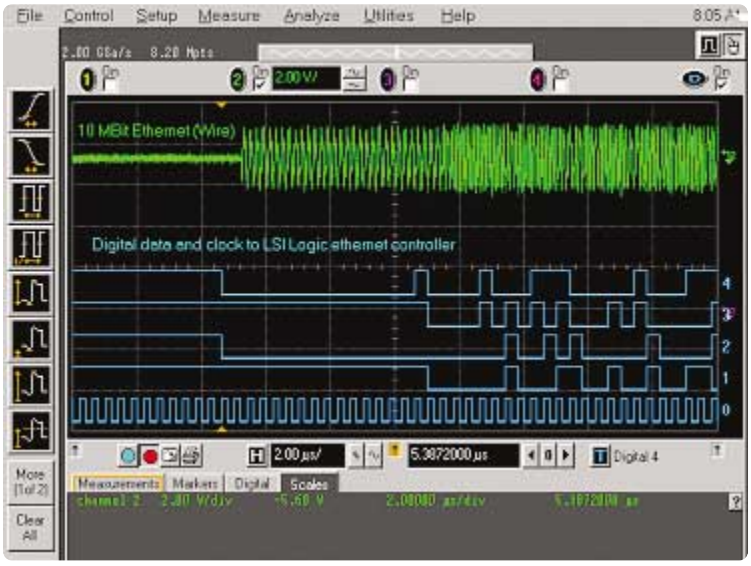


Figure 1. MSO display correlating analog and digital waveforms

Logic-Centric Solution: The Logic Analyzer Scope Module and Eye Scan

The oscilloscope module for logic analyzers approaches the mixed-signal analysis problem from the opposite direction of the MSO. This solution consists of an optional module that is added to the logic analyzer instrument and provides at least two channels of analog acquisition time-correlated with the potentially hundreds of digital channels provided by the logic analyzer. Multiple scope modules can be combined so that as many as eight analog channels on a common time base can be used. In addition to all of the digital analysis tools commonly available in a logic analyzer, the designer has access to basic analog analysis capabilities provided by the scope, but in a single instrument.

The data associated with the analog channels can be displayed on the instrument in two different windows, depending on the type of analysis the user needs. The first display, shown in Figure 2, provides very basic scope functionality such as time and voltage measurements, triggering, and the vertical voltage resolution necessary for analyzing analog signals. While this display does not integrate analog and digital data into the same view, the scope viewer is time-correlated to the logic analyzer's waveform viewer, and global markers can be used to mark correlated positions on both displays.

The display shown in Figure 3, the second option, is similar to the approach used by the MSO to display signals. This display integrates views of both analog and digital waveforms using the logic analyzer's waveform display. While it sacrifices vertical voltage resolution on the analog waveforms, it clearly displays the analog signals time-correlated to the digital signals of interest.

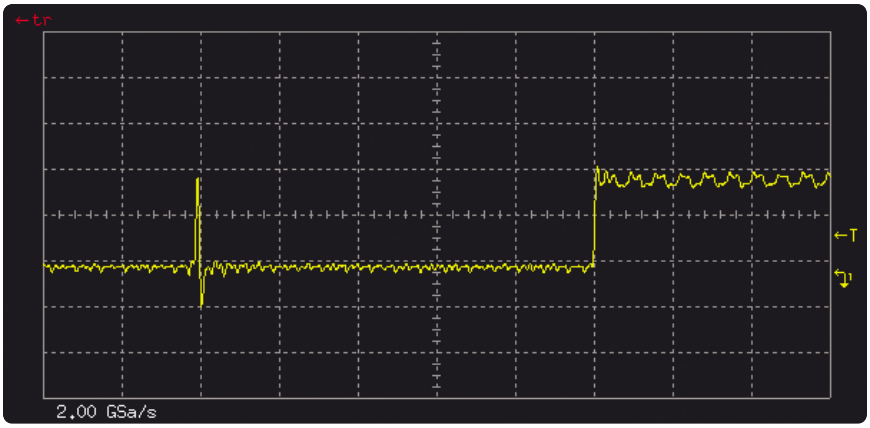


Figure 2. Oscilloscope module display on a logic analyzer

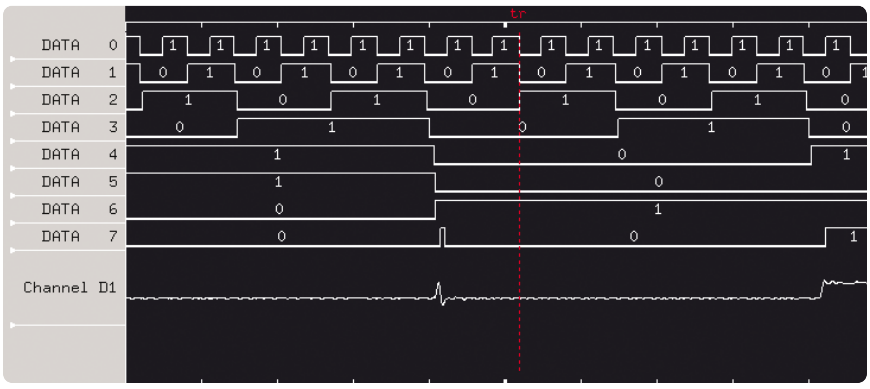


Figure 3. Integrated display of analog and digital data in logic analyzer waveform display

Use models

The logic analyzer scope module fits into two primary mixed-signal analysis use models. The first is an application that requires an analog view of a signal in addition to the digital waveform provided by the logic analyzer. The logic analyzer scope module would typically check or verify certain analog characteristics of a digital waveform such as rise time or voltage levels. The second use model is a broader debug application that requires correlation from an analog signal to a digital waveform, state mode listing display, or even to source code.

Strengths and limitations

The strengths of logic-centric solutions include tightly time-correlated data, high channel counts for digital data, both integrated waveform displays and a separate scope display, the ability to correlate analog characteristics to events in a state listing or in actual source code, easy cross triggering, and the possibility of having up to eight analog channels. Like the MSO, this single instrument form factor saves bench space and requires minimal setup for mixed-signal analysis. It will also be familiar to any digital designer experienced with a logic analyzer.

The oscilloscope module cannot fully replace a stand-alone DSO because the feature set is limited and does not include more advanced analog analysis tools such as waveform math, FFTs, and histograms. In addition, the scope module does not have the benefit of the high resolution and fast update displays typical of most DSOs. This makes the scope module really only adequate for single shot measurements.

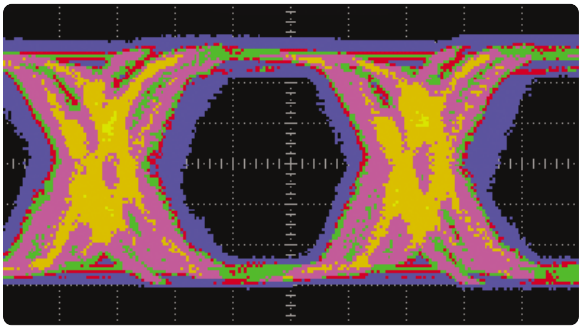


Figure 4. Eye scan diagram

Eye scan

In addition to the scope module, newer logic analyzers offer an option for performing additional analog analysis on high-speed signals without any additional acquisition hardware or probing.

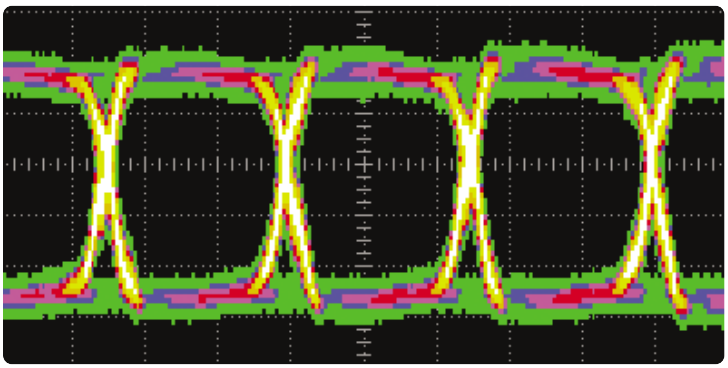
The eye scan feature available in the 16753/4/5/6 and 16760 logic analyzers is a clock synchronous measurement that generates eye diagrams across many signals. While eye scan is not a time-correlated measurement in the traditional sense of mixed-signal analysis, it is an analog representation of voltage transitions across time for digital signals. An eye scan measurement is shown in Figure 4. This eye diagram is a composite of all channels in a 16-bit bus.

This feature expands the logic analyzer into the signal integrity territory generally left to oscilloscopes and other instruments by allowing a designer to easily validate such things as setup/hold margins, eye openings, and threshold voltages. By generating eye diagrams for up to 339 signals in a single run, eye scan can quickly identify errant signals that require further analysis. The feature offers the user a variety of tools to measure the eye opening, generate histograms, overlay the individual signals, or alter the color grading to better highlight problems.

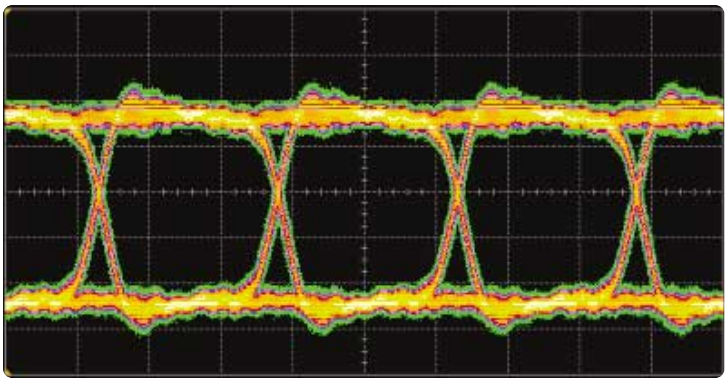
Strengths and limitations

Eye scan's strength is that it can generate eye diagrams for hundreds of signals in a single run in a fraction of the time it would take to make the same measurements with a scope. The resulting eye diagrams are very similar to those generated by an oscilloscope, as shown in Figure 5.

Eye scan is limited in terms of its voltage resolution and its ability to detect activity when no data transitions are occurring. It can quickly flag problems, but precise signal integrity measurements still require an oscilloscope.



a. 800 Mb/s PRBS measured with eye scan



b. 800 Mb/s PRBS measured with an Agilent Infiniium oscilloscope

Figure 5. Comparison of eye scan and oscilloscope eye diagrams

Extended Logic-Centric Solution: Time Correlation Fixture

An MSO and a logic analyzer scope module both achieve a single instrument solution but trade off either logic analyzer functionality, in the case of the MSO, or scope functionality, in the case of the logic analyzer scope module. The extended logic-centric solution, on the other hand, limits functionality trade offs by using two stand-alone instruments to achieve mixed-signal analysis.

In this solution, the logic analyzer and oscilloscope are connected and communicate with each other in order to deskew and time correlate their acquisitions and integrate the data displays. The setup for this solution requires the Agilent E5850A time correlation fixture to provide a common clock edge that synchronizes the two instruments. One channel of each instrument is attached to the calibration signal generated by the E5850A, and a calibration routine is run to calculate the skew between the instruments and adjust for it.

In addition to simply correlating the data between the two instruments, this solution also provides other useful features. First, the waveforms from the oscilloscope are displayed in the logic analyzer's waveform display, as shown in Figure 6a. Second, the global markers on the logic analyzer are locked to the time markers on the scope, so if you move marker G1 on the logic analyzer, marker Ax moves to the corresponding position on the scope display, and vice versa. Figure 6b shows the positions marked in the logic analyzer's waveform display also marked in the oscilloscope display.

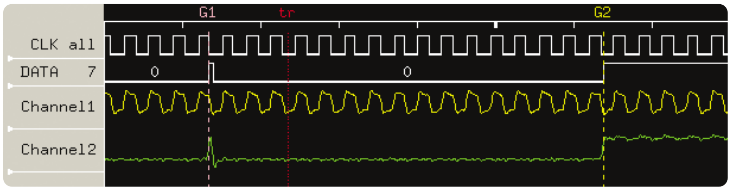


Figure 6a. Global markers G1 and G2 placed in the logic analyzer's waveform display

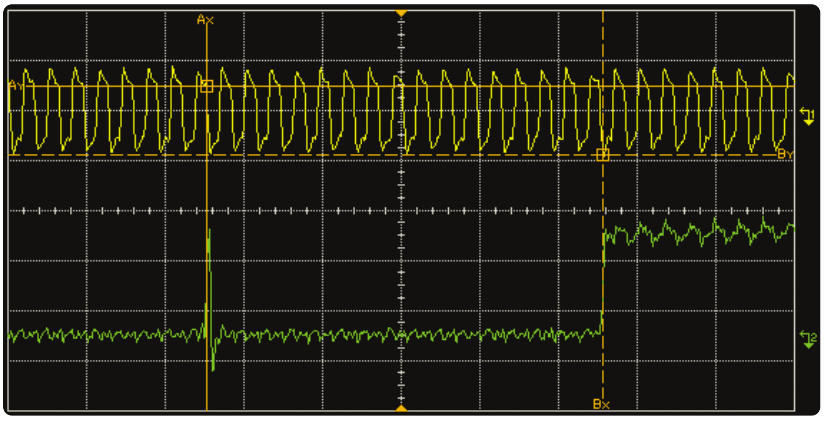


Figure 6b. Markers Ax and Bx in the oscilloscope display are locked to the same positions in time as the logic analyzer's global markers

Extended Logic-Centric Solution: Time Correlation Fixture (continued)

Use models

The dual instrument use model applies very well to high-end applications that need the full-feature, high performance logic synchronized to full-featured, high performance analog capabilities. Like the logic-centric scope module solution, it can be used to view the analog characteristics of a digital waveform or it can correlate signals between analog and digital components. In addition, because a full-featured DSO is being used, all of the traditional analog analysis capabilities are available to the user.

Strengths and limitations

The dual instrument solution's strength is that it combines full-featured instruments into a fully time-correlated, mixed-signal analysis solution and allows the user a much broader range of selections in terms of performance and capabilities for both the analog and digital analysis.

It does come with a few drawbacks. First, the time correlation is not as tight as the MSO and scope module solutions, whose acquisition hardware is built into the same instrument as the complementary analysis hardware. Second, setup is more time consuming and cumbersome and requires far more bench space than the single instrument solutions. Third, the triggering functionality is not across all digital and analog channels. In other words, you can either use the logic analyzer channels to trigger the scope or the scope channels to trigger the analyzer but not a combination, as in the MSO. Finally, the functionality is split between two separate and very different displays and software user interface environments with primary control in the logic analyzer. This is typically not a problem when used infrequently but can be cumbersome as an everyday solution.

While all of these solutions address a certain amount of common ground, some application problems are better met by the features and functionality of one solution as opposed to the others. The application examples that follow illustrate a specific debug problem and why one solution is best equipped to address it.

Embedded 32-Bit Processor and Wireless LAN

A classic example of a mixed-signal system is a wireless LAN application that is controlled by a 32-bit embedded processor. This application takes data from a wireless laptop, demodulates the signal down to baseband, and then converts the signal to a wireline signal on a LAN. Debugging a design like this requires the designer to view a variety of signals including the 802.11 baseband signal, the 10 Mp/s Ethernet signal, SDRAM, and the LAN control lines. With traditional equipment, triggering across all of these signals and viewing them in a time-correlated display can prove to be quite difficult. With an MSO, on the other hand, capturing and displaying all of the signals in a single acquisition is very easy and is illustrated in Figure 7.

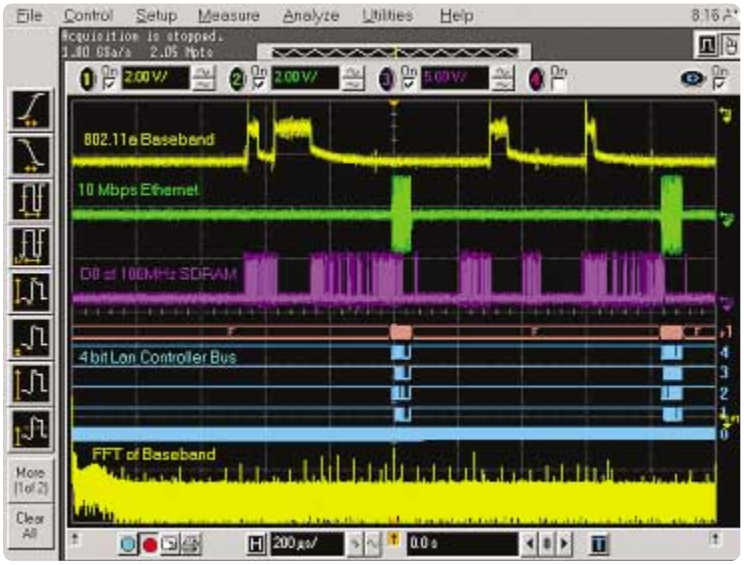


Figure 7. Mixed-signal acquisition of wireless LAN signals using an MSO

While verifying activity in this system, the designer sees noise spikes in the baseband signal's FFT. Since the system includes a high power line driver on the wireline side that is in close proximity to a sensitive RF receiver on the wireless side, it seems that unintended coupling is the source of the problem.

Further analysis into this problem can be conducted using the MSO's digital channels. Figure 8 shows the activity on the LAN as digital bus values. This bus is actually using four of the MSO's digital channels. In addition, this activity is correlated to activity on the baseband signal. The FFT of the baseband is also displayed. Noise spikes in the baseband can be seen on the FFT and correlated to specific data activity on the LAN.

This analysis allows the designer to focus in on possible root causes of the problem. While additional analysis of the frequency content using a spectrum analyzer might be necessary, the MSO has done a significant amount of work to narrow down the problem.

Advantages of an MSO solution

This example illustrates several powerful advantages of the MSO. First, the measurement requires traditional analog analysis in the form of an FFT, but it also requires more channels than a traditional DSO provides. Second, one cycle of the device under test takes more than 500 µs, so deep memory is necessary for capturing a trace of sufficient length. Finally, it is necessary to trigger on a specific value of the LAN controller and then correlate these digital signals to the analog representations of the baseband and Ethernet signal.

Alternatively, the extended logic-centric instrument solution could be used but would require significantly more time and effort to obtain the same result. The scope module in a logic analyzer is not a realistic option because it lacks the required functionality.

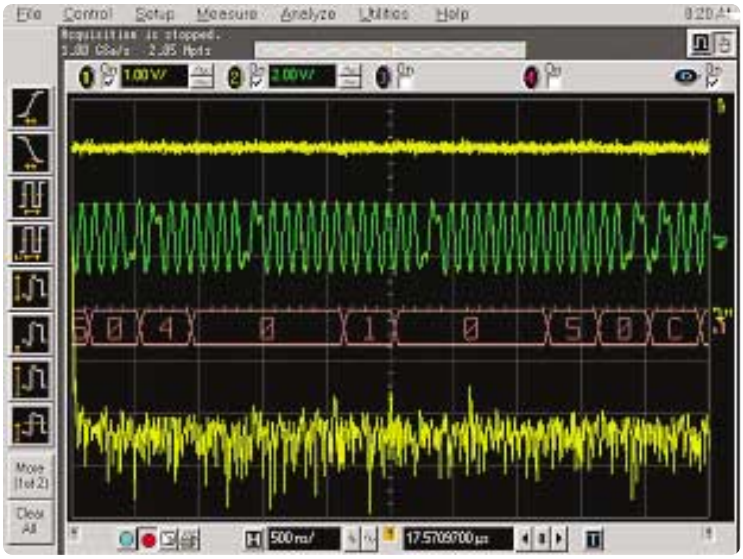


Figure 8. An MSO simultaneously displays the digital data on the LAN as well as the baseband signal and its FFT

Embedded Processor and D/A Converter

Mixed-signal analysis can be useful to trace anomalies in an analog waveform back to the behavior of software running on a system. An example of this is a small board with an MPC860 processor running at 66 MHz. The MPC860 executes firmware that controls the activity on the board, including a D/A converter that is periodically told by the software to output a triangle wave. During verification of the activity of the D/A, an oscilloscope reveals problems with the triangle waveform that include the flat distortion and stair step effects shown in Figure 9.

The source of this distortion is unknown. It could be a malfunction in the D/A component or it could be caused by other activity on the board. An oscilloscope module can be used to debug this problem. Channel 1 of the scope is connected to the output of the D/A converter. The scope is set to trigger when the triangle wave goes above 800 mV and stays there for longer than 1.2 ms. The scope module is also configured to cross trigger to the logic analyzer, which is running in state mode and monitoring the ADDR and DATA lines on the MPC860. This trigger will capture a waveform with maximum distortion and correlate it to the software activity on the processor.

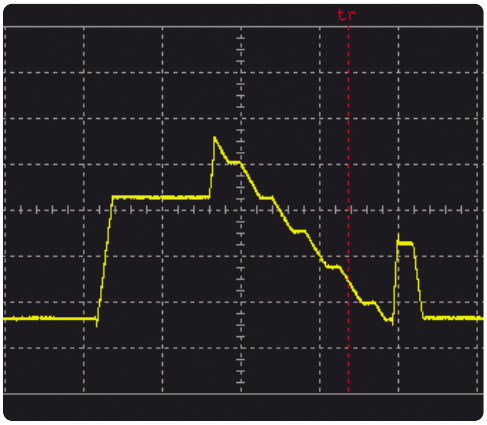


Figure 9. Distorted triangle waveform captured by the oscilloscope module

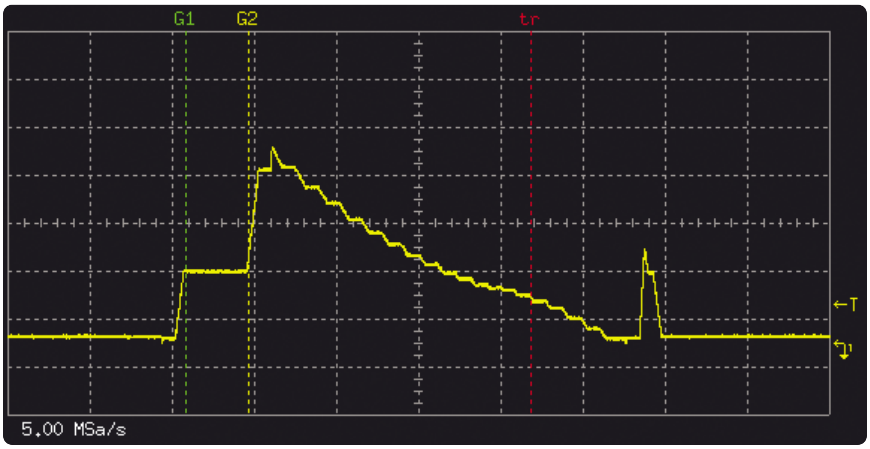


Figure 10. Beginning and end of the flat distortion marked in the oscilloscope module's display

Once the waveform is captured and viewed in the logic analyzer's oscilloscope display, the global markers are placed at the starting and ending points of the first flat distortion, as shown in Figure 10. Because the logic analyzer's global markers appear in all of its various displays, these same points will also be marked in the listing display.

The data correlation in the logic analyzer can be extended one step further to the source code level. Figure 11a shows the state listing display with the G1 marker indicating the state at which the flat distortion begins. By scrolling through the states shown in the listing display line by line between the G1 and G2 markers, the user can see the corresponding execution of source code.

The correlated source code view shown in Figure 11b indicates that the states prior to the G1 marker correspond to the execution of code that controls the D/A converter. At the state marked by G1, the source code jumps to a new routine called *ext_exception*. The source code viewer verifies that the code executing on the MPC860 is no longer the D/A control code but rather the interrupt service routine. By continuing to scroll through the listing the designer can also watch the source code step line by line through the service routine until it finally returns to the D/A control at the state marked by G2.

Since this problem is software and not hardware, it can be solved by changing the program to give priority to the D/A software over the interrupts. The same process can be used to identify the source of the remaining distortions, all of which are caused by similar interrupts.

Advantages of logic-centric solution with scope module

This example illustrates how a hardware problem can be isolated and traced back to software by using logic-centric, mixed-signal analysis. The scope-centric MSO solution could possibly achieve a similar result by triggering a break in the designer's debugger software. This requires a more extensive setup process and has potential correlation issues because the MSO does not acquire synchronous data. While the extended logic-centric solution could also accomplish similar tasks, it would have been much more labor intensive in terms of setup time.

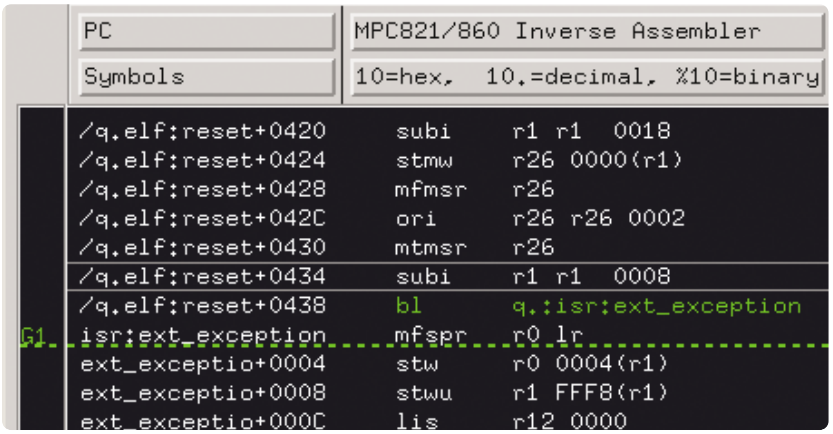


Figure 11a. State listing of bus activity around start of distortion (G1)

```
148      /* Stimulate the D/A Converter */
149      /* --------------------------- */
150      /* The D/A converters output voltage is 5 v
151      /* Create a triangle wave by ramping up the
152      /* at a time, then immediately ramping it d
153      /* ----------------------------------------
154      voltage = 0x0;
155      while (voltage < 0xf0)
156      {
157         *dac = voltage;          /* Vout = 5V(vo
158         voltage = voltage + 0x0a;
159      }
160
161      voltage = 0xff;
162      while (voltage > 0x08)
163      {
164         *dac = voltage;          /* Vout = 5V(vo
165         voltage = voltage - 0x02;
```

Figure 11b. Source code before distortion

```
53  void
54  ext_exception()  /* C Routine for Ext Interrupt
55  {
56     unsigned long exception;
57     unsigned short temp;
58
59     /* This is the C Routine to handle an extern
60     /* This function is called by the extern_lou
61     /* located in file 'exc_table.s'.
62     /* Note that other external interrupts are d
63     /* this routine.*/
64
65     exception = quicc->sivec;
66
```

Figure 11c. Source code when distortion begins (G1)

Application Examples (continued)

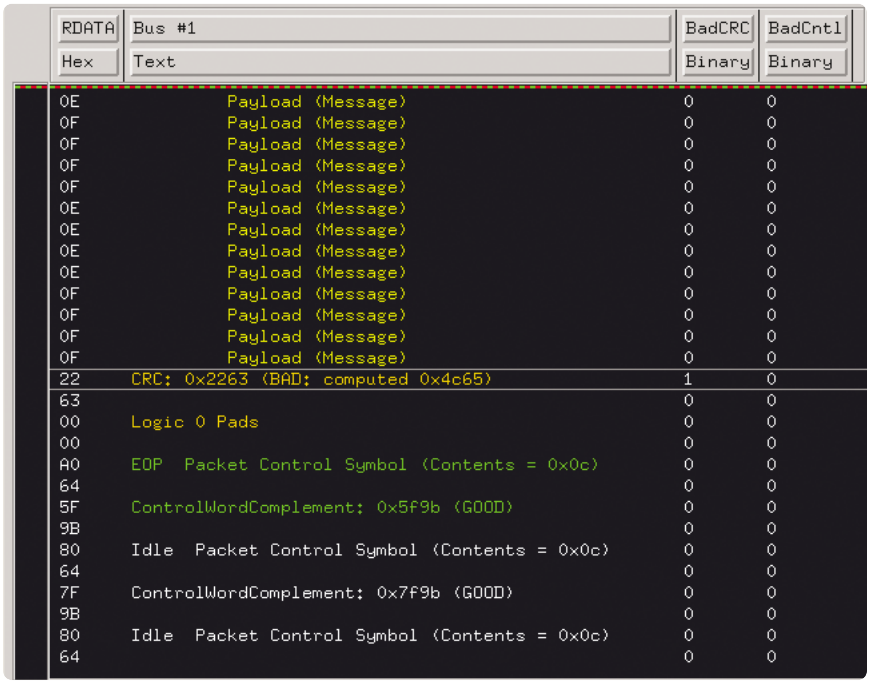
RapidIO

Signal integrity measurements for digital waveforms are a form of mixed-signal analysis that can often link the analog characteristics of signals to anomalies in the digital data.

The following example focuses on a board design that uses RapidIO to transfer data at 500 MT/s. An Agilent 16760A logic analyzer card and N4215A RapidIO analysis toolset are used to monitor the packets moving across the RapidIO bus. The RapidIO tool is able to decode the packet data and display the information in the analyzer's listing display, as shown in Figure 12.

In order to insure the integrity of the packet data, a CRC value is calculated based on the contents of the packet, and this value is embedded in the packet prior to transmission. When the packet is received at its intended destination, the CRC is re-calculated and compared to the initial CRC value. If the values are different, the packet data has been corrupted and the source of this corruption must be identified.

Figure 12 shows a packet that has generated a CRC error. Further investigation reveals additional but infrequent CRC errors occurring in other packets.



RDATA	Bus #1	BadCRC	BadCntl
Hex	Text	Binary	Binary
0E	Payload (Message)	0	0
0F	Payload (Message)	0	0
0F	Payload (Message)	0	0
0F	Payload (Message)	0	0
0F	Payload (Message)	0	0
0E	Payload (Message)	0	0
0E	Payload (Message)	0	0
0E	Payload (Message)	0	0
0E	Payload (Message)	0	0
0F	Payload (Message)	0	0
0F	Payload (Message)	0	0
0F	Payload (Message)	0	0
0F	Payload (Message)	0	0
22	CRC: 0x2263 (BAD; computed 0x4c65)	1	0
63		0	0
00	Logic 0 Pads	0	0
00		0	0
A0	EOP Packet Control Symbol (Contents = 0x0c)	0	0
64		0	0
5F	ControlWordComplement: 0x5f9b (GOOD)	0	0
9B		0	0
80	Idle Packet Control Symbol (Contents = 0x0c)	0	0
64		0	0
7F	ControlWordComplement: 0x7f9b (GOOD)	0	0
9B		0	0
80	Idle Packet Control Symbol (Contents = 0x0c)	0	0
64		0	0

Figure 12. RapidIO listing display showing a CRC error

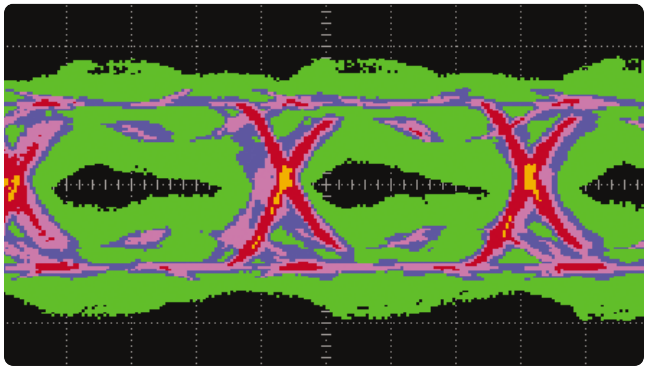


Figure 13a. Eye diagram of RapidIO bus

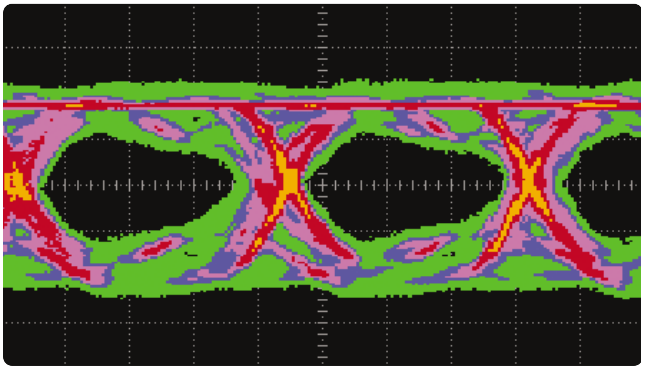


Figure 13b. Valid eye diagram for RapidIO data bit 0

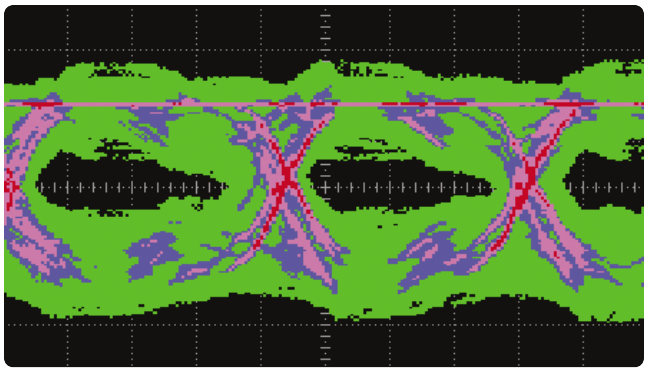


Figure 13c. Distorted eye on bit 3

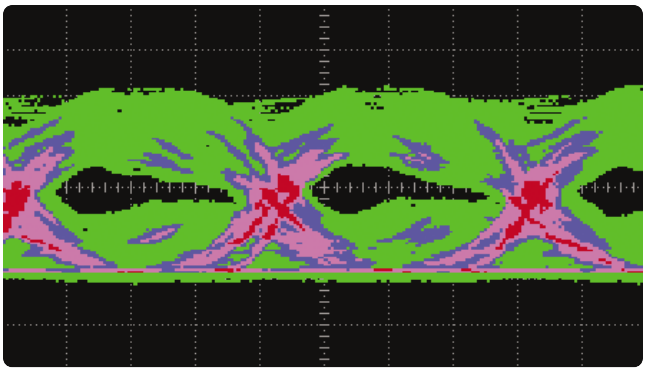


Figure 13d. Distorted eye on bit 6

The source of the data corruption is unknown, so the designer must figure out where to begin the debug process. Probing and evaluating various signal behaviors using traditional state analysis or an oscilloscope is inexact and potentially time consuming.

Alternatively, the designer is able to use the existing logic analyzer probes and the 16760A eye scan feature to quickly validate the analog signal integrity of all signals on the bus in a single measurement.

The composite eye diagram is shown in Figure 13a and it is immediately obvious that signal integrity issues are distorting the size and shape of the eye. In addition to the composite bus view, eye scan allows the designer to see each bit's eye diagram individually. Figure 13b shows the eye associated with bit-0 of the RapidIO data bus, and it is a valid eye opening. Scrolling through the remaining signals identifies bits 3 and 6, as shown in Figures 13c and 13d, as the two problematic signals from a signal integrity standpoint.

At this point eye scan has successfully isolated a problem on the board, but is it the problem causing the CRC errors? The color grading of the eye diagrams provides additional clues. The areas colored green are low incident events. At worst, the transitions happening in these areas occur approximately 15,625 times per million clocks and probably far less than that. In other words, these are very infrequent events, just like the CRC errors that show up in the decoded packets. Designers must take additional debug steps to identify the root cause of this problem using other tools at their disposal. The RapidIO tool and eye scan have taken them a long way in this process by quickly isolating a potential source of the problem.

In the end, it is determined that two BGA vias, the negative leg of the bit-3s differential pair and the positive leg of the bit-6s differential pair, are coupling because of a bad solder connection. Because these signals are differential, this coupling does not cause a problem all of the time and actually requires a very specific circumstance for it to occur. The bit errors only occur when both signals are simultaneously switching in the same direction. In all other cases, the appropriate data values still are transmitted and received, so valid data is seen most of the time.

Advantages of logic-centric solution with scope module and eye scan

Without the tools and approach described in this application, the problem would have been difficult to detect and may have been easily missed. Since a logic analyzer is the only instrument that provides both the acquisition speeds to acquire 500 MT/s data synchronously and a tool that decodes the RapidIO packets, this problem requires a logic-centric solution to initially identify and isolate the problem.

While the MSO is able to display eye diagrams, it does not have the necessary bandwidth to accurately perform the measurement. In order to sample the 500 MT/s data rate accurately, the scope's bandwidth would have to be approximately 2 GHz. If the necessary bandwidth were available in an MSO, it would take many measurements accumulating data over a much longer period to see the problem shown by eye scan. In addition, the MSO is not able to make the necessary state mode measurement with decoded packetized data that is initially required to indicate a problem exists.

USB2.0

It is often necessary to view the analog characteristics of a digital signal to validate that it is functioning correctly and is operating within the defined margins. An application using USB2.0 at high speeds creates an environment that makes this task a little more challenging. In this example, an external CD-RW is using USB2.0 to move data between itself and a PC at 480 Mb/s. Simply probing the USB signal with a scope is not a difficult task, but as soon as designers want to pin-point a location in the data stream they are faced with a much more challenging task. The desired measurement tasks can be achieved using the dual instrument solution.

Because USB transmits data packets in 8-bit bytes, a logic analyzer can be used to trigger on specific events. In this example, the designer needs to locate the beginning of a data sequence so the Start of Frame (SOF) Packet ID (PID) will be the trigger event. To make this possible, a FuturePlus FS4120 USB2.0 analysis probe (Agilent part number: FSI-60050) is used to de-serialize the USB data and to provide probing points for the scope and the logic analyzer. A 2.25 GHz Agilent 54846B oscilloscope and 1157A active probe are used to probe the USB signal. A 16750A logic analyzer probes the PID signals and others on the analysis probe. For this setup to work, one more piece is needed. The Agilent E5850A time correlation fixture connects the logic analyzer to the oscilloscope so that time-correlated cross triggering is possible.

In this example, the designer must identify the start of a frame and then verify various analog characteristics of the USB signal at that point. The logic analyzer isolates the desired location in the data by triggering on the SOF event. When the analyzer triggers, it will also cross trigger the oscilloscope so that its trigger point is also at the SOF event.

Figure 14 shows the logic analyzer triggered at the SOF point. The channel 1 waveform at the top of the screen is the time-correlated USB signal that has been imported into the display from the oscilloscope. Figure 15 shows the oscilloscope display with its trigger position also located at the SOF event.

The designer now knows the desired starting point for the analysis and can continue with the validation process using any of the analog measurements available on the oscilloscope.

Advantages of extended logic-centric solution

This example clearly requires mixed signal analysis capabilities to allow for the appropriate trigger qualification. The dual instrument solution is the only viable option because the problem requires the acquisition of state mode data and FuturePlus's packet decoder on the logic analyzer side and at least 2 GHz of bandwidth on the oscilloscope side. These requirements can only be met by high-end, stand-alone instruments.

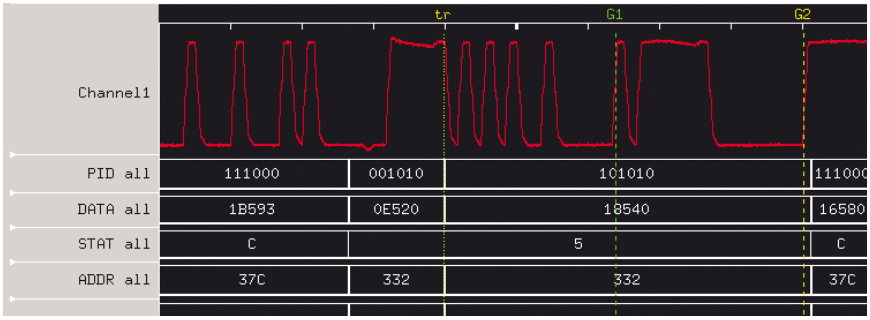


Figure 14. Logic analyzer waveform triggered at the Start of Frame (SOF)

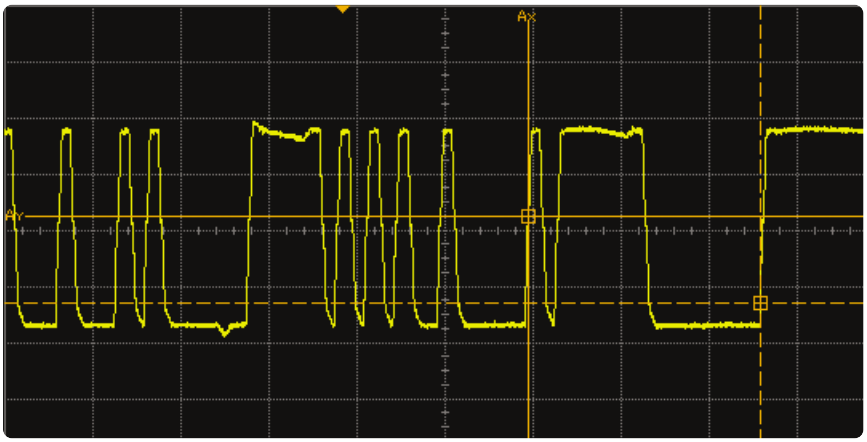


Figure 15. Oscilloscope display correlated to logic analyzer with same trigger point at the SOF

Summary

The similarities and differences as well as the strengths and weaknesses of each mixed-signal analysis solution should now be a little clearer. It is certainly true that there are significant overlaps between the capabilities and potential uses for each solution. Selecting an appropriate solution to meet a designer's needs boils down to some simple decisions. First is matching the speeds of the signals to be analyzed to the performance specifications of the instruments. Table 1 shows some basic guidelines for how particular data rates match up to solutions. As data rates increase, the choice of solutions decreases.

The second step is to evaluate the desired functionality for analyzing data. Table 2 rates each solution in terms of various features and functions. In addition to the first two steps, there is an intangible decision based on user preferences. Individual designers often prefer, or are more comfortable with, one instrument over another. If multiple solutions meet a designer's needs, then these preferences must be strongly considered when determining the appropriate solution. It is certain that the Agilent family of mixed-signal solutions is broad and deep enough to address a large variety of needs.

Mixed analysis solution	Data rate (MTransfers/second)	Example applications
Scope module (logic-centric)	≤ 100 MT/s	JTAG, MPC860, FPGA
MSO (scope-centric)	≤ 250 MT/s	ARM, FPGA
Dual instrument time-correlation (extended logic-centric)	≤ 500 MT/s	DDR, USB 2.0
Eye scan (logic-centric)	200 - 1500 MT/s	RapidIO, SPI4.2

Table 1. Data rate and solution comparison

	Scope-centric	Logic-centric	Extended logic-centric
Time-correlated data	A	A	B
Integrated analog and digital displays	A	B	B
Full width triggering	A	B	B
Complex sequential triggering	B	A	A
Data deskew	A	A	B
Analog analysis functions	A	C	A
Digital analysis functions	C	A	A
State analysis acquisition	N/A	A	A
Eye scan analysis	N/A	A	A
Eye diagram measurements	B	C	A
Fast display update rate	A	C	C**
Ease of use	A	B	C

Table 2. Comparison of functionality (A = Excellent, B = Good, C = Fair, N/A = Not Available)

** The extended logic-centric solution is limited to single shot acquisitions.

Glossary

Glossary

Asynchronous acquisition (timing mode) Acquisition of samples from a device under test at regular intervals defined by the logic analyzer's internal sample rate. Also known as timing mode.

BGA – Ball Grid Array

CRC Cyclic Redundancy Check

Deskew – To cancel or nullify the effects of differences between two different internal delay paths for a signal. Deskewing is done so that both instruments recognize the signal at the same time and the sample points can be time-correlated.

DSO – Digital Storage Oscilloscope

DSP – Digital Signal Processor

Eye Diagram – Constructed by overlaying plots of the waveform from successive unit time intervals; Provides a comprehensive overview of signal integrity effects including jitter, noise, reflections, ringing, power and ground coupling, and inter-symbol interference.

FFT – Fast Fourier Transform; an algorithm used to transform time domain data to frequency domain data.

LAN – Local Area Network

MSO – Mixed Signal Oscilloscope

State Analysis –When the logic analyzer acquires samples from the device under test synchronously, in other words, when a signal or signals from the device under test indicates when to acquire a sample. Typically, the signal used to set up the sampling is a state machine clock signal or microprocessor clock signal. Also known as synchronous sampling.

Synchronous Acquisition – When the logic analyzer acquires samples from the device under test synchronously, in other words, when a signal or signals from the device under test indicates when to acquire a sample. Typically, the signal used to set up the sampling is a state machine clock signal or microprocessor clock signal. Also known as state mode.

Time-correlation – aligning signals in time so that a sample point on one signal can be correlated to the sample point on another signal that happened at the same position in time.

Trigger – The event about which acquired data is stored; in other words, the event that you are looking for. For example, you may want to trigger on an edge in order to see the events that lead up to it and the events that happen after it. The event that triggers the instrument becomes a reference point in the data display.

Related Literature

Related Literature

Publication Title	Publication Type	Publication Number
8 Hints For Solving Common Debugging Problems With Your Logic Analyzer Application Note 1326	Application Note	5968-5700E
Saving Time with Multiple-channel Signal Integrity Measurements Application Note 1382-8	Application Note	5988-5409EN
Feeling Comfortable with Logic Analyzers Application Note 1337	Application Note	968-8291E
8 more Hints for Making Better Scope Measurements	Application Note	5968-8756E
8 Hints for Debugging Microcontroller-based Designs	Application Note	5980-0943EN
Mixed Analog and Digital Signal Debug and Analysis using a Mixed Signal Oscilloscope Wireless LAN Example Application Application Note 1418	Application Note	5988-7746EN

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