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CRITICAL CONDUCTION MODE, FLYBACK SWITCHING POWER SUPPLY USING THE MC33364

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1 INTRODUCTION

This application note presents a way of designing an AC-DC flyback converter that is operating in the critical conduction current mode, using the MC33364. The first section describes the main differences of operation between fixed frequency and critical conduction current mode flyback converters. The second section describes the design of a typical converter, including the design of the transformer.

2 FLYBACK CONVERTER OPERATION SUMMARY

2.1 Fixed Frequency Current-mode Flyback Converters

The block diagram of a fixed frequency current mode controlled flyback converter can be seen in Figure 2-1. Here a fixed frequency oscillator initiates a power switch conduction period. This is terminated by either the current within the power switch reaching a predetermined limit (as set by the error amplifier) or the oscillator terminating the period (and initiating the next power switch conduction period).

2.1.1 Operation

A simplified flyback converter can be seen in Figure 2-2. The power switch (Q) essentially places the primary inductance of the flyback transformer (T) across the input voltage source when it is turned on. The secondary is disconnected because the output rectifier (D) is reverse biased. The voltage drop (monitored by the control IC) on the current sense resistor grows with the primary current. When the primary current (voltage drop) reaches a predetermined value the power switch (Q) is turned off by the IC. In accordance with Lenze's law, the transformer reverses the direction of the voltage on the windings because it has saved some energy and wants to keep the same current flowing as existed before the switch was turned off. Now the output rectifier is forward biased and conducts the secondary current. The output capacitor (C) is charged by that secondary current, which decreases as the energy saved within the transformer decreases.

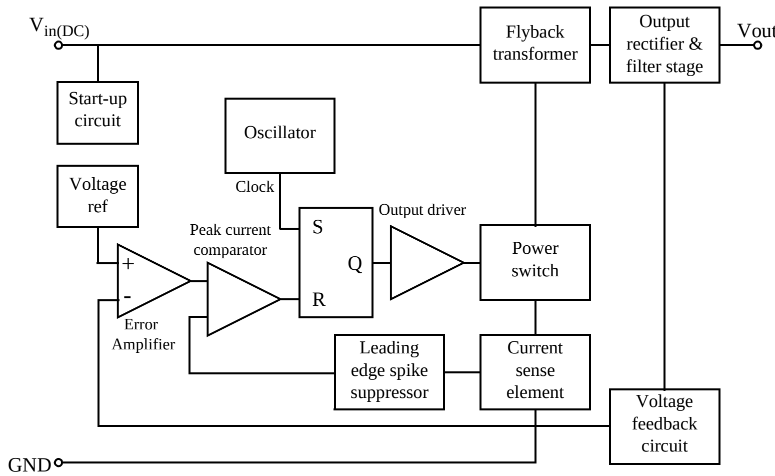


Figure 2-1. Block Diagram of a Fixed Frequency Current-mode Flyback Converter

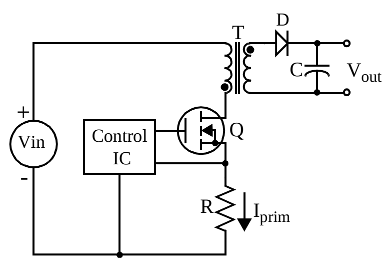


Figure 2-2. A Simplified Schematic of a Flyback Converter

2.1.2 Primary circuit consideration

The primary winding's current takes the form of a linear ramp starting from zero amps and whose peak value ippk is given by:

$$i_{ppk} = \frac{V_{in} \cdot t_{on}}{L_p}$$

V_{in} ... input DC voltage
t_{on} ... on-time
L_p ... primary inductance

The slope of the current ramp is V_{in}/L_p.

The flyback topology, as with all boost-mode converters, operates under the principle of storing energy within the core material of the transformer. The energy stored during each conduction period is given by:

$$E = \frac{1}{2} \cdot L_p \cdot i^2{}_{ppk}$$

Then the output power is given by:

$$P_{out} = \frac{1}{2} \cdot L_p \cdot i^2{}_{ppk} \cdot f_{op}$$

f_{op} ... operating frequency

2.1.3 Secondary circuit consideration

The secondary winding's current takes the form of a linearly decreasing ramp starting from peak value ispk that is given by:

$$i_{spk} = i_{ppk} \cdot \frac{n_p}{n_s}$$

n_p,n_s ... number of primary and secondary turns

The core discharge time during the switch (Q) off time is given by:

$$t_{dis} = \frac{L_s \cdot i_{spk}}{V_s}$$

L_S .... secondary inductance
i_{spk} .. secondary current
V_S .... secondary voltage

2.1.4 Overload condition

When the power supply is overloaded the output voltage V_S goes down and L_S*i_S is a constant. For such conditions the core discharge time will be longer than what was calculated for nominal output voltage. The function of the control IC oscillator does not depend on the magnetization of the transformer core, so therefore it will start the next cycle even if the core was not totally demagnetized.

The primary current ramp of the next cycle does not start from zero but from some value which is determined by the remaining energy in the transformer's core. Such type of operation is known as the "Continuous mode", which is mainly not acceptable due to power losses on the output rectifier. For these reasons one should add some protection circuit to guard against core demagnetization and this leads to the design of a critical conduction mode converter, which is described in the next section.

2.1.5 Fixed frequency current mode design recommendations

The power supply should be designed for the worst case of operating conditions. These conditions occur at the lowest input voltage and the maximum output power for a given operating frequency. At these conditions, the power supply would work in the range between discontinuous mode and continuous mode of operation, this operating region is known as the "Critical conduction mode". It means that there will be no dead time in the switch-off time of the switching period. For higher input voltage or lower output power the power supply will operate in the discontinuous mode and there will be a dead time in the switch-off time.

2.2 Critical conduction Current mode Flyback Converters

The block diagram of a critical conduction current mode controlled flyback converter can be seen in Figure 2-3.

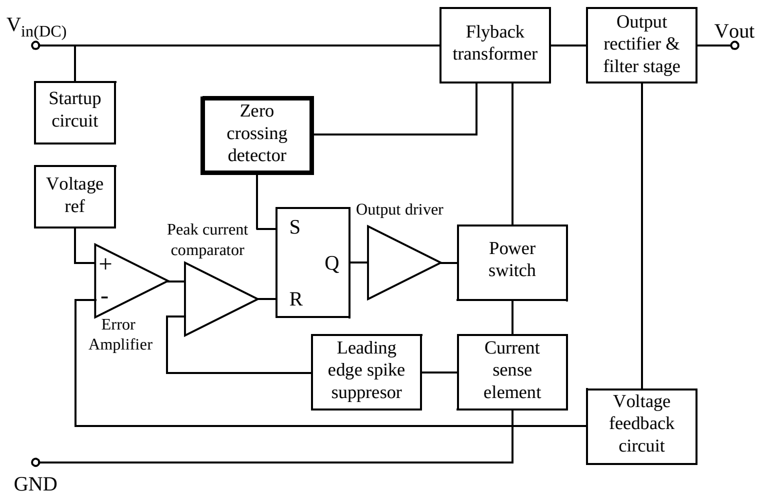


Figure 2-3. Block Diagram of a Critical Conduction Current-mode Flyback Converter

The major difference between this and a fixed frequency current flyback converter is the zero crossing detector block.

The critical conduction mode of operation is when the flyback circuit has little or no dead time in the switch-off time. When the transformer or the coupled inductor has released all of the stored energy, the next power cycle can start.

One question might be: How does the transformer or circuit know that all energy has been released? As long as there is some energy in the transformer there is a voltage across the secondary winding. If all of the available energy has been released to the secondary load then the voltage across the switch oscillates around the input voltage due to the rest of energy in the parasitic capacitances (in the switch, primary winding and on the PC board).

The voltage on the primary winding itself oscillates around the zero. The frequency of the oscillation is given by:

$$f_{toff} = \frac{1}{2 \cdot \pi \cdot \sqrt{L_p \cdot C_{par}}}$$

L_p ... primary inductance
C_{par} .. parasitic capacitances

The initial amplitude of oscillation on the primary winding during that time is given by:

$$V_{init} = V_s \cdot \frac{n_p}{n_s}$$

V_s ... secondary voltage
n_p ... number of turns on the primary side
n_s ... number of turns on the secondary side

Something similar happens on the secondary and auxiliary windings. The only difference is in the level of voltage (given by the turns ratio). The auxiliary winding is used for zero crossing detection and for supplying the IC. If the voltage across the auxiliary winding approaches zero, then the latch within the IC is set and the power cycle starts again.

2.2.1 Advantage of critical conduction mode

The advantage of the critical conduction mode is that the peak current is lower than in the fixed frequency mode of operation for the same power. The reason is that the average current is identical in both cases but the fixed frequency has a dead time while the critical conduction has no dead time. The lower peak current leads to lower power dissipation in many cases. The critical conduction mode power supply is also self-protected in case of the short circuit on the output, without large current stress on the output rectifier as happens with the fixed frequency current mode of operation.

3 CRITICAL CONDUCTION MODE FLYBACK CONVERTER EXAMPLE

The described critical conduction mode flyback converter has the following performance and maximum ratings:

Output power	12W
Output	12V @ 1Amp max
Input voltage range	90VAC - 270VAC

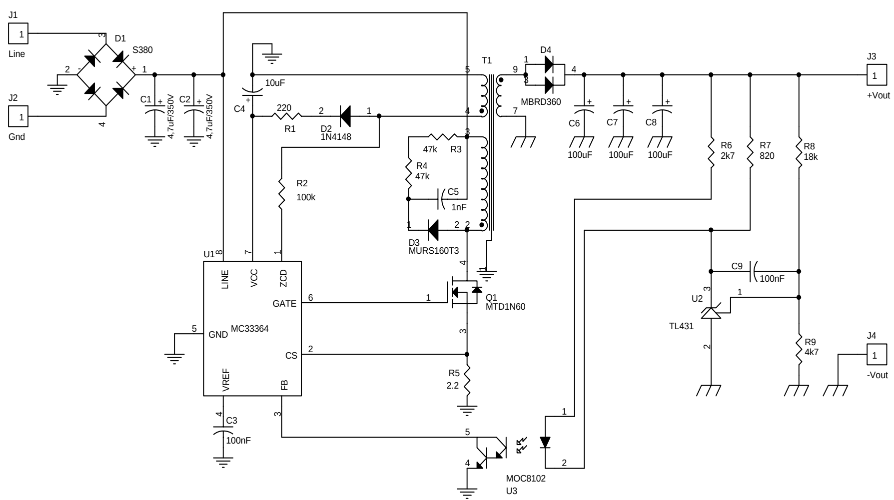


Figure 3-1. The Critical Conduction Mode Flyback Converter Schematic

3.1 Circuit operation

The circuit operation is as follows: the rectifier bridge D1 and the capacitors C1,C2 convert the AC line voltage to DC. This voltage supplies the primary winding of the transformer T1 and start-up block in U1 through pin 8. The primary current loop is closed by the transformer's primary winding, the TMOS switch Q1 and the current sense resistor R5. The resistors R3,R4, diode D3 and capacitor C5 create a clamping network that protects Q1 from spikes on the primary winding. The network consisting of capacitor C4, diode D2 and resistor R1 prepares a Vcc supply voltage for U1 from the auxiliary winding of the transformer. The resistor R1 makes Vcc more stable and resistant to noise. The resistor R2 reduces the current flow through the internal clamping and protection zener diode of the zero crossing detector (ZCD, pin1) within U1. C3 is the decoupling capacitor of the reference voltage. The diode D4 and the capacitors C6, C7 and C8 rectify and filter the output voltage. The device U2 drives the primary side through the optoisolator to make the output voltage stable. The output voltage information is delivered to U2 by a resistor divider that consists of resistors R8 and R9. The capacitor C9 provides frequency compensation of the feedback loop. The resistor R6 limits the current flowing through the LED diode and U2. The resistor R7 supplies U2 for its proper operation when the power supply fully loaded (the LED current is zero).

Designator	Quantity	Value/Rating	Description
C1, C2	2	4.7µF/450V	Capacitor, Electrolytic
C3	1	100nF	Capacitor, Ceramic (SMD)
C4	1	10µF/25V	Capacitor, Electrolytic
C5	1	1nF/1kV	Capacitor, Ceramic
C6, C7, C8	3	100µF/50V	Capacitor, Electrolytic
C9	1	100nF	Capacitor, Ceramic (SMD)
D1	1	S380	Rectifier bridge, 380VAC,0.8A (SMD)
D2	1	1N4148	Diode (SMD)
D3	1	MURS160T3	Ultrafast Diode, 1A, 600V (SMD)
D4	1	MBRD360	Schottky diode (SMD)
J1, J2, J3, J4	4		Connector
Q1	1	MTD1N60	MOSFET 1A, 600V (SMD)
R1	1	220Ω, 1/4W	Resistor(SMD)
R2	1	100kΩ, 1/4W	Resistor (SMD)
R3, R4	2	47kΩ, 1/4W	Resistor (SMD)
R5	1	2.2Ω, 1/4W	Resistor (SMD)
R6	1	2.7kΩ, 1/4W	Resistor (SMD)
R7	1	820Ω, 1/4W	Resistor (SMD)
R8	1	18kΩ, 1/4W	Resistor (SMD)
R9	1	4.7kΩ, 1/4W	Resistor (SMD)
T1	1		Transformer (see text)
U1	1	MC33364	Integrated circuit
U2	1	TL431	Integrated circuit
U3	1	MOC8102	Optoisolator

Table 3-1. Parts List

3.1.1 Frequency clamp block of MC33364

The basic function of this converter is described in the theoretical section of this application note. The operation of the Motorola's control IC MC33364 follows this description, with one exception. Since the critical conduction mode converter is a variable frequency system, the MC33364 has a built-in special block to reduce switching frequency in the no-load condition. This block is named the "frequency clamp" block. The MC33364 used in this example has the frequency clamping internally set to 126kHz, however, some parts with a disabled or variable frequency clamp are available. The frequency clamp works as follows: the clamp controls the part of the switching cycle when the primary switch is turned off. If this "off-time" (determined by the demagnetization of the transformer's core) is too short then the frequency clamp block does not allow the switch to turn-on again until the defined frequency clamp time is reached (i.e., the frequency clamp block will insert some dead time).

3.1.2 Start-up block of MC33364

The advantages of the MC33364's start-up circuit need to be described in more details. The start-up circuit includes a special high voltage switch that controls the path between the rectified line voltage and the V_{cc} supply capacitor to charge that capacitor by a determined current when the power supply is first connected to the line. After V_{cc} reaches a certain value, the start-up switch is turned off by the undervoltage and the overvoltage control circuit. Also the temperature is monitored because, during the start-up time, there is a large power dissipation within the start-up switch. After a few primary switching cycles the IC is supplied from auxiliary winding. Because the power supply output can be shorted and the auxiliary voltage will fall down at this time, the MC33364 will periodically start its start-up block. This mode is named "hiccup mode". During this mode the temperature of the chip rises but remains protected by the thermal shutdown block. The main advantage of the start-up block is that during the power supply's normal operation, it does not consume any power.

3.2 Predesign Considerations

DC input voltages:

$$V_{in(min)DC} = \sqrt{2} \cdot V_{in(min)AC} = \sqrt{2}(90\text{VAC}) = 127\text{VDC}$$

$$V_{in(max)DC} = \sqrt{2} \cdot V_{in(max)AC} = \sqrt{2}(270\text{VAC}) = 382\text{VDC}$$

Maximum input average current:

$$I_{in-av(max)} = \frac{P_{out}}{\eta \cdot V_{in(min)}} = \frac{(12\text{W})}{0{,}8(127\text{V})} = 0{,}118\text{A}$$

η.. efficiency

A TMOS switch with 600V avalanche breakdown voltage is used. The voltage on the switch's drain consists of the input voltage and the flyback voltage of the transformer's primary winding. There is a ringing on the rising edge's top of the flyback voltage due to the leakage inductance of the transformer. This ringing looks like damped oscillations. The initial amplitude of that oscillation is given by the energy saved in the leakage inductance (i.e., by the value of the leakage inductance and the primary peak current). This ringing is clamped by the RCD network. The first half-sine wave of the ringing is most dangerous even if clamped. This clamped wave has an amplitude of 50V, so one has to add this value to the total voltage across the switch. One also has to add another 50V to secure the switch's reliability.

After this approach we can calculate the suitable value of the flyback voltage:

$$V_{flbk} = V_{TMOS} - V_{in(max)} - 100\text{V} = 600\text{V} - 382\text{V} - 100\text{V} = 118\text{V}$$

Since this value is very close to the $V_{in(min)}$, it was decided for easier further calculations to make them equal:

$$V_{flbk} = V_{in(min)} = 127\text{V}$$

The V_{flbk} value of the duty cycle is given by:

$$\delta_{max} = \frac{V_{flbk}}{V_{flbk} + V_{in(min)}} = \frac{(127\text{V})}{(127\text{V}) + (127\text{V})} = 0{,}5$$

The maximum input primary peak current:

$$I_{ppk} = \frac{2 \cdot I_{in-av(max)}}{\delta_{max}} = \frac{2(0{,}118\text{A})}{0{,}5} = 0{,}472\text{A}$$

The desired minimum frequency f_{min} of operation is 70 kHz.

3.3 Designing the transformer

After reviewing the core sizing informations provided by the core manufacturer it was decided to use an EE core of size about 20 mm. A Siemens N67 magnetic material is used, which corresponds to a Philips 3C85 or TDK PC40 material.

The primary inductance value is given by:

$$L_p = \frac{\delta_{max} \cdot V_{in(min)}}{I_{ppk} \cdot f_{min}} = \frac{0{,}5(127\text{V})}{(0{,}472\text{A})(70\times10^3\text{Hz})} = 1{,}92\text{mH}$$

The manufacturer recommends for that magnetic core a maximum operating flux density of:

B_{max} = 0.2 T

The cross-sectional area A_C of the EF20 core is:

A_c = 33.5 mm^2

The operating flux density is given by:

$$B_{max} = \frac{L_p \cdot I_{ppk}}{n_p \cdot A_c}$$

From this equation one can obtain the equation for the number of turns of the primary winding:

$$n_p = \frac{L_p \cdot I_{ppk}}{B_{max} \cdot A_c}$$

The A_L factor (defines how many turns is needed for a given inductance) is determined by:

$$A_L = \frac{L_p}{n^2_p} = \frac{L_p \cdot (B_{max} \cdot A_c)^2}{(L_p \cdot I_{ppk})^2} = \frac{(B_{max} \cdot A_c)^2}{L_p \cdot I^2_{ppk}} = \frac{((0{,}2\mathrm{T})(33{,}5\times10^{-6}\mathrm{m}^2))^2}{(1{,}92\times10^{-3}\mathrm{H})(0{,}472\mathrm{A})^2} = 105\mathrm{nH}$$

From the manufacturer's catalogue recommendation, the core with an A_L of 100nH is selected. The desired number of turns of the primary winding is:

$$n_p = \sqrt{\frac{L_p}{A_L}} = \sqrt{\frac{1{,}92\times10^{-3}\mathrm{H}}{100\times10^{-9}\mathrm{H}}} = 139\mathrm{turns}$$

If only the same magnetic core with a higher A_L is available, one has to increase the minimum frequency and calculate its value:

$$f_{min} = \frac{\delta_{max} \cdot V_{in(min)} \cdot A_L \cdot I_{ppk}}{(B_{max} \cdot A_c)^2}$$

and then to determine the value of the primary inductance and its number of turns again. If the minimum operating frequency is too high and the value of the A_L is too low, then one has to increase the size of the core.

The number of turns needed by the +12V secondary is (assuming an ultrafast rectifier is used):

$$n_s = \frac{(V_s + V_{fwd}) \cdot (1 - \delta_{max}) \cdot n_p}{\delta_{max} \cdot V_{in(min)}} = \frac{(12\mathrm{V} + 0{,}7\mathrm{V})(1 - 0{,}5)139}{0{,}5(127\mathrm{V})} = 14\mathrm{turns}$$

The auxiliary winding to power the control IC is +16V and its number of turns is given by:

$$n_{aux} = \frac{(V_{aux} + V_{fwd}) \cdot (1 - \delta_{max}) \cdot n_p}{\delta_{max} \cdot V_{in(min)}} = \frac{(16\mathrm{V} + 0{,}9\mathrm{V})(1 - 0{,}5)139}{0{,}5(127\mathrm{V})} = 19\mathrm{turns}$$

3.4 The Bulk Input Filter Capacitor

The approximate value of capacitance needed is:

$$C_{in} = \frac{t_{off} \cdot I_{in-av(max)}}{V_{ripple}} = \frac{(5\times10^{-3}\mathrm{s})(0{,}118\mathrm{A})}{(50\mathrm{V})} = 11{,}8\mu\mathrm{F} = 10\mu\mathrm{F}$$

3.5 Sizing the Output Filter Capacitor

Because we have a variable frequency system, all the calculations for the value of the output filter capacitors will be done at the lowest frequency, since the ripple voltage will be greatest at this frequency. The approximate equation for the output capacitance value is given by:

$$C_{out} = \frac{I_{out(max)}}{f_{min} \cdot V_{rip(max)}} = \frac{(2\mathrm{A})}{(70\times10^3\mathrm{Hz})(0{,}1\mathrm{V})} = 286\mu\mathrm{F}$$

Make three output capacitors 100µF connected in parallel or one capacitor 330µF. The parallel combination is the better choice because it has lower parasitic inductance and resistance (the total parasitic inductance or resistance is given by the parallel combination of each capacitor's parasitic inductance or resistance) which can significantly decrease the output ripple voltage. Also capacitors designed for higher voltage tend to have a lower parasitic inductance and resistance, so use the highest rating possible.

3.6 The Current Sense Resistor

There is an internal network between the primary IC's voltage feedback pin and its internal PWM comparator. This network is depicted in figure 3-2 in more detail. The most important voltage is V_{inv} on the PWM comparator's inverting input. If no external bias resistor from reference voltage to feedback pin is connected then V_{inv} is roughly in the range of 0.075V to 1.15V. The1.15V level is achieved is at the power supply maximum output power.

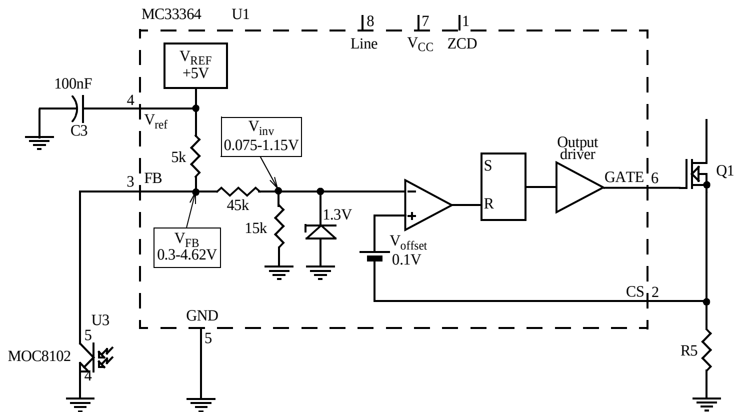


Figure 3-2. Primary Side Voltage Feedback Loop

There is also an internal offset voltage V_{offset} connected between the current sense input pin and the PWM comparator's noninverting input with a typical value of 0.1V.

Then the peak voltage drop on the current sense resistor is given by:

$$V_{cs} = V_{inv(max)} - V_{offset} = 1{,}15V - 0{,}1V = 1{,}05V$$

The design of the current sense resistor (R5) is simply given by:

$$R_5 = \frac{V_{cs}}{I_{ppk}} = \frac{(1{,}05\text{V})}{(0{,}472\text{A})} = 2{,}22\Omega = 2{,}2\Omega$$

3.7 Designing the Voltage Feedback Loop

The error amplifier function is provided by a TL431 on the secondary, connected to the primary side via an optoisolator, the MOC8102.

The voltage of the optoisolator collector node sets the peak current flowing through the power switch during each cycle. This pin will be connected to the feedback pin of the MC33364.

Starting on the secondary side of the power supply, assign the sense current through the voltage-sensing resistor divider to be approximately 0.5mA. One can immediately calculate the value of the lower and upper resistor:

$$R_9 = \frac{V_{ref(TL431)}}{I_{div}} = \frac{2{,}5\text{V}}{0{,}5\times10^{-3}\text{A}} = 5\text{k}\Omega = 4{,}7\text{k}\Omega$$

$$R_8 = R_9\left(\frac{V_{out}}{V_{ref(TL431)}} - 1\right) = 4{,}7\text{k}\Omega\left(\frac{12V}{2{,}5V} - 1\right) = 17860\Omega = 18\text{k}\Omega$$

Since a resistor of 5kΩ is internally connected from the reference voltage +5V to the feedback pin of the MC33364, a current of 1mA will be drawn from the transistor within the MOC8102. The MOC8102 has a typical current transfer ratio C_{trr} of 100% (with 25% tolerance) at a LED current of 10mA. For the phototransistor current of 1mA the LED requires a current of 2mA, because at these conditions the MOC8102 has C_{trr} of 50%. A LED current of 3mA will be suitable a value for further calculation of bias resistor R6:

$$R_6 = \frac{(V_{out} - (V_{ref(TL431)} + V_{LED}))}{I_{LED}} = \frac{(12\text{V} - (2{,}5\text{V} + 1{,}4\text{V}))}{3\times10^{-3}\text{A}} = 2{,}7\text{k}\Omega$$

The resistor R7 has a very important function, as mentioned in the circuit operation description. If it is not present, then the power supply output voltage falls down with increasing load sooner than expected. The reason is the following: When the power supply is fully loaded (nominal output power at minimal input voltage), the LED current (and also phototransistor current) is zero. But the voltage regulator U2 requires a cathode current of at least 1mA for proper operation of its internal voltage reference. If the cathode current is smaller then the reference voltage decreases and consequently the power supply output voltage decreases and it degrades the power supply output characteristic. A cathode current of 1.5mA will be adequate. The resistor R7 biases this cathode current and its value is given by:

$$R_7 = \frac{V_{LED}}{I_{TL431}} = \frac{1{,}4V}{1{,}5 \times 10^{-3}\mathrm{A}} = 933\Omega = 820\Omega$$

This completes the design of the uncompensated voltage feedback circuit.

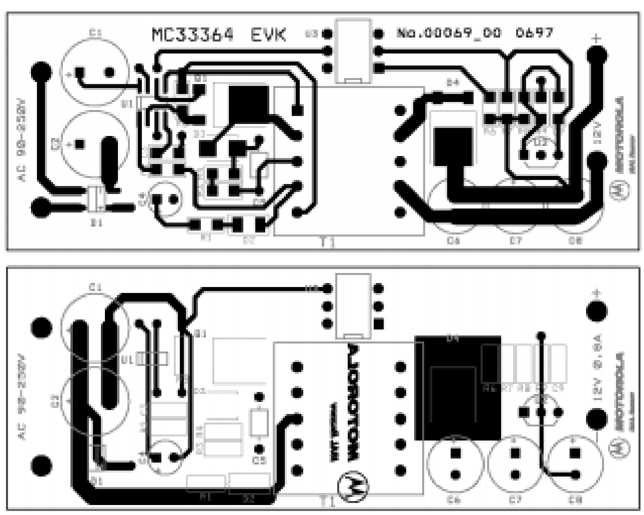
3.8 Designing the Voltage Feedback Loop Compensation

The single-pole method is used for frequency compensation of the feedback loop. The capacitor C9 is providing this function. The calculation of its value is not easy and is a function of the transfer function of the SMPS and the character of the load. For this reason is recommended to check the power supply stability using a network analyser with the injection transformer.

The best way to find the appropriate value of the compensation capacitor is following: set the capacitor C9 with very high value (in order of microfarads), connect a voltage clamp (zener diode) on the power supply output (possible output voltage overshoot due to slow feedback), connect the power supply to the load, insert a network analyser and run the power supply. Then we measure phase and gain stability margins by network analyser and decrease the value of the compensation capacitor to a minimum value at which the power supply feedback is “enough stable”. The term “enough stable” means: Whenever the closed-loop gain is greater than or equal 1, the closed-loop phase shall never come within 30° of 360°.

4 PCB DESIGN

The printed circuit board (PCB) design is one of the most important processes of the switched mode power supply design. Poor design can lead to future EMI problems and power supply malfunction. Special care of grounding has to be taken. Note the grounded connection of the current sense resistor was used as a base point for all other grounds on the power supply primary side. One also has to avoid a creation of loops that can radiate noise and disturb the power supply’s control circuit and all nearby electronics. For these reasons, a double-sided printed circuit board with plated-through holes and SMD active, and also passive, components were used. Picture 4-1 depicts each side of the PCB.



Top view

Bottom view

Figure 4-1. Printed Circuit Board.

5 CONCLUSION

The MC33364 allows one to build the SMPS with significant saving of external components compared to older control ICs. The saving of those components also means a smaller sensitivity of the control circuit to radiated noise, that every hard-switching power supply produces in a large amounts. The need for only a few external components simplifies the construction and minimises the price. The MC33364 simultaneously keeps enough freedom for the design of various power supplies with output powers from 1W up to tens of watts. The critical conduction mode power supply is also self-protected in case of short circuit on the output, without large current stress on the output rectifier as happens with the fixed frequency current mode of operation.

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