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MOTOROLA

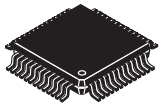
MC13110A
MC13111A

Universal Cordless Telephone Subsystem IC

The MC13110A and MC13111A integrates several of the functions required for a cordless telephone into a single integrated circuit. This significantly reduces component count, board space requirements, external adjustments, and lowers overall costs. It is designed for use in both the handset and the base.

- Fully Programmable in all Power Modes
- Dual Conversion FM Receiver
  - Complete Dual Conversion Receiver – Antenna Input to Audio Out 80 MHz Maximum Carrier Frequency
  - RSSI Output
  - Carrier Detect Output with Programmable Threshold
  - Comparator for Data Recovery
  - Operates with Either a Quad Coil or Ceramic Discriminator
- Compander
  - Expander Includes Mute, Digital Volume Control, Speaker Driver, Programmable Low Pass Filter, and Gain Block
  - Compressor Includes Mute, Programmable Low Pass Filter, Limiter, and Gain Block
- MC13110A only: Frequency Inversion Scrambler
  - Function Controlled via MPU Interface
  - Programmable Carrier Modulation Frequency
- Dual Universal Programmable PLL
  - Supports New 25 Channel U.S. Standard with No External Switches
  - Universal Design for Domestic and Foreign Cordless Telephone Standards
  - Digitally Controlled Via a Serial Interface Port
  - Receive Side Includes 1st LO VCO, Phase Detector, and 14–Bit Programmable Counter and 2nd LO with 12–Bit Counter
  - Transmit Section Contains Phase Detector and 14–Bit Counter
  - MPU Clock Outputs Eliminates Need for MPU Crystal
- Low Battery Detect
  - Provides Two Levels of Monitoring with Separate Outputs
  - Separate, Adjustable Trip Points
- 2.7 to 5.5 V Operation (15 μA Current Consumption in Inactive Mode)
- AN1575: Refer to this Application Note for a List of the “Worldwide Cordless Telephone Frequencies

UNIVERSAL NARROWBAND FM RECEIVER INTEGRATED CIRCUIT



52 1

FB SUFFIX
PLASTIC PACKAGE
CASE 848B
(QFP–52)

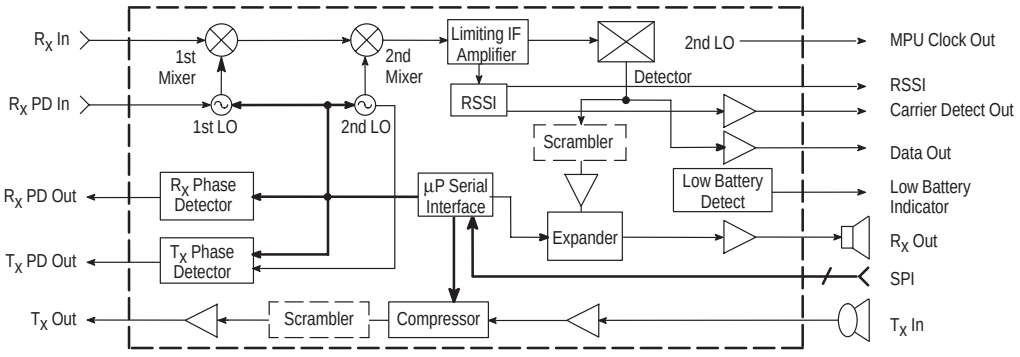
48 1

FTA SUFFIX
PLASTIC PACKAGE
CASE 932
(LQFP–48)

ORDERING INFORMATION

Device	Tested Operating Temperature Range	Package
MC13110AFB	T_A = – 40° to 85°C	QFP–52
MC13110AFTA		LQFP–48
MC13111AFB		QFP–52
MC13111AFTA		LQFP–48

Simplified Block Diagram

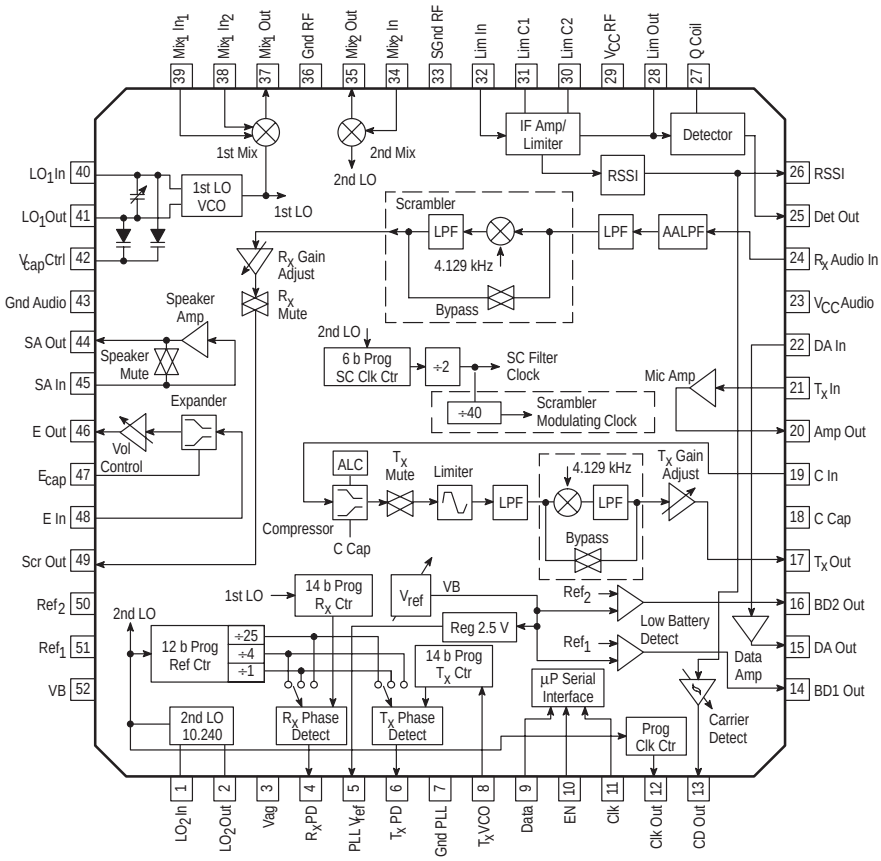


NOTE:
= MC13110A Only

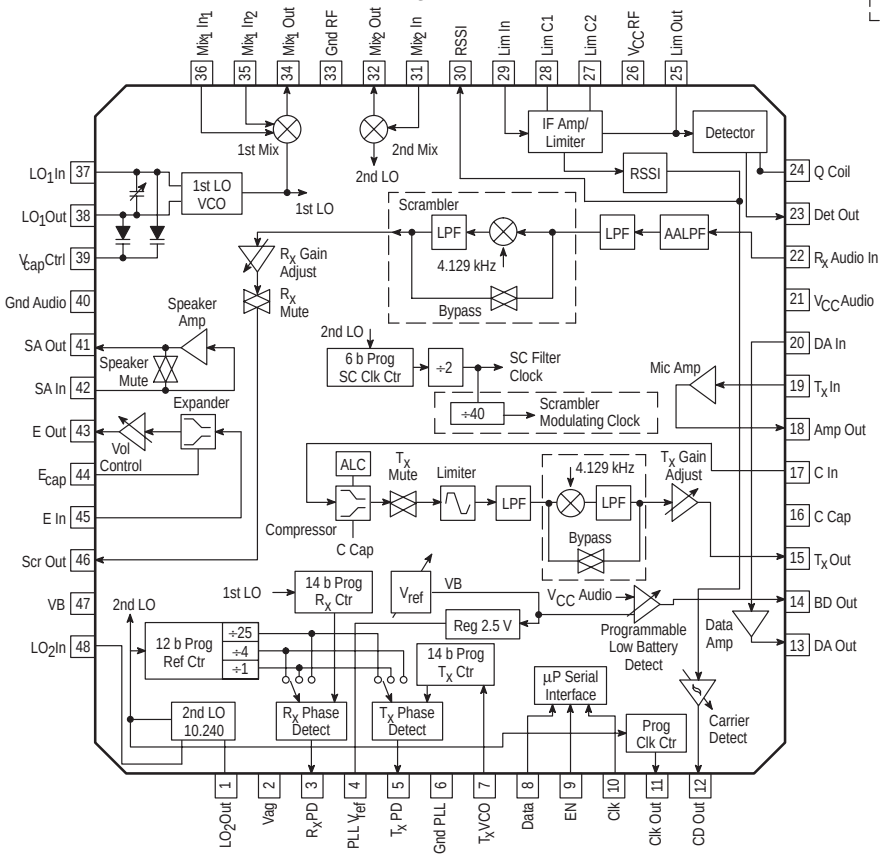
This device contains 8262 active transistors.

PIN CONNECTIONS

QFP–52



LQFP–48



NOTE:
[ ] = MC13110A Only

MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	–0.5 to 6.0	Vdc
Junction Temperature	T_J	–65 to 150	°C
Maximum Power Dissipation, T_A = 25°C	P_D	70	mW

NOTES: 1. Maximum Ratings are those values beyond which damage to the device may occur.
2. Functional operation should be restricted to the limits in the Recommended Operating Conditions and Electrical Characteristics tables or Pin Descriptions section.
3. ESD data available upon request.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	2.7	3.6	5.5	Vdc
Operating Ambient Temperature	T_A	–40	–	85	°C
Input Voltage Low (Data, Clk, EN)	V_{IL}	–	–	0.3	V
Input Voltage High (Data, Clk, EN)	V_{IH}	PLL V_{ref} – 0.3	–	–	V
Bandgap Reference Voltage	V_B	–	1.5	–	V

NOTE: 4. All limits are not necessarily functional concurrently.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 3.6 V, T_A = 25°C, unless otherwise specified, IP3 = 0; Test Circuit Figure 1.)

Characteristic	Symbol	Figure	Min	Typ	Max	Unit
Static Current		1				
Active Mode	ACT I_{CC}		5.5	8.5	10.5	mA
Receive Mode	R_X I_{CC}		3.1	4.1	5.3	mA
Standby Mode	STD I_{CC}		–	465	560	µA
Inactive Mode	INACT I_{CC}		–	15	30	µA
Current Increase When IP3 = 1 (Active and Receive Modes)	I_{IP3}	1	–	1.4	1.8	mA

ELECTRICAL CHARACTERISTICS (V_{CC} = 3.6 V, V_B = 1.5 V, T_A = 25°C, Active or R_x Mode, unless otherwise specified; Test Circuit Figure 1.)

Characteristic	Figure	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
FM RECEIVER (f_{RF} = 46.77 MHz [USA Ch 21], f_{dev} = ±3.0 kHz, f_{mod} = 1.0 kHz, $V_{cap\ ctrl}$ = 1.2 V)								
Input Sensitivity (for 12 dB SINAD at Det Out Using C–Message Weighting Filter) 50 Ω Termination, Generator Referred	68, 69	Mix_1 In_1/In_2	Det Out	V_{SIN}	– –	2.2 –100	– –	µVrms dBm
Single–Ended, Matched Input, Generator Referred					– –	0.4 –115	– –	
Differential, Matched Input, Generator Referred					– –	0.4 –115	– –	
First and Second Mixer Voltage Gain Total (V_{in} = 1.0 mVrms, with CF_1 and CF_2 Load)	1	Mix_1 In_1 or In_2	Mix_2 Out	MX_{gainT}	24	29	–	dB
Isolation of First Mixer Output and Second Mixer Input (V_{in} = 1.0 mVrms, with CFI Removed)	–	Mix_1 In_1 or In_2	Mix_2 In	Mix–Iso	–	60	–	dB
Total Harmonic Distortion (V_{in} = 3.16 mVrms)	1	Mix_1 In_1 or In_2	Det Out	THD	–	1.4	2.0	%
Recovered Audio (V_{in} = 3.16 mVrms)	1	Mix_1 In_1 or In_2	Det Out	AFO	80	112	150	mVrms
AM Rejection Ratio (V_{in} = 3.16 mVrms, 30% AM, @ 1.0 kHz)	1	Mix_1 In_1 or In_2	Det Out	AMR	30	48	–	dB
Signal to Noise Ratio (V_{in} = 3.16 mVrms, No Modulation)	–	Mix_1 In_1 or In_2	Det Out	SNR	–	48	–	dB
FIRST MIXER (No Modulation, f_{in} = USA Ch21, 46.77 MHz, 50 Ω Termination at Inputs)								
Input Impedance Single–Ended	16	–	Mix_1 In_1 or In_2	R_{PS1} C_{PS1}	– –	1.6 3.7	– –	kΩ pF
Differential	16		Mix_1 In_1/In_2	R_{PD1} C_{PD1}	– –	1.6 1.8	– –	
Output Impedance	14	–	Mix_1 Out	R_{P1} Out C_{P1} Out	– –	300 3.7	– –	Ω pF
Voltage Conversion Gain (V_{in} = 1.0 mVrms, with CF_1 Filter as Load)	17, 18	Mix_1 In_1 or In_2	Mix_1 Out	MX_{gain1}	–	12	–	dB
1.0 dB Voltage Compression Level (Input Referred) IP3 Bit Set to 0	19, 21	Mix_1 In_1 or In_2	Mix_1 Out	V_O Mix_1 1 dB	– –	20 –21	– –	mVrms dBm
IP3 Bit Set to 1	20, 21				– –	56 –12	– –	
Third Order Intercept (Input Referred) [Note 5] IP3 Bit Set to 0	19, 21	Mix_1 In_1 or In_2	Mix_1 Out	TOI_{mix1}	– –	64 –11	– –	mVrms dBm
IP3 Bit Set to 1	20, 21				– –	178 –2.0	– –	
–3.0 dB IF Bandwidth	22	Mix_1 In_1 or In_2	Mix_1 Out	Mix_1 BW	–	13	–	MHz

NOTE: 5. Third order intercept calculated for input levels 10 dB below 1.0 dB compression point.

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 3.6 V, V_B = 1.5 V, T_A = 25°C, Active or R_X Mode, unless otherwise specified; Test Circuit Figure 1.)

Characteristic	Figure	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
SECOND MIXER (No Modulation, f_{in} = 10.7 MHz, 50 Ω Termination at Inputs)								
Input Impedance	24	Mix_2 In	Mix_2 In	R_{P2} In C_{P2} In	– –	2.8 3.6	– –	kΩ pF
Output Impedance	24	–	Mix_2 Out	R_{P2} Out C_{P2} Out	– –	1.5 6.1	– –	kΩ pF
Voltage Conversion Gain (V_{in} = 1.0 mVrms, with CF_2 Filter as Load)	26, 27	Mix_2 In	Mix_2 Out	MX_{gain2}	–	20	–	dB
1.0 dB Voltage Compression Level (Input Referred) IP3 Bit Set 0 IP3 Bit Set 1	28, 30 29, 30	Mix_2 In	Mix_2 Out	V_O Mix_2 1 dB	– – – –	32 –17 45 –14	– – – –	mVrms dBm
Third Order Intercept (Input Referred) [Note 6] IP3 Bit Set 0 IP3 Bit Set 1	28, 30 29, 30	Mix_2 In	Mix_2 Out	TOI_{mix2}	– – – –	136 –4.3 158 –3.0	– – – –	mVrms dBm
–3.0 dB IF Bandwidth	31	Mix_2 In	Mix_2 Out	Mix_2 BW	–	2.5	–	MHz
LIMITER/DEMODULATOR (f_{in} = 455 kHz, f_{dev} = ±3.0 kHz, f_{mod} = 1.0 kHz)								
Input Impedance	49	Lim In	Lim In	R_{PLim} C_{PLim}	– –	1.5 16	– –	kΩ pF
Detector Output Impedance	–	–	Det Out	R_O	–	1.1	–	kΩ
IF –3.0 dB Limiting Sensitivity	1	Lim In	Det Out	IF Sens	–	71	100	μVrms
Demodulator Bandwidth	–	Lim In	Det Out	BW	–	20	–	kHz
RSSI/CARRIER DETECT (No Modulation)								
RSSI Output Dynamic Range	56	Mix_1 In	RSSI	RSSI	–	80	–	dB
DC Voltage Range	56	Mix_1 In	RSSI	DC RSSI	–	0.2 to 1.5	–	Vdc
Carrier Detect Threshold CD Threshold Adjust = (10100) (Threshold Relative to Mix_1 In Level)	57	Mix_1 In	CD Out	V_T	–	15	–	μVrms
Hysteresis, CD = (10100) (Threshold Relative to Mix_1 In Level)	57	Mix1 In	CD Out	Hys	–	2.0	–	dB
Output High Voltage CD = (00000), RSSI = 0.2 V	1	RSSI	CD Out	V_{OH}	V_{CC} – 0.1	3.6	–	V
Output Low Voltage CD = (11111), RSSI = 0.9 V	1	RSSI	CD Out	V_{OL}	–	0.02	0.4	V
Carrier Detect Threshold Adjustment Range (Programmable through MPU Interface)	125	–	–	V_T Range	–	–20 to 11	–	dB
Carrier Detect Threshold – Number of Programmable Levels	125	–	–	V_{Tn}	–	32	–	–

NOTE: 6. Third order intercept calculated for input levels 10 dB below 1.0 dB compression point.

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 3.6 V, V_B = 1.5 V, T_A = 25°C, Active or R_X Mode, unless otherwise specified; Test Circuit Figure 1.)

Characteristic	Figure	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
R_X AUDIO PATH (f_{in} = 1.0 kHz, Active Mode, scrambler bypassed)								
Absolute Gain (V_{in} = –20 dBV)	1, 72	R_X Audio In	SA Out	G	–4.0	0	4.0	dB
Gain Tracking (Referenced to E Out for V_{in} = –20 dBV) V_{in} = –30 dBV V_{in} = –40 dBV	1, 76	E In	E Out	G_t	 –21 –42	 –20 –40	 –19 –38	dB
Total Harmonic Distortion (V_{in} = –20 dBV)	1, 76	R_X Audio In	SA Out	THD	–	0.7	1.0	%
Maximum Input Voltage (V_{CC} = 2.7 V)	76	R_X Audio In	–	–	–	–11.5	–	dBV
Maximum Output Voltage (Increase input voltage until output voltage THD = 5.0%, then measure output voltage)	1	E In	E Out	V_{Omax}	–2.0	0	–	dBV
Input Impedance	–	R_X Audio In E In	–	Z_{in}	– –	600 7.5	– –	kΩ
Attack Time E_{cap} = 0.5 µF, R_{filt} = 40 k (See Appendix B)	–	E In	E Out	t_a	–	3.0	–	ms
Release Time E_{cap} = 0.5 µF, R_{filt} = 40 k (See Appendix B)	–	E In	E Out	t_r	–	13.5	–	ms
Compressor to Expander Crosstalk V_{in} = –10 dBV, $V_{(E\ In)}$ = AC Gnd	1	C In	E Out	C_T	–	–90	–70	dB
R_X Muting (Δ Gain) V_{in} = –20 dBV, R_X Gain Adj = (01111)	1	R_X Audio In	E Out	M_e	–	–84	–60	dB
R_X High Frequency Corner R_X Path, V R_X Audio In = –20 dBV	1	R_X Audio In	Scr Out	R_X f_{ch}	3.779	3.879	3.979	kHz
Low Pass Filter Passband Ripple (V_{in} = –20 dBV)	1, 73	R_X Audio In	Scr Out	Ripple	–	0.4	0.6	dB
R_X Gain Adjust Range (Programmable through MPU Interface)	124	R_X Audio In	Scr Out	R_X Range	–	–9.0 to 10	–	dB
R_X Gain Adjust Steps – Number of Programmable Levels	124	R_X Audio In	Scr Out	R_X n	–	20	–	dB
Audio Path Noise, C–Message Weighting (Input AC–Grounded)	70	R_X Audio In	Scr Out E Out SA Out	EN	– –	–85 <–95 <–95	– –	dBV
Volume Control Adjust Range	122	E In	E Out	V_{ctl}Range	–	–14 to 16	–	dB
Volume Control – Number of Programmable Levels	122	E In	E Out	V_{cn}	–	16	–	–
SPEAKER AMP/SP MUTE (Active Mode)								
Maximum Output Swing R_L = No Load, V_{in} = 3.4 Vpp R_L = 130 Ω, V_{in} = 2.8 Vpp R_L = 620 Ω, V_{in} = 4.0 Vpp	1, 79	SA In	SA Out	V_{Omax}	 2.8 2.0 –	 3.2 2.6 3.4	 – – –	Vpp
Speaker Amp Muting V_{in} = –20 dBV, R_L = 130 Ω	1	SA In	SA Out	M_{sp}	–	–92	–60	dB

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 3.6 V, V_B = 1.5 V, T_A = 25°C, Active or R_X Mode, unless otherwise specified; Test Circuit Figure 1.)

Characteristic	Figure	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
DATA AMP COMPARATOR								
Hysteresis	1	DA In	DA Out	Hys	30	42	50	mV
Threshold Voltage	–	DA In	DA Out	V_T	–	V_{CC} – 0.7	–	V
Input Impedance	1	–	DA In	Z_I	200	250	280	kΩ
Output Impedance	–	–	DA Out	Z_O	–	100	–	kΩ
Output High Voltage V_{in} = V_{CC} – 1.0 V, I_{OH} = 0 mA	1	DA In	DA Out	V_{OH}	V_{CC} – 0.1	3.6	–	V
Output Low Voltage V_{in} = V_{CC} – 0.4 V, I_{OL} = 0 mA	1	DA In	DA Out	V_{OL}	–	0.1	0.4	V
Maximum Frequency	–	DA In	DA Out	F_{max}	–	10	–	kHz
MIC AMP (f_{in} = 1.0 kHz, External resistors set to gain of 1, Active Mode)								
Open Loop Gain	–	T_X In	Amp Out	AVOL	–	100,000	–	V/V
Gain Bandwidth	–	T_X In	Amp Out	GBW	–	100	–	kHz
Maximum Output Swing (R_L = 10 kΩ)	–	T_X In	Amp Out	V_{Omax}	–	3.2	–	Vpp
T_X AUDIO PATH (f_{in} = 1.0 kHz, T_X Gain Adj = (01111); ALC, Limiter, and Mutes Disabled; Active Mode, scrambler bypassed)								
Absolute Gain (V_{in} = –10 dBV)	1, 83	T_X In	T_X Out	G	–4.0	0	4.0	dB
Gain Tracking (Referenced to T_X Out for V_{in} = –10 dBV) V_{in} = –30 dBV V_{in} = –40 dBV	1, 87	T_X In	T_X Out	G_t	 –11 –17	 –10 –15	 –9.0 –13	dB
Total Harmonic Distortion (V_{in} = –10 dBV)	1, 87	T_X In	T_X Out	THD	–	0.8	1.8	%
Maximum Output Voltage (Increase input voltage until output voltage THD = 5.0%, then measure output voltage. T_X Gain Adjust = 8 dB)	1	T_X In	T_X Out	V_{Omax}	–2.0	0	–	dBV
Input Impedance	–	–	C In	Z_{in}	–	10	–	kΩ
Attack Time (C_{cap} = 0.5 µF, R_{filt} = 40 k (See Appendix B))	–	C In	T_X Out	t_a	–	3.0	–	ms
Release Time (C_{cap} = 0.5 µF, R_{filt} = 40 k (See Appendix B))	–	C In	T_X Out	t_r	–	13.5	–	ms
Expander to Compressor Crosstalk (V_{in} = –20 dBV, Speaker Amp No Load, $V_{(C\ In)}$ = AC Gnd)	1	E In	T_X Out	C_T	–	–60	–40	dB
T_X Muting (V_{in} – 10 dBV)	1	T_X In	T_X Out	M_C	–	–88	–60	dB
ALC Output Level (ALC enabled) V_{in} = –10 dBV V_{in} = –2.5 dBV	1, 87, 90	T_X In	T_X Out	ALC_{out}	 –15 –13	 –13 –11	 –8.0 –6.0	dBV
ALC Slope (ALC enabled) V_{in} = –10 dBv V_{in} = –2.5 dBv	1	T_X In	T_X Out	Slope	0.1	0.25	0.4	dB/dB
ALC Input Dynamic Range	–	C In	T_X Out	DR	–	–16 to –2.5	–	dBV
Limiter Output Level (V_{in} = –2.5 dBV, Limiter enabled)	1	T_X In	T_X Out	V_{lim}	–10	–8.0	–	dBV
T_X High Frequency Corner [Note 7] (VT_X In = –10 dBV, Mic Amp = Unity Gain)	1	T_X In	T_X Out	T_X f_c	3.6	3.7	3.8	kHz

NOTE: 7. The filter specification is based on a 10.24 MHz 2nd LO, and a switched–capacitor (SC) filter counter divider ratio of 31. If other 2nd LO frequencies and/or SC filter counter divider ratios are used, the filter corner frequency will be proportional to the resulting SC filter clock frequency.

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 3.6 V, V_B = 1.5 V, T_A = 25°C, Active or R_X Mode, unless otherwise specified; Test Circuit Figure 1.)

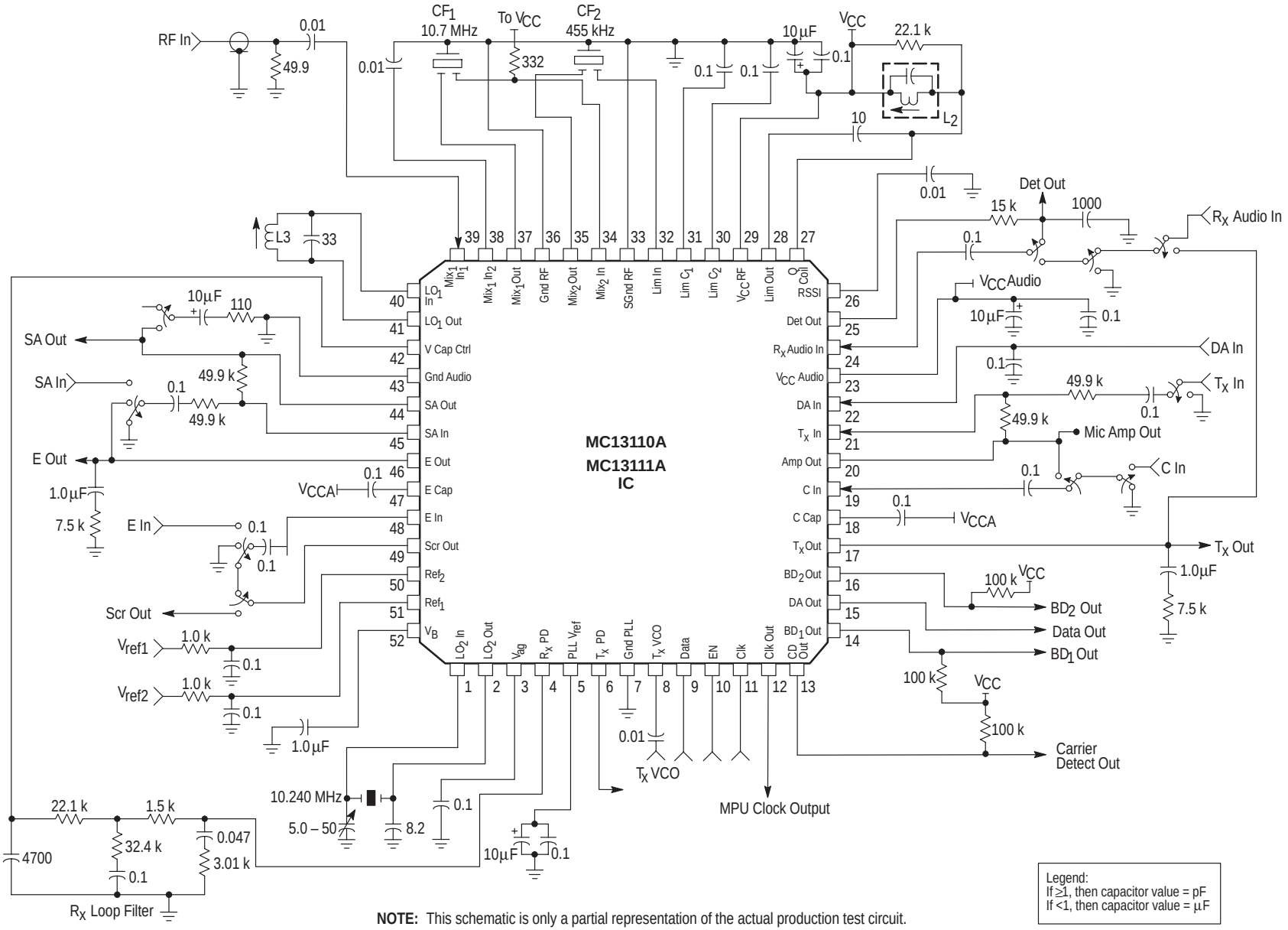
Characteristic	Figure	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
T_X AUDIO PATH (f_{in} = 1.0 kHz, T_X Gain Adj = (01111); ALC, Limiter, and Mutes Disabled; Active Mode, scrambler bypassed)								
Low Pass Filter Passband Ripple (V_{in} = –10 dBV)	1, 84	T_X In	T_X Out	Ripple	–	0.7	1.2	dB
Maximum Compressor Gain (V_{in} = –70 dBV)	–	C In	T_X Out	AV_{max}	–	23	–	dB
T_X Gain Adjust Range (Programmable through MPU Interface)	124	C In	T_X Out	T_X Range	–	–9.0 to 10	–	dB
T_X Gain Adjust Steps – Number of Programmable Levels	124	C In	T_X Out	T_X n	–	20	–	–
R_X AND T_X SCRAMBLER (2nd LO = 10.24 MHz, T_X Gain Adj = (01111), R_X Gain Adj = (01111), Volume Control = (0 dB Default Levels), SCF Clock Divider = 31. Total is divide by 62 for SCF clock frequency of 165.16 kHz)								
R_X High Frequency Corner (Note 8) R_X Path, f = 479 Hz, V R_X Audio In = –20 dBV	–	R_X Audio In	Scr Out	R_X f_{ch}	3.55	3.65	3.75	kHz
T_X High Frequency Corner (Note 8) T_X Path, f = 300 Hz, V T_X In = –10 dBV, Mic Amp = Unity Gain	–	T_X In	T_X Out	T_X f_{ch}	3.829	3.879	3.929	kHz
Absolute Gain R_X: V_{in} = –20 dBV T_X: V_{in} = –10 dBV, Limiter disabled	 – –	 R_X Audio In T_X In	 E Out T_X Out	AV	 –4.0 –4.0	 0.4 –1.0	 4.0 4.0	dB
Pass Band Ripple R_X + T_X Path – 1.0 µF from T_X Out to R_X Audio In, f_{in} = low corner frequency to high corner frequency	–	C In	E Out	Ripple	–	1.9	2.5	dB
Scrambler Modulation Frequency R_X: 100 mV (–20 dBV) T_X: 316 mV (–10 dBV)	 – –	 R_X Audio In C In	 E Out T_X Out	f_{mod}	4.119	4.129	4.139	kHz
Group Delay R_X + T_X Path – 1.0 µF from T_X Out to R_X Audio In, f_{in} = 1.0 kHz	–	C In	E Out	GD	–	1.0	–	ms
f_{in} = low corner frequency to high corner frequency	–	C In	E Out	GD	–	4.0	–	
Carrier Breakthrough R_X + T_X Path – 1.0 µF from T_X Out to R_X Audio In	–	C In	E Out	CBT	–	–60	–	dB
Baseband Breakthrough R_X + T_X Path – 1.0 µF from T_X Out to R_X Audio In, f_{in} = 1.0 kHz, f_{meas} = 3.192 kHz	–	C In	E Out	BBT	–	–50	–	dB
LOW BATTERY DETECT								
Average Threshold Voltage Before Electronic Adjustment (V_{ref}_Adj = (0111))	1, 130	Ref_1 Ref_2	BD_1 Out BD_2 Out	VT_i	1.38	1.48	1.58	V
Average Threshold Voltage After Electronic Adjustment (V_{ref}_Adj = (adjusted value))	1	Ref_1 Ref_2	BD_1 Out BD_2 Out	VT_f	1.475	1.5	1.525	V
Hysteresis	–	Ref_1 Ref_2	BD_1 Out BD_2 Out	Hys	–	4.0	–	mV
Input Current (V_{in} = 1.0 and 2.0 V)	1	–	Ref_1 Ref_2	I_{in}	–50	–	50	nA
Output High Voltage (V_{in} = 2.0 V)	1	Ref_1 Ref_2	BD_1 Out BD_2 Out	V_{OH}	V_{CC} – 0.1	3.6	–	V

NOTE: 8. The filter specification is based on a 10.24 MHz 2nd LO, and a switch–capacitor (SC) filter counter divider ratio of 31. If other 2nd LO frequencies and/or SC filter counter divider ratios are used, the filter corner frequency will be proportional to the resulting SC filter clock frequency.

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 3.6 V, V_B = 1.5 V, T_A = 25°C, Active or R_X Mode, unless otherwise specified; Test Circuit Figure 1.)

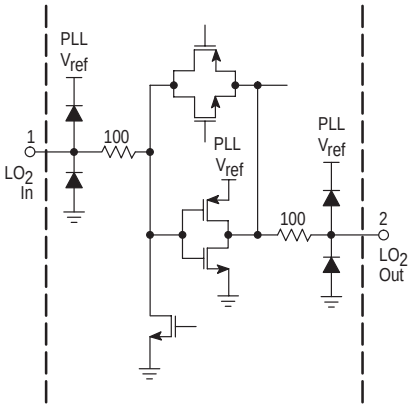
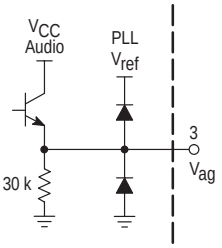
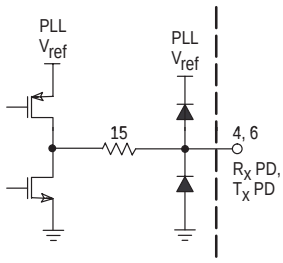
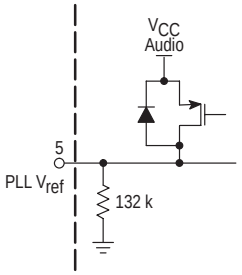
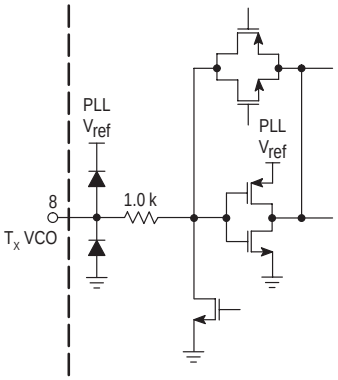
Characteristic	Figure	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
LOW BATTERY DETECT								
Output Low Voltage (V_{in} = 1.0 V)	1	Ref_1 Ref_2	BD_1 Out BD_2 Out	V_{OL}	–	0.2	0.4	V
BATTERY DETECT INTERNAL THRESHOLD								
After Electronic Adjustment of V_B Voltage	1, 127	V_{CC} Audio	BD_2 Out					V
BD Select = (111)				IBS_7	3.381	3.455	3.529	
BD Select = (110)				IBS_6	3.298	3.370	3.442	
BD Select = (101)				IBS_5	3.217	3.287	3.357	
BD Select = (100)				IBS_4	3.134	3.202	3.270	
BD Select = (011)				IBS_3	2.970	3.034	3.098	
BD Select = (010)				IBS_2	2.886	2.948	3.010	
BD Select = (001)				IBS_1	2.802	2.862	2.922	
PLL PHASE DETECTOR								
Output Source Current (V_{PD} = Gnd + 0.5 V to PLL V_{ref} – 0.5 V)	–	–	R_X PD T_X PD	I_{OH}	–	1.0	–	mA
Output Sink Current (V_{PD} = Gnd + 0.5 V to PLL V_{ref} – 0.5 V)	–	–	R_X PD T_X PD	I_{OL}	–	1.0	–	mA
PLL LOOP CHARACTERISTICS								
Maximum 2nd LO Frequency (No Crystal)	–	LO_2 In	–	f_{2ext}	–	12	–	MHz
Maximum 2nd LO Frequency (With Crystal)	–	–	LO_2 In LO_2 Out	f_{2ext}	–	12	–	MHz
Maximum T_X VCO (Input Frequency), V_{in} = 200 mVpp	–	–	T_X VCO	f_{txmax}	–	80	–	MHz
PLL VOLTAGE REGULATOR								
Regulated Output Level (I_L = 0 mA, after V_{ref} Adjustment)	1	–	PLL V_{ref}	V_O	2.4	2.5	2.6	V
Line Regulation (I_L = 0 mA, V_{CC} = 3.0 to 5.5 V)	1	V_{CC} Audio	PLL V_{ref}	V_{Reg}Line	–	11.8	40	mV
Load Regulation (I_L = 1.0 mA)	1	V_{CC} Audio	PLL V_{ref}	V_{Reg} Load	–20	–1.4	–	mV
MICROPROCESSOR SERIAL INTERFACE								
Input Current Low (V_{in} = 0.3 V, Standby Mode)	1	–	Data, Clk, EN	I_{IL}	–5.0	0.4	–	µA
Input Current High (V_{in} = 3.3 V, Standby Mode)	1	–	Data, Clk, EN	I_{IH}	–	1.6	5.0	µA
Hysteresis Voltage	–	–	Data, Clk, EN	V_{hys}	–	1.0	–	V
Maximum Clock Frequency	–	Data, EN, Clk	–	–	–	2.0	–	MHz
Input Capacitance	–	Data, Clk, EN	–	C_{in}	–	8.0	–	pF
EN to Clk Setup Time	106	–	EN, Clk	t_{suEC}	–	200	–	ns
Data to Clk Setup Time	105	–	Data, Clk	t_{suDC}	–	100	–	ns
Hold Time	105	–	Data, Clk	t_h	–	90	–	ns
Recovery Time	106	–	EN, Clk	t_{rec}	–	90	–	ns
Input Pulse Width	–	–	EN, Clk	t_w	–	100	–	ns
MPU Interface Power–Up Delay (90% of PLL V_{ref} to Data,Clk, EN)	108	–	–	t_{puMPU}	–	100	–	µs

Figure 1. Production Test Circuit (52 Pin QFP)

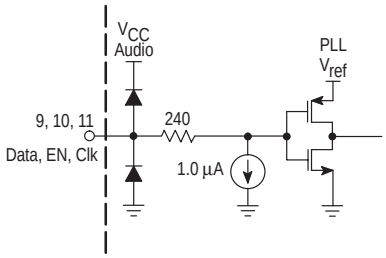
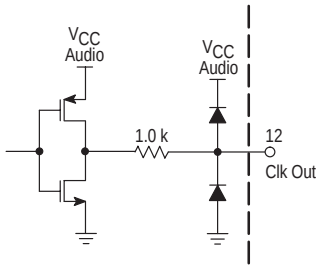
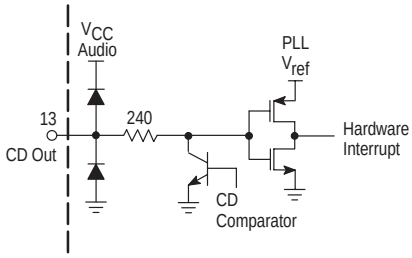
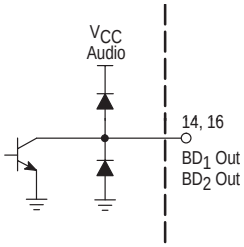
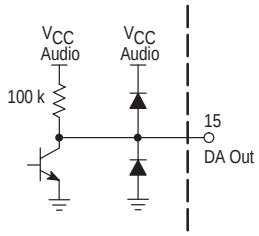
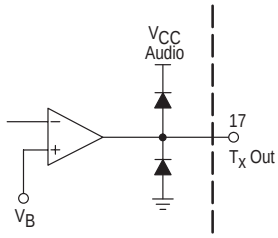


NOTE: This schematic is only a partial representation of the actual production test circuit.

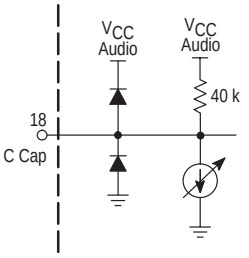
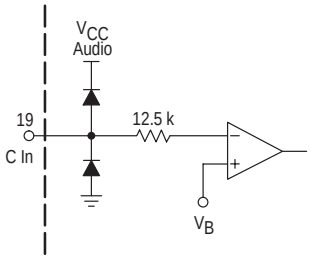
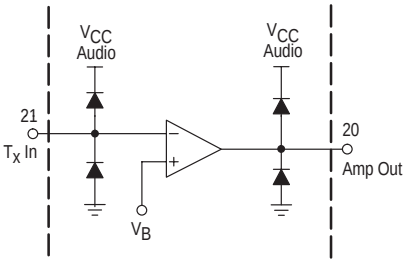
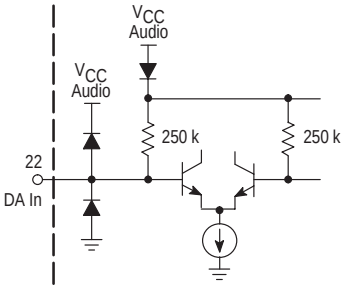
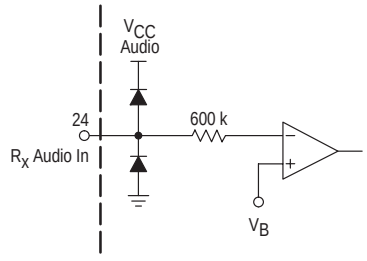
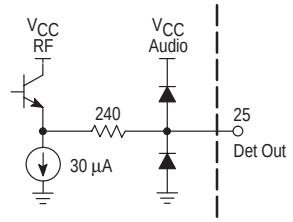
PIN FUNCTION DESCRIPTION

Pin		Symbol/ Type	Equivalent Internal Circuit (52 Pin QFP)	Description
LQFP–48	QFP–52			
48 1	1 2	LO_2 In LO_2 Out		These pins form the PLL reference oscillator when connected to an external parallel–resonant crystal (10.24 MHz typical). The reference oscillator is also the second Local Oscillator (LO_2) for the RF receiver. "LO_2 In" may also serve as an input for an externally generated reference signal which is typically ac–coupled. When the IC is set to the inactive mode, LO_2 In is internally pulled low to disable the oscillator. The input capacitance to ground at each pin (LO_2 In/ LO_2 Out) is 3.0 pF.
2	3	V_{ag}		V_{ag} is the internal reference voltage for the switched capacitor filter section. This pin must be decoupled with a 0.1 μF capacitor.
3	4	R_X PD (Output)		This pin is a tri–state voltage output of the R_X and T_X Phase Detector. It is either "high", "low", or "high impedance," depending on the phase difference of the phase detector input signals. During lock, very narrow pulses with a frequency equal to the reference frequency are present. This pin drives the external R_X and T_X PLL loop filters. R_X and T_X PD outputs can sink or source 1.0 mA.
5	6	T_X PD (Output)		
4	5	PLL V_{ref}		PLL V_{ref} is a PLL voltage regulator output pin. An internal voltage regulator provides a stable power supply voltage for the R_X and T_X PLL's and can also be used as a regulated supply voltage for other IC's. It can source up to 1.0 mA externally. Proper supply filtering is a must on this pin. PLL V_{ref} is pulled up to V_{CC} audio for the standby and inactive modes (Note 1).
6	7	Gnd PLL		Ground pin for digital PLL section of IC.
7	8	T_X VCO (Input)		T_X VCO is the transmit divide counter input which is driven by an ac–coupled external transmit loop VCO. The minimum signal level is 200 mVpp @ 60.0 MHz. This pin also functions as the test mode input for the counter tests.

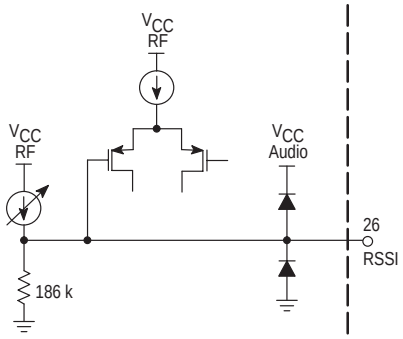
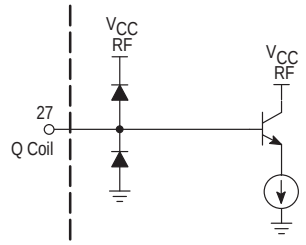
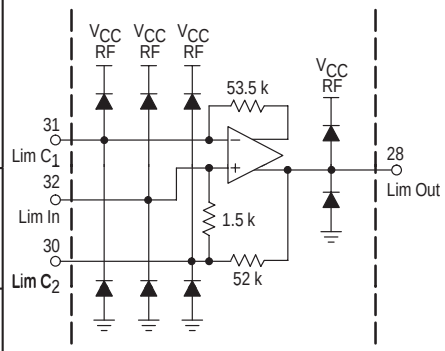
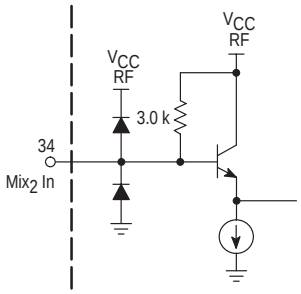
PIN FUNCTION DESCRIPTION (continued)

Pin		Symbol/ Type	Equivalent Internal Circuit (52 Pin QFP)	Description
LQFP–48	QFP–52			
8 9 10	9 10 11	Data EN Clk (Input)		Microprocessor serial interface input pins are for programming various counters and control functions. The switching thresholds are referenced to PLL V_{ref} and Gnd PLL. The inputs operate up to V_{CC}. These pins have 1.0 µA internal pull–down currents.
11	12	Clk Out (Output)		The microprocessor clock output is derived from the 2nd LO crystal oscillator and a programmable divider with divide ratios of 2 to 312.5. It can be used to drive a microprocessor and thereby reduce the number of crystals required in the system design. The driver has an internal resistor in series with the output which can be combined with an external capacitor to form a low pass filter to reduce radiated noise on the PCB. This output also functions as the output for the counter test modes. The Clk Out can be disabled via the MPU interface.
12	13	CD Out (I/O)		Dual function pin; 1) Carrier detect output (open collector with external 100 kΩ pull–up resistor. 2) Hardware interrupt input which can be used to “wake–up” from the Inactive Mode.
–	14	BD_1 Out		Low battery detect output #1 is an open collector with external pull–up resistor.
14	16	BD_2 Out (Output)		Low battery detect output #2 is an open collector with external pull–up resistor.
13	15	DA Out (Output)		Data amplifier output (open collector with internal 100 kΩ pull–up resistor).
15	17	T_X Out (Output)		T_X Out is the T_X path audio output. Internally this pin has a low–pass filter circuitry with –3 dB bandwidth of 4.0 kHz. T_X gain and mute are programmable through the MPU interface. This pin is sensitive to load capacitance.

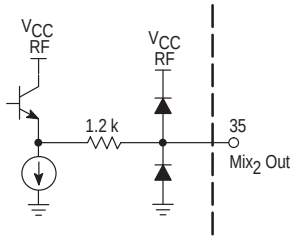
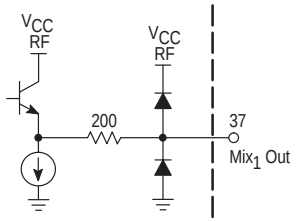
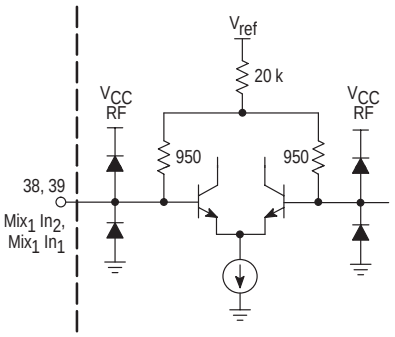
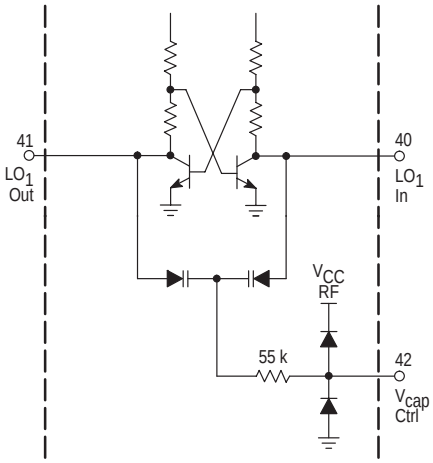
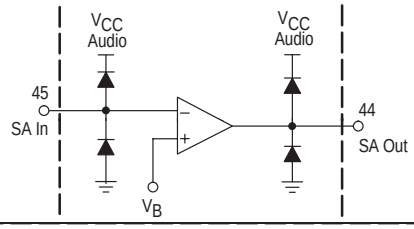
PIN FUNCTION DESCRIPTION (continued)

Pin		Symbol/ Type	Equivalent Internal Circuit (52 Pin QFP)	Description
LQFP–48	QFP–52			
16	18	C Cap		C Cap is the compressor rectifier filter capacitor pin. It is recommended that an external filter capacitor to V_{CC} audio be used. A practical capacitor range is 0.1 to 1.0 µF. 0.47 µF is the recommended value.
17	19	C In (Input)		C In is the compressor input. This pin is internally biased and has an input impedance of 12.5 k. C In must be ac–coupled.
18	20	Amp Out (Output)		Microphone amplifier output. The gain is set with external resistors. The feedback resistor should be less than 200 kΩ.
19	21	T_X In (Input)		T_X In is the T_X path input to the microphone amplifier (Mic Amp). An external resistor is connected to this pin to set the Mic Amp gain and input impedance. T_X In must be ac–coupled, too.
20	22	DA In (Input)		The data amplifier input (DA In) resistance is 250 kΩ and must be ac–coupled. Hysteresis is internally provided.
21	23	V_{CC} Audio		V_{CC} audio is the supply for the audio section. It is necessary to adequately filter this pin.
22	24	R_X Audio In (Input)		The R_X audio input resistance is 600 kΩ and must be ac–coupled.
23	25	Det Out (Output)		Det Out is the audio output from the FM detector. This pin is dc–coupled from the FM detector and has an output impedance of 1100 Ω.

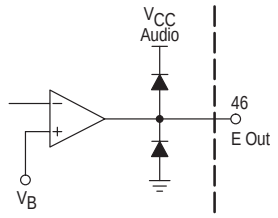
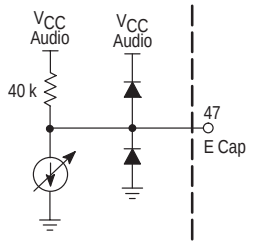
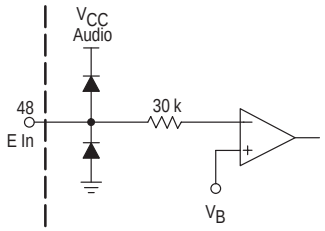
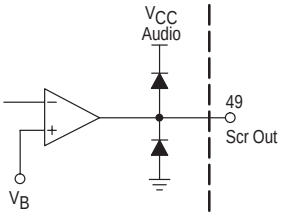
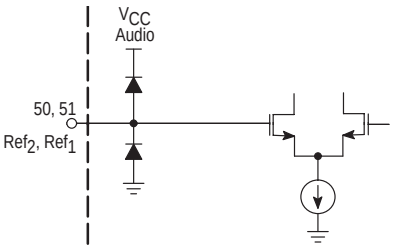
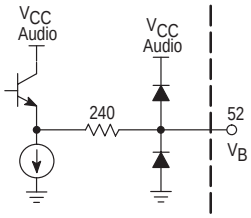
PIN FUNCTION DESCRIPTION (continued)

Pin		Symbol/ Type	Equivalent Internal Circuit (52 Pin QFP)	Description
LQFP–48	QFP–52			
30	26	RSSI		RSSI is the receive signal strength indicator. This pin must be filtered through a capacitor to ground. The capacitance value range should be 0.01 to 0.1 µF. This is also the input to the Carrier Detect comparator. An external R to ground shifts the RSSI voltage.
24	27	Q Coil		A quad coil or ceramic discriminator connects this pin as part of the FM demodulator circuit. DC–couple this pin to V_{CC} RF through the quad coil or the external resistor.
26	29	V_{CC} RF		V_{CC} supply for RF receiver section (1st LO, mixer, limiter, demodulator). Proper supply filtering is needed on this pin too.
25	28	Lim Out		A quad coil or ceramic discriminator are connected to these pins as part of the FM demodulator circuit. A coupling capacitor connects this pin to the quad coil or ceramic discriminator as part of the FM demodulator circuit. This pin can drive coupling capacitors up to 47 pF with no deterioration in performance.
27 28	30 31	Lim C_2 Lim C_1		IF amplifier/limiter capacitor pins. These decoupling capacitors should be 0.1 µF. They determine the IF limiter gain and low frequency bandwidth.
29	32	Lim In (Input)		Signal input for IF amplifier/limiter. Signals should be ac–coupled to this pin. The input impedance is 1.5 kΩ at 455 kHz.
–	33	SGnd RF		This pin is not connected internally but should be grounded to reduce potential coupling between pins.
31	34	Mix_2 In (Input)		Mix_2 In is the second mixer input. Signals are to be ac–coupled to this pin, which is biased internally to V_{CC} RF. The input impedance is 2.8 kΩ at 455 kHz. The input impedance can be reduced by connecting an external resistor to V_{CC} RF.

PIN FUNCTION DESCRIPTION (continued)

Pin		Symbol/ Type	Equivalent Internal Circuit (52 Pin QFP)	Description
LQFP–48	QFP–52			
32	35	Mix_2 Out (Output)		Mix_2 Out is the second mixer output. The second mixer has a 3 dB bandwidth of 2.5 MHz and an output impedance of 1.5 kΩ. The output current drive is 50 μA.
33	36	Gnd RF		Ground pin for RF section of the IC.
34	37	Mix_1 Out (Output)		The first mixer has a 3 dB IF bandwidth of 13 MHz and an output impedance of 300 Ω. The output current drive is 300 μA and can be programmed for 1.0 mA.
35	38	Mix_1 In_2 (Input)		Signals should be ac–coupled to this pin, which is biased internally to V_{CC} – 1.6 V. The single–ended and differential input impedance are about 1.6 and 1.8 kΩ at 46 MHz, respectively.
36	39	Mix_1 In_1 (Input)		
37 38	40 41	LO_1 In LO_1 Out		Tank Elements, an internal varactor and capacitor matrix for 1st LO multivibrator oscillator are connected to these pins. The oscillator is useable up to 80 MHz.
39	42	V_{cap} Ctrl		V_{cap} Ctrl is the 1st LO varactor control pin. The voltage at this pin is referenced to Gnd Audio and varies the capacitance between LO_1 In and LO_2 Out. An increase in voltage will decrease capacitance.
40	43	Gnd Audio		Ground for audio section of the IC.
41	44	SA Out (Output)		The speaker amplifier gain is set with an external feedback resistor. It should be less than 200 kΩ. The speaker amplifier can be muted through the MPU interface.
42	45	SA In (Input)		An external resistor is connected to the speaker amplifier input (SA In). This will set the gain and input impedance and must be ac–coupled.

PIN FUNCTION DESCRIPTION (continued)

Pin		Symbol/ Type	Equivalent Internal Circuit (52 Pin QFP)	Description
LQFP–48	QFP–52			
43	46	E Out (Output)		The output level of the expander output is determined by the volume control. Volume control is programmable through the MPU interface.
44	47	E Cap		E Cap is the expander rectifier filter capacitor pin. Connect an external filter capacitor between V_{CC} audio and E Cap. The recommended capacitance range is 0.1 to 1.0 μF. 0.47 μF is the suggested value.
45	48	E In (Input)		The expander input pin is internally biased and has input impedance of 30 kΩ.
46	49	Scr Out (Output)		Scr Out is the R_X audio output. An internal low pass filter has a –3 dB bandwidth of 4.0 kHz.
–	50	Ref_2		Reference voltage input for Low Battery Detect #2.
–	51	Ref_1		Reference voltage input for Low Battery Detect #1.
47	52	V_B		V_B is the internal half supply analog ground reference. This pin must be filtered with a capacitor to ground. A typical capacitor range of 0.5 to 10 μF is desired to reduce crosstalk and noise. It is important to keep this capacitor value equal to the PLL V_{ref} capacitor due to logic timing (Note 9).

NOTE: 9. A capacitor range of 0.5 to 10 μF is recommended. The capacitor value should be the same used on the V_B pin (Pin 52). An additional high quality parallel capacitor of 0.01 μF is essential to filter out spikes originating from the PLL logic circuitry.

The following text, graphics, tables and schematics are provided to the user as a source of valuable technical information about the Universal Cordless Telephone IC. This information originates from thorough evaluation of the device performance for the US and French applications. This data was obtained by using units from typical wafer lots. It is important to note that the forgoing data and information was from a limited number of units. By no means is the user to assume that the data following is a guaranteed parametric. Only the minimum and maximum limits identified in the electrical characteristics tables found earlier in this spec are guaranteed.

General Circuit Description

The MC13110A and MC13111A are a low power dual conversion narrowband FM receiver designed for applications up to 80 MHz carrier frequency. This device is primarily designated to be used for the 49 MHz cordless phone (CT–0), but has other applications such as low data rate narrowband data links and as a backend device for 900 MHz systems where baseband analog processing is required. This device contains a first and second mixer, limiter, demodulator, extended range receive signal strength (RSSI), receive and transmit baseband processing, dual programmable PLL, low battery detect, and serial interface for microprocessor control. The FM receiver can also be used with either a quadrature coil or ceramic resonator. Refer to the Pin Function Description table for the simplified internal circuit schematic and description of this device.

DC Current and Battery Detect

Figures 3 through 6 are the current consumption for Inactive, Standby, Receive, and Active modes versus supply voltages. Figures 7 and 8 show the typical behavior of current consumption in relation to temperature. The relationship of additional current draw due to IP3 bit set to <1> and supply voltage are shown in Figures 9 and 10.

For the Low Battery Detect, the user has the option to operate the IC in the programmable or non–programmable modes. Note that the 48 pin package can only be used in the programmable mode. Figure 127 describes this operation (refer to the Serial Interface section under Clock Divider Register).

In the programmable mode several different internal threshold levels are available (Figure 2). The bits are set through the SCF Clock Divider Register as shown in Figures 108 and 125. The reference for the internal divider network is V_{CC} Audio. The voltages on the internal divider network are compared to the Internal Reference Voltage, VB, generated by an internal source. Since the internal comparator used is non–inverting, a high at V_{CC} Audio will yield a high at the battery detect output, and vice versa for V_{CC} Audio set to a low level. For the 52 pin package option, the Ref 1 and Ref 2 pins need to be tied to V_{CC} when used in the programmable mode. It is essential to keep the external reference pins above Gnd to prevent any possible power–on reset to be activated.

When considering the non–programmable mode (bits set to <000>) for the 52 pin package, the Ref 1 and Ref 2 pins become the comparators reference. An internal switch is activated when the non–programmable mode is chosen connecting Ref 1 and Ref 2. Here, two external precision resistor dividers are used to set independent thresholds for two battery detect hysteresis comparators. The voltages on Ref 1 and Ref 2 are again compared to the internally generated 1.5 V reference voltage (VB).

The Low Battery Detect threshold tolerance can be improved by adjusting a trim–pot in the external resistor divider (user designed). The initial tolerance of the internal reference voltage (VB) is ±6.0%. Alternately, the tolerance of the internal reference voltage can be improved to ±1.5% through MPU serial interface programming (refer to the Serial Interface section, Figure 130). The internal reference can be measured directly at the “VB” pin. During final test of the telephone, the VB internal reference voltage is measured. Then, the internal reference voltage value is adjusted electronically through the MPU serial interface to achieve the desired accuracy level. The voltage reference register value should be stored in ROM during final test so that it can be reloaded each time the combo IC is powered up. The Low Battery Detect outputs are open collector. The battery detect levels will depend on the accuracy of the VB voltage. Figure 12 indicates that the VB voltage is fairly flat over temperature.

Figure 2. Internal Low Battery Detect Levels (with VB = 1.5 V)

Battery Detect Select	Ramping Up (V)	Ramping Down (V)	Average (V)	Hysteresis (mV)
0	–	–	–	–
1	2.867	2.861	2.864	4.0
2	2.953	2.947	2.950	6.0
3	3.039	3.031	3.035	8.0
4	3.207	3.199	3.204	8.0
5	3.291	3.285	3.288	6.0
6	3.375	3.367	3.371	8.0
7	3.461	3.453	3.457	8.0

NOTE: 10. Battery Detect Select 0 is the non–programmable operating mode.

DC CURRENT

Figure 3. Current versus Supply Voltage Inactive Mode

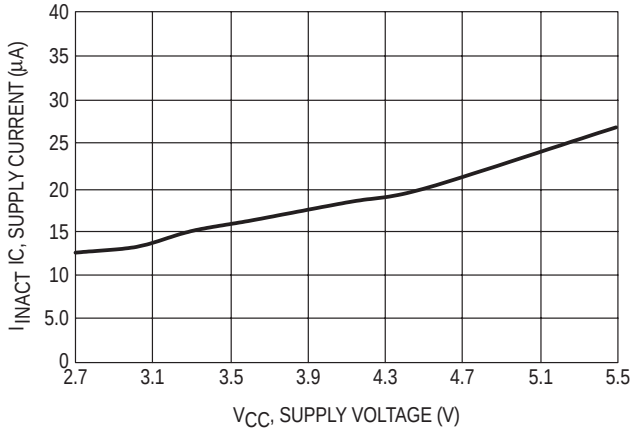


Figure 4. Current versus Supply Voltage Standby Mode, MCU Clock Output – On at 2.048 MHz

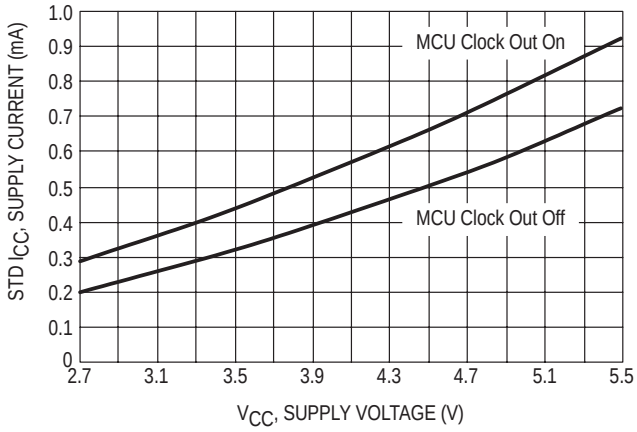


Figure 5. Current versus Supply Voltage Receive Mode

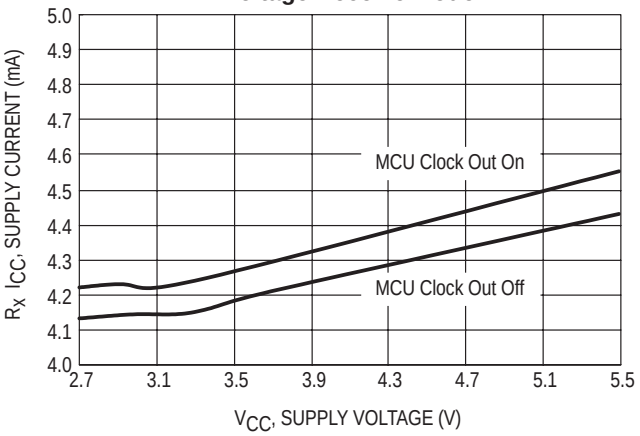


Figure 6. Current versus Supply Voltage Active Mode

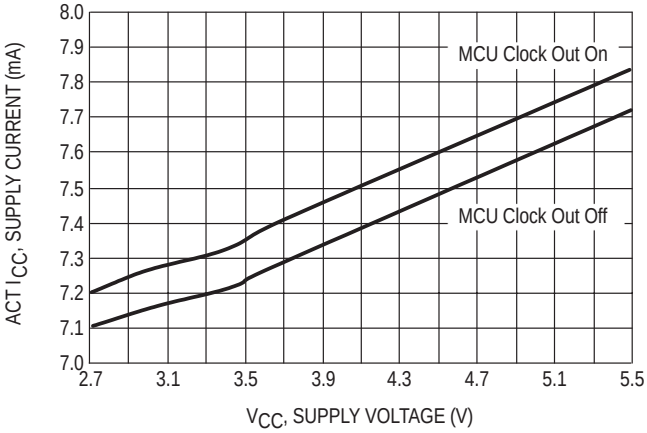


Figure 7. Current versus Temperature Normalized to 25°C

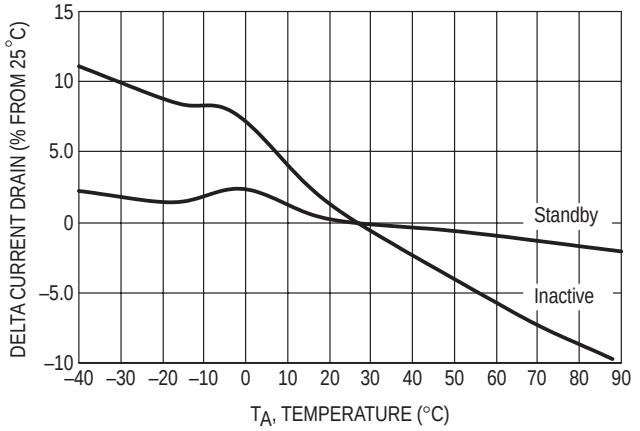
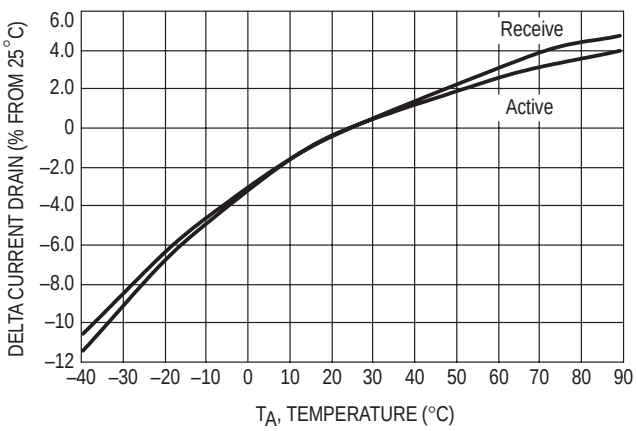


Figure 8. Current versus Temperature Normalized to 25°C



DC CURRENT

Figure 9. Additional Supply Current Consumption versus Supply Voltage, IP3 = <1>

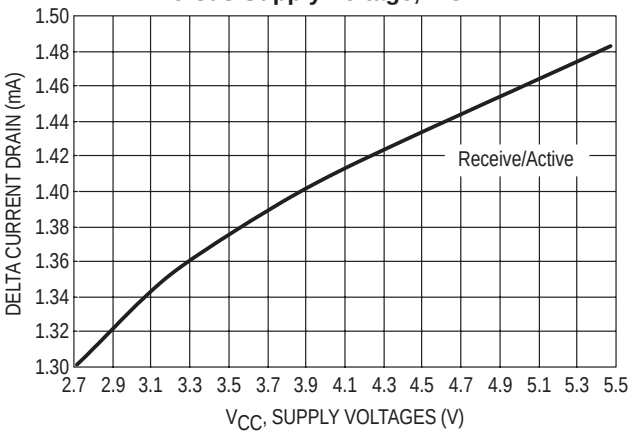


Figure 10. Additional IP3 Supply Current Consumption versus Temperature Normalized to 25°C

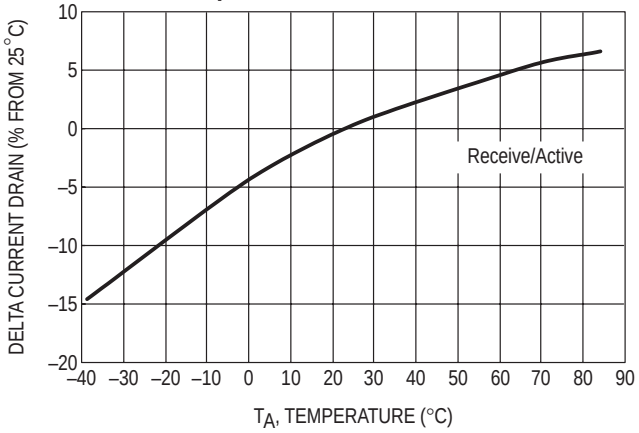


Figure 11. Current Standby Mode versus MCU Clock Output

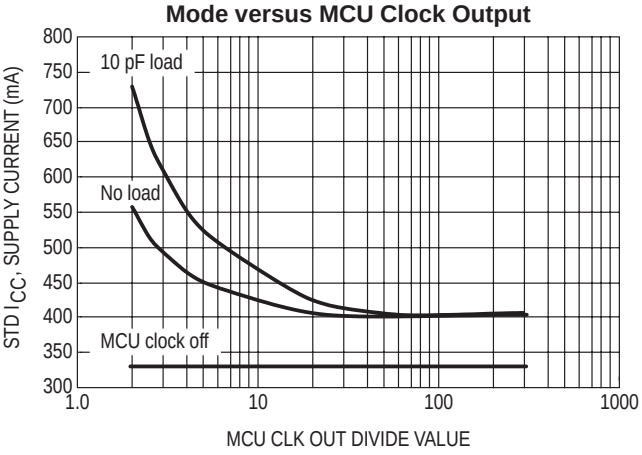
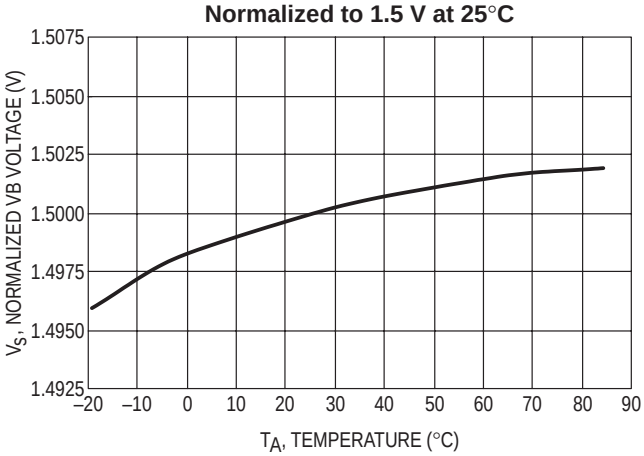


Figure 12. VB Voltage versus Temperature Normalized to 1.5 V at 25°C



Mixer Description

The 1st and 2nd mixers are similar in design. Both are double balanced to suppress the LO and the input frequencies to give only the sum and difference frequencies at the mixer output. Typically the LO is suppressed better than –50 dB for the first mixer and better than –40 dB for the second mixer. The gain of the 1st mixer has a –3.0 dB corner at approximately 13 MHz and is used at a 10.7 MHz IF. It has an output impedance of 300 Ω and matches to a typical 10.7 MHz ceramic filter with a source and load impedance of 330 Ω. A series resistor may be used to raise the impedance for use with crystal filters. They typically have an input impedance much greater than 330 Ω.

First Mixer

Figures 17 through 20 show the first mixer transfer curves for the voltage conversion gain, output level, and intermodulation. Notice that there is approximately 10 dB linearity improvement when the “IP3 Increase” bit is set to <1>. The “IP3 Increase” bit is a programmable bit as shown in the Serial Programmable Interface section under the R_X Counter Latch Register. The IP3 = <1> option will increase the supply current demand by 1.3 mA.

Figure 13. First Mixer Input and Output Impedance Schematic

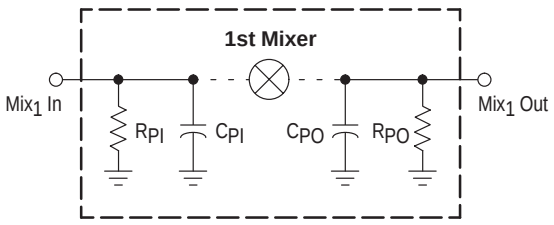


Figure 14. First Mixer Output Impedance

Unit	Output Impedance
B IP3 = <0> (Set Low)	304 Ω // 3.7 pF
B IP3 = <1> (Set High)	300 Ω // 4.0 pF

Figures 13, 14, and 16 represent the input and output impedance for the first mixer. Notice that the input single–ended and differential impedances are basically the same. The output impedance as described in Figure 14 will be used to match to a ceramic or crystal filter’s input impedance. A typical ceramic filter input impedance is 330 Ω while crystal filter input impedance is usually 1500 Ω. Exact impedance matching to ceramic filters are not critical, however, more attention needs to be given to the filter characteristics of a crystal filter. Crystal filters are much narrower. It is important to accurately match to these filters to guaranty a reasonable response.

To find the IF bandwidth response of the first mixer refer to Figure 22. The –3.0 dB bandwidth point is approximately 13 MHz. Figure 15 is a summary of the first mixer feedthrough parameters.

Figure 15. First Mixer Feedthrough Parameters

Parameter	(dBm)
1st LO Feedthrough @ Mix_1 In_1	–70.0
1st LO Feedthrough @ Mix_1 Out	–55.5
RF Feedthrough @ Mix_1 Out with –30 dBm	–61.0

Figure 16. First Mixer Input Impedance over Input Frequency

	US Center Channels		France Center Channels	
Unit	49 MHz	46 MHz	41 MHz	26 MHz
Single–Ended	1550 Ω // 3.7 pF	1560 Ω // 3.7 pF	1570 Ω // 3.8 pF	1650 Ω // 3.7 pF
Differential	1600 Ω // 1.8 pF	1610 Ω // 1.8 pF	1670 Ω // 1.8 pF	1710 Ω // 1.8 pF

NOTE: 11. Single–Ended data is from measured results. Differential data is from simulated results.

FIRST MIXER

Figure 17. First Mixer Voltage Conversion Gain, IP3_bit = 0

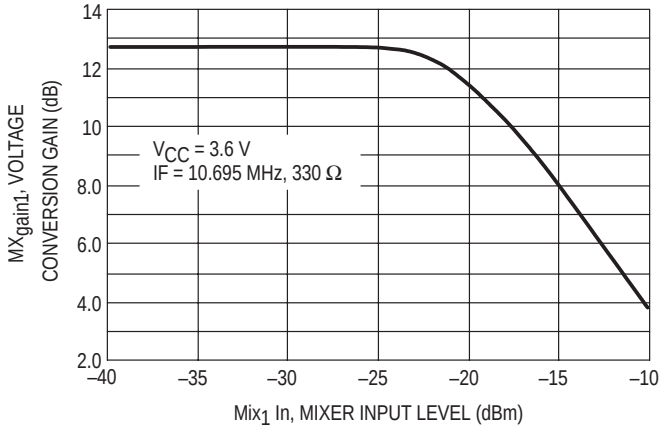


Figure 18. First Mixer Voltage Conversion Gain, IP3_bit = 1

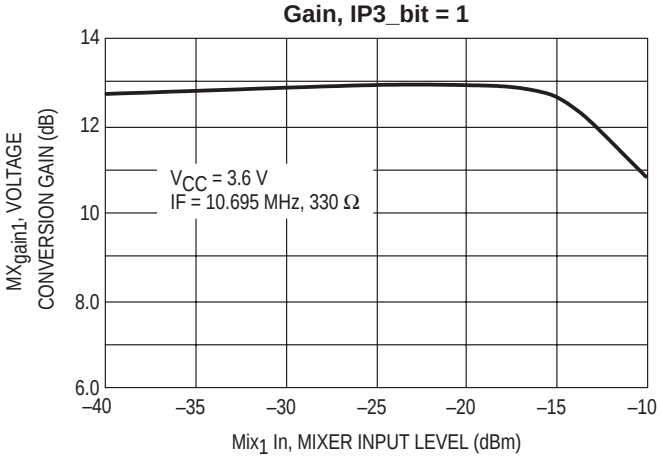


Figure 19. First Mixer Output Level and Intermodulation, IP3_bit = 0

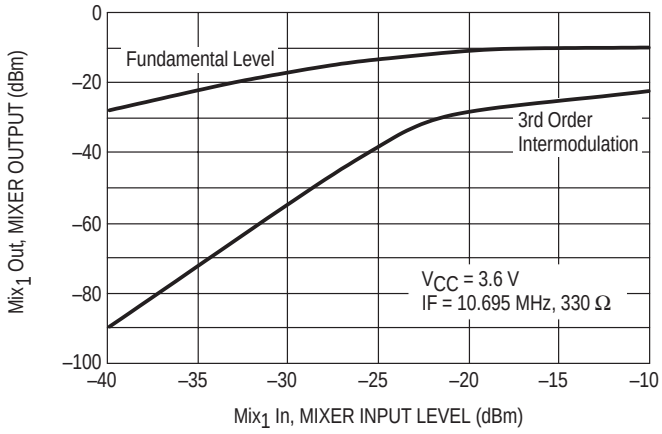


Figure 20. First Mixer Output Level and Intermodulation, IP3_bit = 1

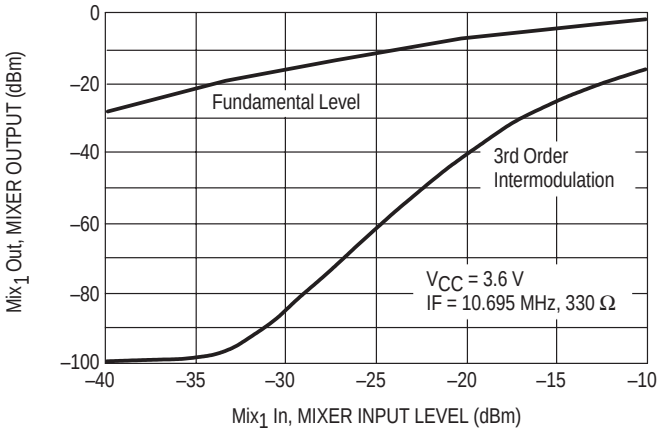


Figure 21. First Mixer Compression versus Supply Voltage

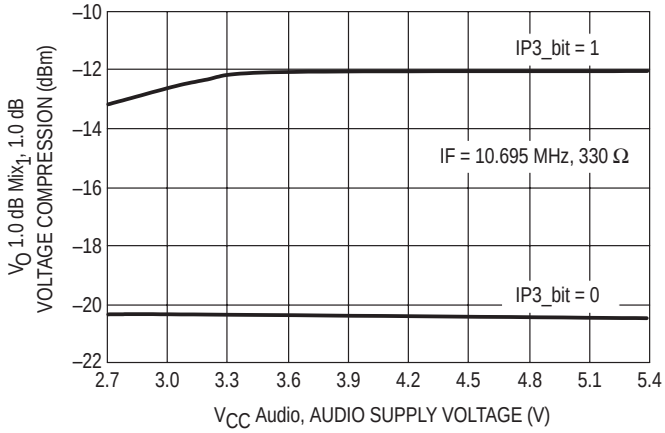
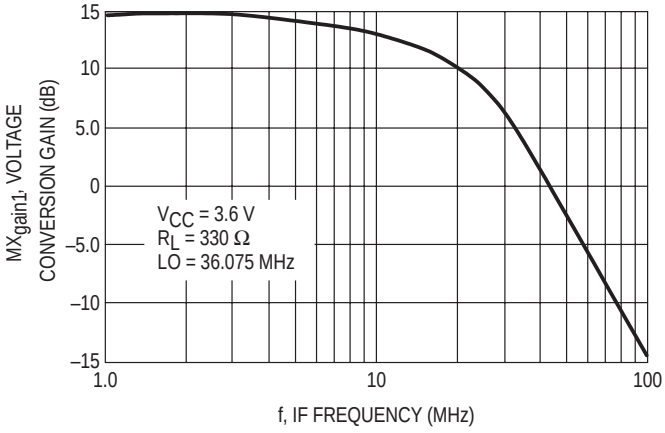


Figure 22. First IF Bandwidth



Second Mixer

Figures 26 through 29 represents the second mixer transfer characteristics for the voltage conversion gain, output level, and intermodulation. There is a slight improvement in gain when the “IP3 bit” is set to <1> for the second mixer. (Note: This is the same programmable bit discussed earlier in the section.)

Figure 23. Second Mixer Input and Output Impedance Schematic

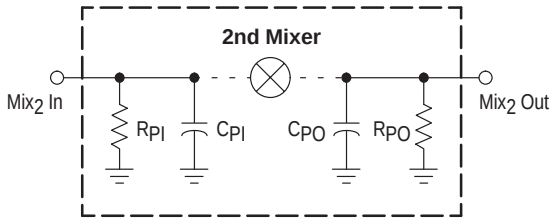


Figure 24. Second Mixer Input and Output Impedances

Unit	Input Impedance R_{PI} // C_{PI}	Output Impedance R_{PO} // C_{PO}
IP3 = <0> (Set Low)	2817 Ω // 3.6 pF	1493 Ω // 6.1 pF
IP3 = <1> (Set High)	2817 Ω // 3.6 pF	1435 Ω // 6.2 pF

The 2nd mixer input impedance is typically 2.8 kΩ. It requires an external 360 Ω parallel resistor for use with a standard 330 Ω, 10.7 MHz ceramic filter. The second mixer output impedance is 1.5 kΩ making it suitable to match standard 455 kHz ceramic filters.

The IF bandwidth response of the second mixer is shown in Figure 31. The –3.0 dB corner is 2.5 MHz. The feedthrough parameters are summarized in Figure 25.

Figure 25. Second Mixer Feedthrough Parameters

Parameter	(dBm)
2nd LO Feedthrough @ Mix_2 Out	–42.9
IF Feedthrough @ Mix_2 Out with –30 dBm	–61.7

SECOND MIXER

Figure 26. Second Mixer Conversion Gain, IP3_bit = 0

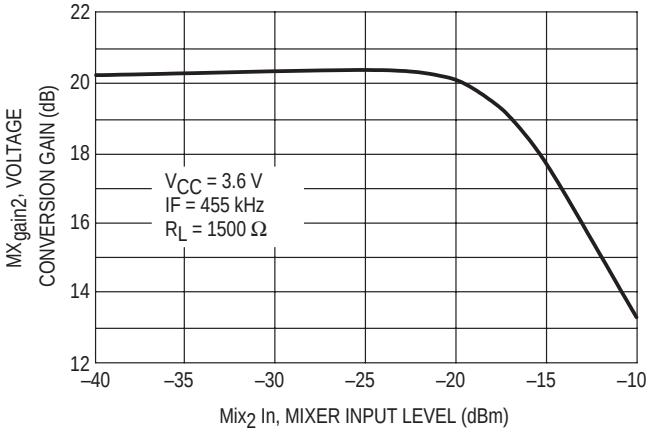


Figure 27. Second Mixer Conversion Gain, IP3_bit = 1

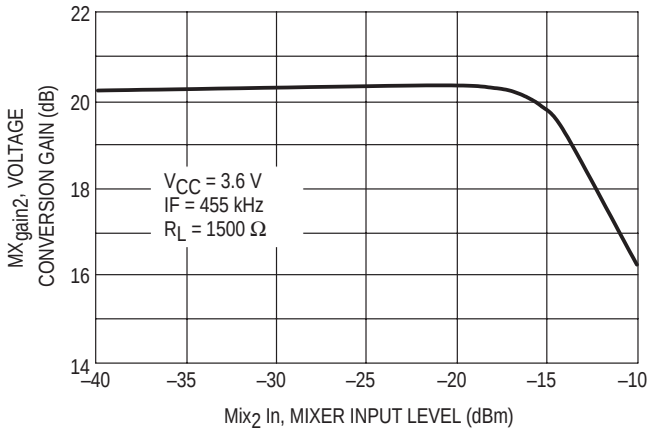


Figure 28. Second Mixer Output Level and Intermodulation, IP3_bit = 0

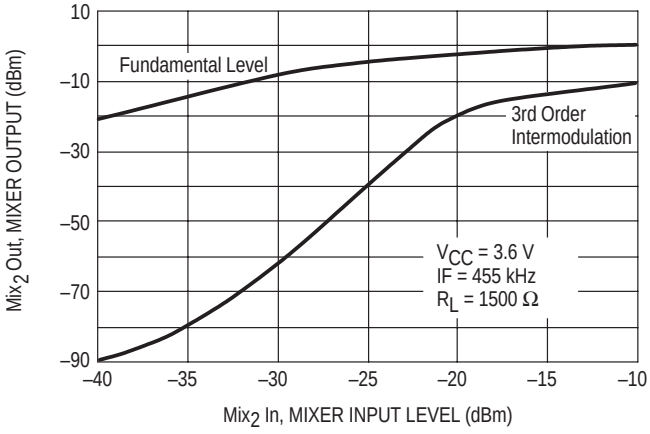


Figure 29. Second Mixer Output Level and Intermodulation, IP3_bit = 1

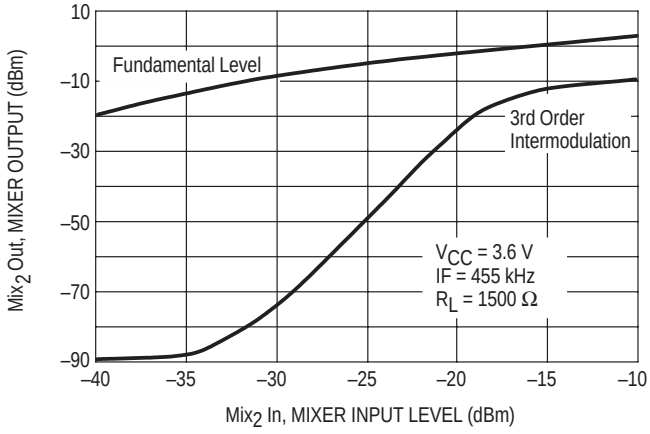


Figure 30. Second Mixer Compression versus Supply Voltage

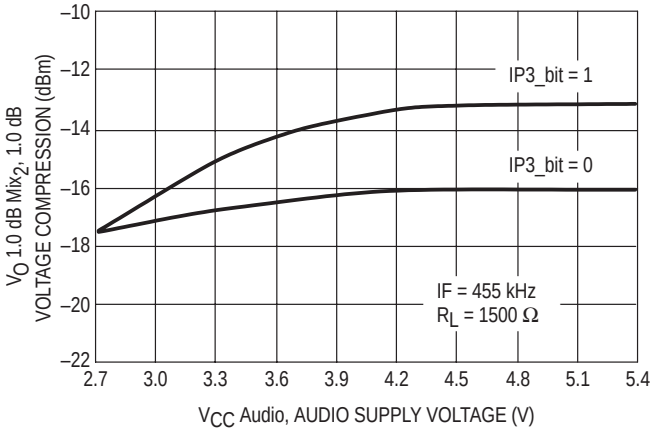
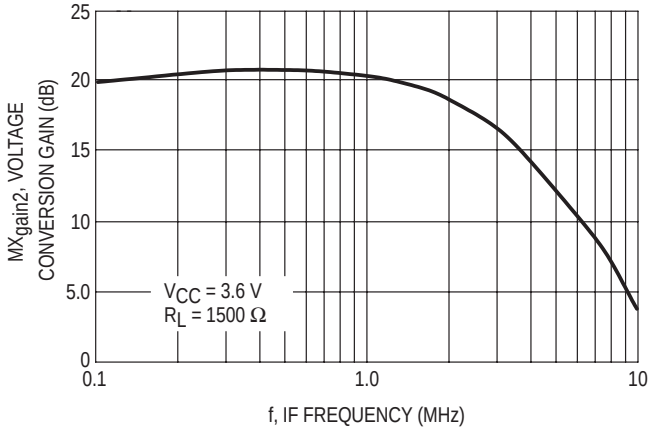


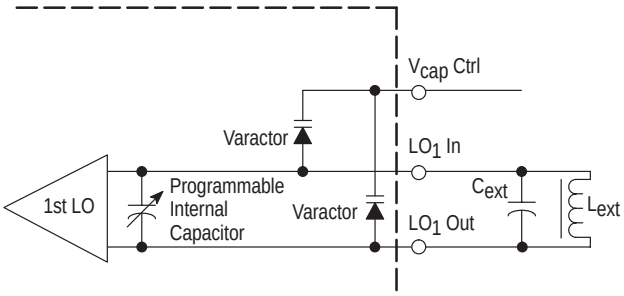
Figure 31. Second IF Bandwidth



First Local Oscillator

The 1st LO is a multi–vibrator oscillator. The tank circuit is composed of a parallel external capacitance and inductance, internal programmable capacitor matrix, and internal varactor. The local oscillator requires a voltage controlled input to the internal varactor and an external loop filter driven by on–board phase–lock control loop (PLL). The 1st LO internal component values have a tolerance of ±15%. A typical dc bias level on the LO Input and LO Output is 0.45 Vdc. The temperature coefficient of the varactor is +0.08%/°C. The curve in Figure 33 is the varactor control voltage range as it relates to varactor capacitance. It represents the expected internal capacitance for a given control voltage (V_{cap}Ctrl) of the MC13110A and MC13111A. Figure 32 shows a representative schematic of the first LO function.

Figure 32. First Local Oscillator Schematic



To select the proper L_{ext} and C_{ext} we can do the following analysis. From Figure 34 it is observed that an inductor will have a significant affect on first LO performance, especially over frequency. The overall minimum Q required for first LO to function as it relates to the LO frequency is also given in Figure 34.

Choose an inductor value, say 470 nH. From Figure 34, the minimum operating Q is approximately 25. From the following equation:

$$Q\ Coil = R_p/X\ Coil$$

where: R_p = parallel equivalent impedance (Figure 35).

C_{ext} can be determined as follows:

$$f_{LO} = \frac{1}{2\pi\sqrt{L_{ext}C_{ext}}}$$

where: L_{ext} = external inductance, C_{ext} = external capacitance.

Figure 34 clearly indicates that for lower coil values, higher quality factors (Q) are required for the first LO to function properly. Also, lower LO frequencies need higher Q's. In Figure 35 the internal programmable capacitor selection relative to the first LO frequency and the parallel impedance is shown. This information will help the user to decide what inductor (L_{ext}) to choose for best performance in terms of Q.

Refer to the Auxiliary Register in the Serial Interface Section for further discussion on LO programmability.

FIRST LOCAL OSCILLATOR

Figure 33. First LO Varicap Capacitance versus Control Voltage

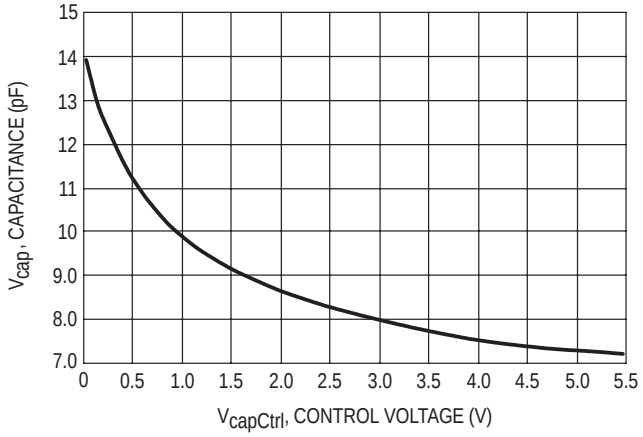


Figure 34. First LO Minimum Required Overall Q Value versus Inductor Value

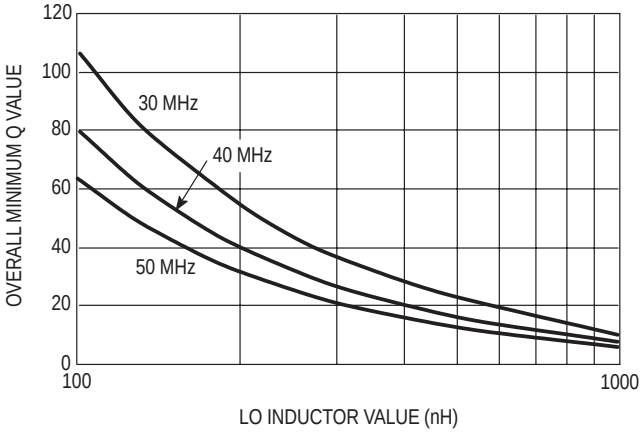


Figure 35. Representative Parallel Impedance versus Capacitor Select

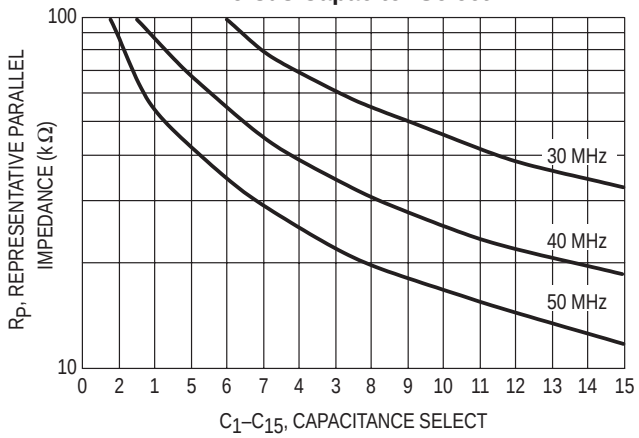


Figure 36. Varicap Value at V_{CV} = 1.0 V Over Temperature

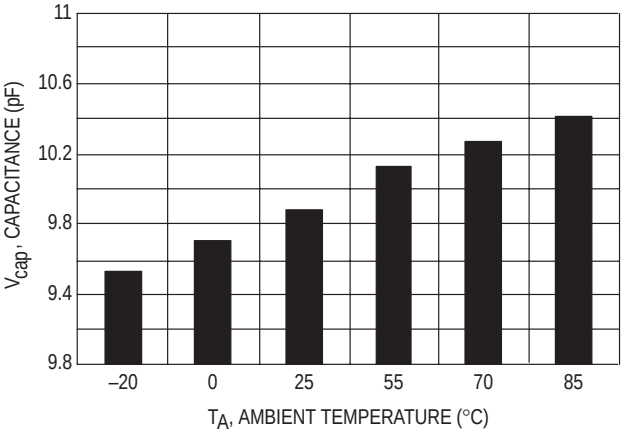


Figure 37. Control Voltage versus Channel Number, U.S. Handset Application

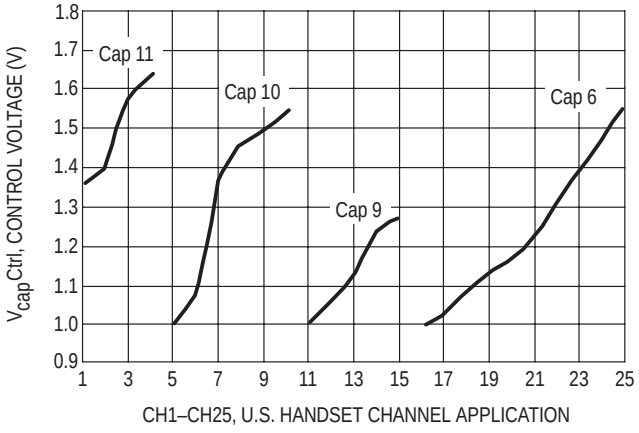
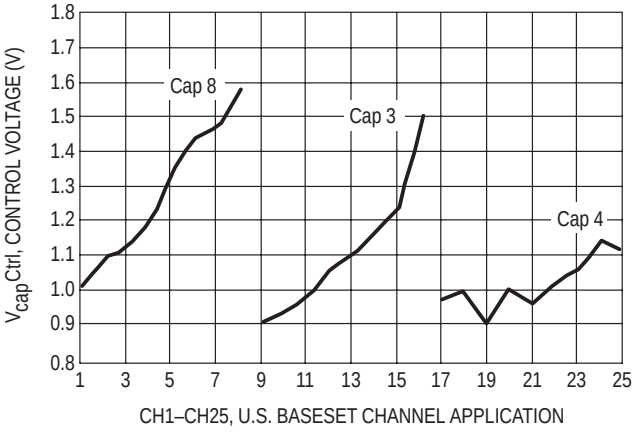


Figure 38. Control Voltage versus Channel Number, U.S. Baseset Application



Second Local Oscillator

The 2nd LO is a CMOS oscillator. It is used as the PLL reference oscillator and local oscillator for the second frequency conversion in the RF receiver. It is designed to utilize an external parallel resonant crystal. See schematic in Figure 39.

Figure 39. Second Local Oscillator Schematic

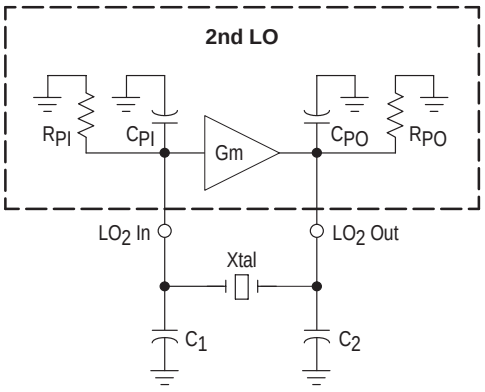


Figure 40. Second Local Oscillator Input and Output Impedance

Input Impedance (R_{PI} // C_{PI})	11.6 kΩ // 2.9 pF
Output Impedance (R_{PO} // C_{PO})	9.6 kΩ // 2.7 pF

Figure 41 shows a typical gain/phase response of the second local oscillator. Load capacitance (C_L), equivalent series resistance (ESR), and even supply voltage will have and affect on the 2nd LO response as shown in Figures 45 and 46. Except for the standby mode open loop gain is fairly constant as supply voltage increases from 2.5 V. This is due to the regulated voltage of 2.5 V on PLL V_{ref}. From the graphs it can seen that optimum performance is achieved when C1 equals C2 (C1/C2 = 1).

Figure 46 represents the ESR versus crystal load capacitance for the 2nd LO. This relationship was defined by using a 6.0 dB minimum loop gain margin at 3.6 V. This is considered the minimum gain margin to guarantee oscillator start–up.

Oscillator start–up is also significantly affected by the crystal load capacitance selection. In Figures 42 and 43 the relationship between crystal load capacitance, supply voltage, and external load capacitance ratio (C2/C1), can be seen. The lower the load capacitance the better the performance.

Given the desired crystal load capacitance, C1 and C2 can be determined from Figure 47. It is also interesting to point out that current consumption increases when C1 ≠ C2, as shown in Figure 44.

Be careful not to overdrive the crystal. This could cause a noise problem. An external series resistor on the crystal output can be added to reduce the drive level, if necessary.

SECOND LOCAL OSCILLATOR

Figure 41. Second LO Gain/Phase @ –10 dBm

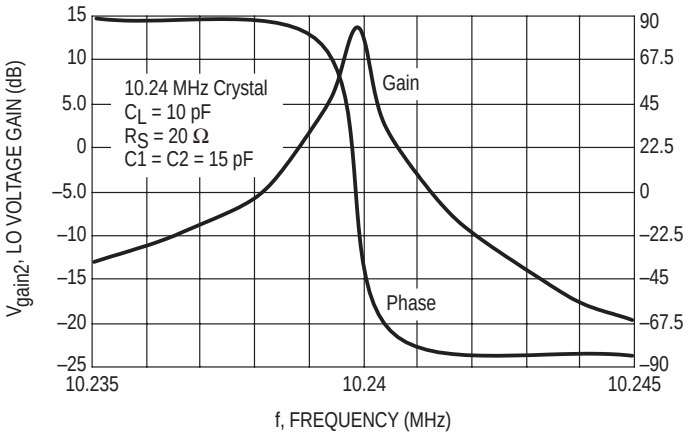
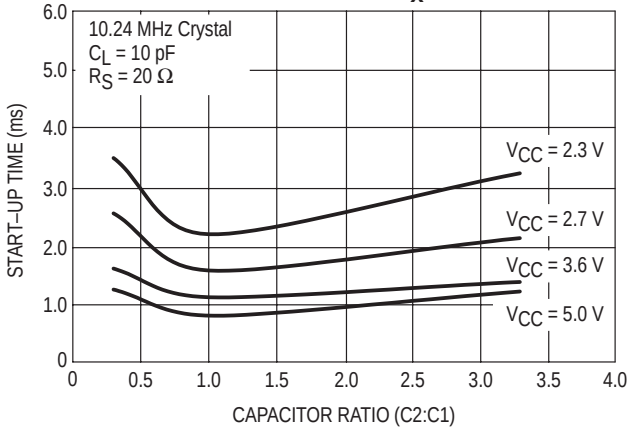


Figure 42. Start–Up Time versus Capacitor Ratio, Inactive to R_X Mode



SECOND LOCAL OSCILLATOR

Figure 43. Start–Up Time versus Capacitor Ratio, Inactive to R_X Mode

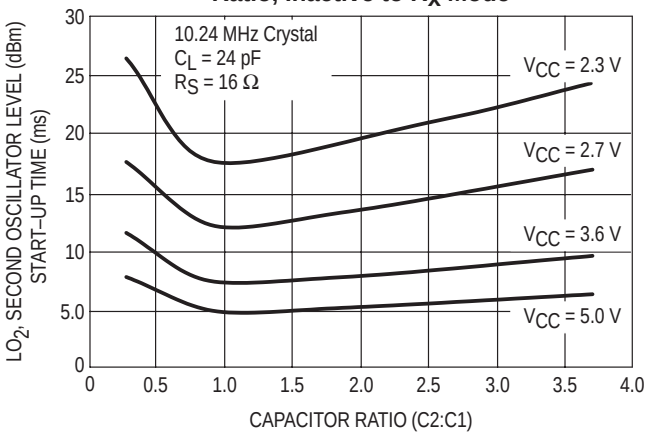


Figure 44. Second LO Current Consumption versus Capacitor Ratio

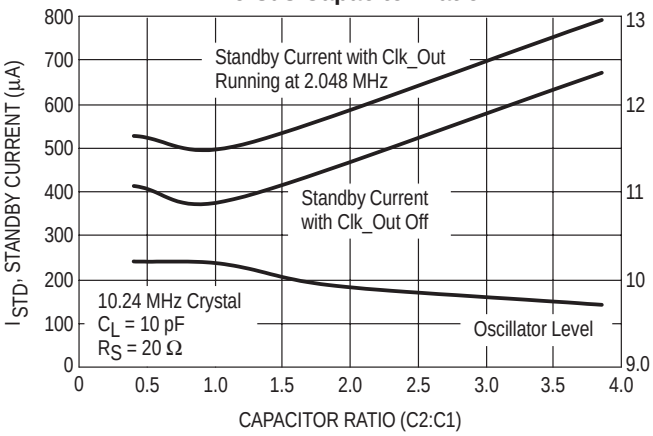


Figure 45. Maximum Open Loop Gain versus Capacitor Ratio

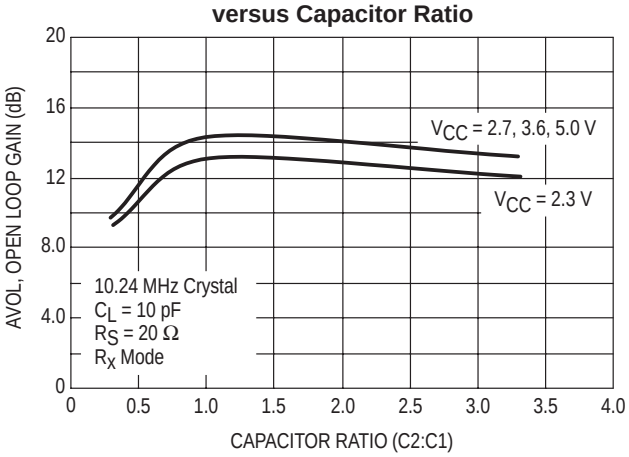


Figure 46. Maximum Allowable Equivalent Series Resistance (ESR) versus Crystal Load Capacitance

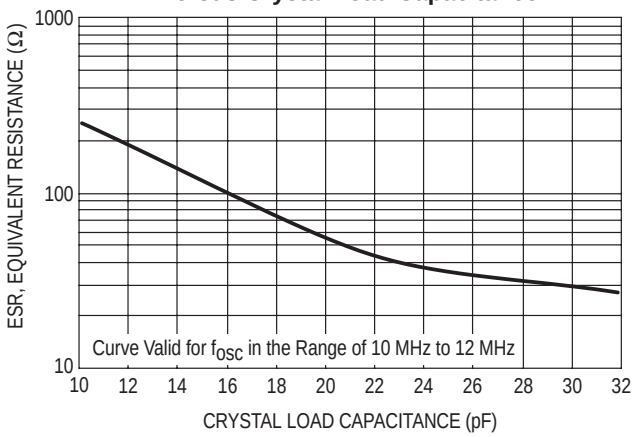
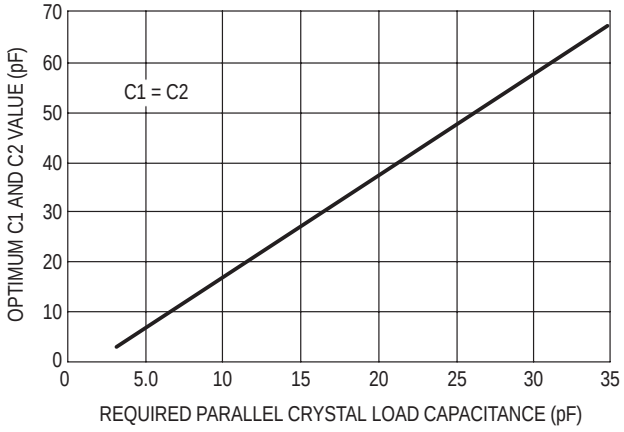


Figure 47. Optimum Value for C1 and C2 versus Equivalent Required Parallel Capacitance of the Crystal



IF Limiter and Demodulator

The limiting IF amplifier typically has about 110 dB of gain; the frequency response starts rolling off at 1.0 MHz. Decoupling capacitors should be placed close to Pins 31 and 32 to ensure low noise and stable operation. The IF input impedance is 1.5 kΩ. This is a suitable match to 455 kHz ceramic filters.

Figure 48. IF Limiter Schematic

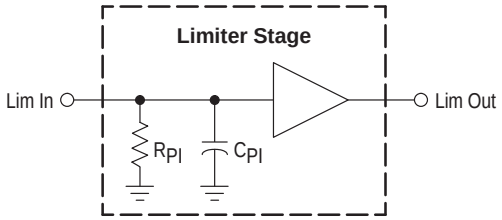
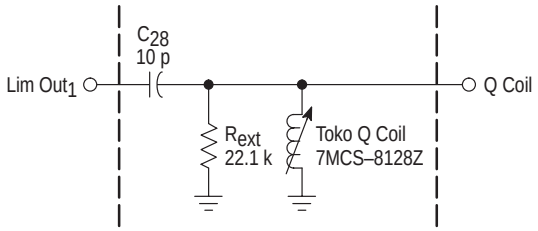


Figure 49. Limiter Input Impedance

Unit	Input Impedance (R_{PI})	Input Impedance (C_{PI})
Lim In	1538 Ω	15.7 pF

Figure 50. Quadrature Detector Demodulator Schematic



The quadrature detector is coupled to the IF with an external capacitor between Pins 27 and 28. Thus, the recovered signal level output is increased for a given bandwidth by increasing the capacitor. The external quadrature component may be either a LCR resonant circuit, which may be adjustable, or a ceramic resonator which is usually fixed tuned. (More on ceramic resonators later.)

The bandwidth performance of the detector is controlled by the loaded Q of the LC tank circuit (Figure 50). The following equation defines the components which set the detector circuit's bandwidth:

(1) $R_T = Q\ X_L$,

where R_T is the equivalent shunt resistance across the LC tank. X_L is the reactance of the quadrature inductor at the IF frequency ($X_L = 2\pi\ f\ L$).

The 455 kHz IF center frequency is calculated by:

(2) $f_C = [2\pi\ (L\ Cp)^{1/2}] - 1$

where L is the parallel tank inductor. Cp is the equivalent parallel capacitance of the parallel resonant tank circuit.

The following is a design example for a detector at 455 kHz and a specific loaded Q:

The loaded Q of the quadrature detector is chosen somewhat less than the Q of the IF bandpass for margin. For an IF frequency of 455 kHz and an IF bandpass of 20 kHz, the IF bandpass Q is approximately 23; the loaded Q of the quadrature tank is chosen slightly lower at 15.

Example:

Let the total external C = 180 pF. (Note: the capacitance is the typical capacitance for the quad coil.) Since the external capacitance is much greater than the internal device and PCB parasitic capacitance, the parasitic capacitance may be neglected.

Rewrite equation (2) and solve for L:

$L = (0.159)^2/(C\ f_c^2)$
L = 678 μH ; Thus, a standard value is chosen:
L = 680 μH (surface mount inductor)

The value of the total damping resistor to obtain the required loaded Q of 15 can be calculated from equation (1):

$R_T = Q(2\pi\ f\ L)$
$R_T = 15(2\pi)(0.455)(680) = 29.5\ k\Omega$

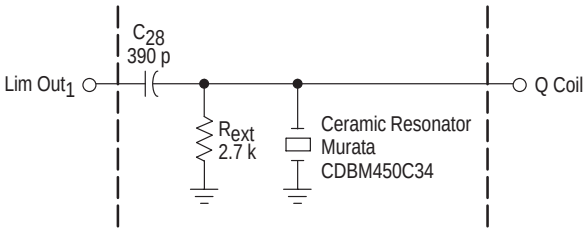
The internal resistance, R_{int} at the quadrature tank Pin 27 is approximately 100 kΩ and is considered in determining the external resistance, R_{ext} which is calculated from:

$R_{ext} = ((R_T)(R_{int}))/(R_{int} - R_T)$
R_{ext} = 41.8 kΩ;Thus, choose a standard value:
R_{ext} = 39 kΩ

In Figure 50, the R_{ext} is chosen to be 22.1 kΩ. An adjustable quadrature coil is selected. This tank circuit represents one popular network used to match to the 455 kHz carrier frequency. The output of the detector is represented as a "S–curve" as shown in Figure 52. The goal is to tune the inductor in the area that is most linear on the "S–curve" (minimum distortion) to optimize the performance in terms of dc output level. The slope of the curve can also be adjusted by choosing higher or lower values of R_{ext}. This will have an affect on the audio output level and bandwidth. As R_{ext} is increased the detector output slope will decrease. The maximum audio output swing and distortion will be reduced and the bandwidth increased. Of course, just the opposite is true for smaller R_{ext}.

A ceramic discriminator is recommended for the quadrature circuit in applications where fixed tuning is desired. The ceramic discriminator and a 5.6 kΩ resistor are placed from Pin 27 to V_{CC}. A 22 pF capacitor is placed from Pin 28 to 27 to properly drive the discriminator. MuRata Erie has designed a resonator for this part (CDBM455C48 for USA & A/P regions and CDBM450C48 for Europe). This resonator has been designed specifically for the MC13110/111 family. Figure 51 shows the schematic used to generate the "S–curve" and waveform shown in Figure 54 and 55.

Figure 51. Ceramic Resonator Demodulator Schematic with Murata CDBM450C48



(CDBM455C48 US; CDBM450C48 France)

The “S–curve” for the ceramic discriminator shown in Figure 54 is centered around 450 kHz. It is for the French application. The same resonator is also used for the US application and is centered around 455 kHz. Clearly, the “S–curves” for the resonator and quad coil have very similar limiter outputs. As discussed previously, the slope of the “S–curve” centered around the center frequency can be controlled by the parallel resistor, R_{ext}. Distortion, bandwidth, and audio output level will be affected.

IF LIMITER AND DEMODULATION

Figure 52. S–Curve of Limiter Discriminator with Quadrature Coil

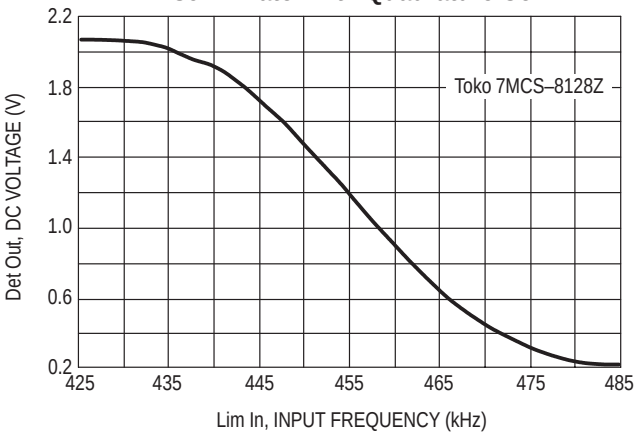


Figure 53. Typical Limiter Output Waveform with Quadrature Coil

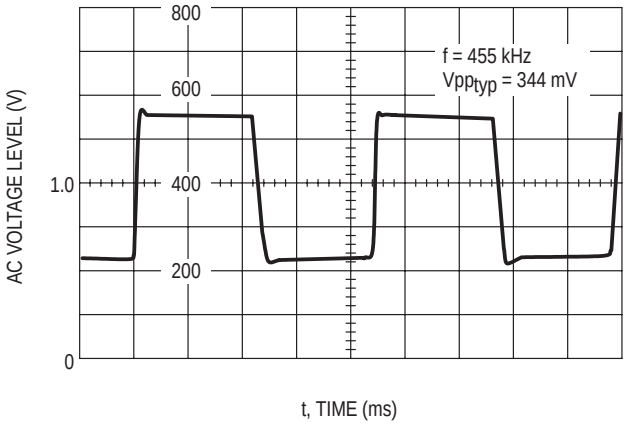


Figure 54. S–Curve of Limiter Discriminator with Ceramic Resonator

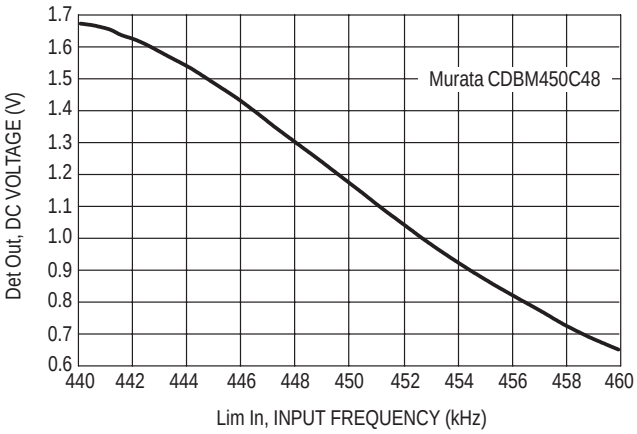
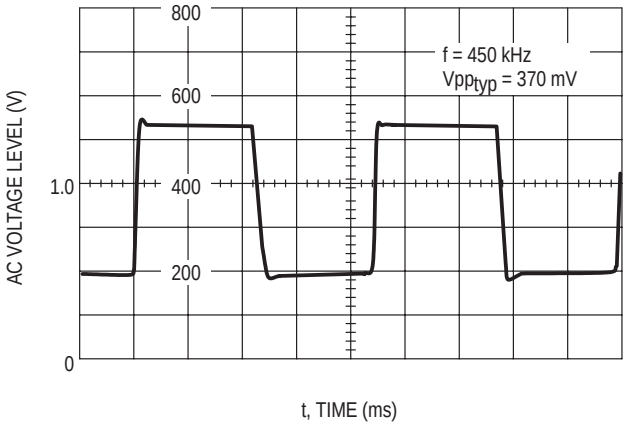


Figure 55. Typical Limiter Output Waveform with Ceramic Resonator



RSSI and Carrier Detect

The Received Signal Strength Indicator (RSSI) indicates the strength of the IF level. The output is proportional to the logarithm of the IF input signal magnitude. RSSI dynamic range is typically 80 dB. A 187 kΩ resistor to ground is provided internally to the IC. This internal resistor converts the RSSI current to a voltage level at the “RSSI” pin. To improve the RSSI accuracy over temperature an internal compensated reference is used. Figure 56 shows the RSSI versus RF input. The slope of the curve is 16.5 mV/dB.

The Carrier Detect Output (CD Out) is an open–collector transistor output. An external pull–up resistor of 100 kΩ will be required to bias this device. To form a carrier detect filter a capacitor needs to be connected from the RSSI pin to ground. The carrier detect threshold is programmable through the MPU interface (see “Carrier Detect Threshold Programming” in the serial interface section). The range can be scaled by connecting additional external resistance from the RSSI pin to ground in parallel with the capacitor. From Figure 57, the affect of an external resistor at RSSI on the carrier detect level can be noticed. Since there is hysteresis in the carrier detect comparator, one trip level can be found when the input signal is increased while the another one can be found when the signal is decreased.

Figure 58 represents the RSSI ripple in relation to the RF input for different filtering capacitors at RSSI. Clearly, the higher the capacitor, the less the ripple. However, at low carrier detect thresholds, the ripple might supersede the hysteresis of the carrier detect. The carrier detect output may appear to be unstable. Using a large capacitor will help to stabilize the RSSI level, but RSSI charge time will be affected. Figure 59 shows this relationship.

The user must decide on a compromise between the RSSI ripple and RSSI start–up time. Choose a 0.01 μf capacitor as a starting point. For low carrier detect threshold settings, a 0.047 μf capacitor is recommended.

RSSI AND CARRIER DETECT

Figure 56. Typical RSSI Voltage Level versus RF Input

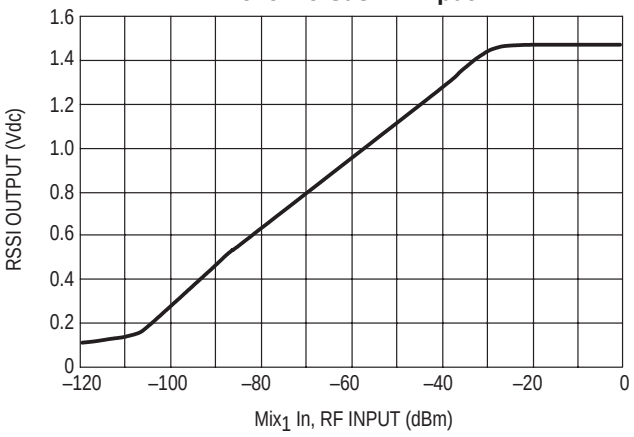


Figure 57. Carrier Detect Threshold versus External RSSI Resistor

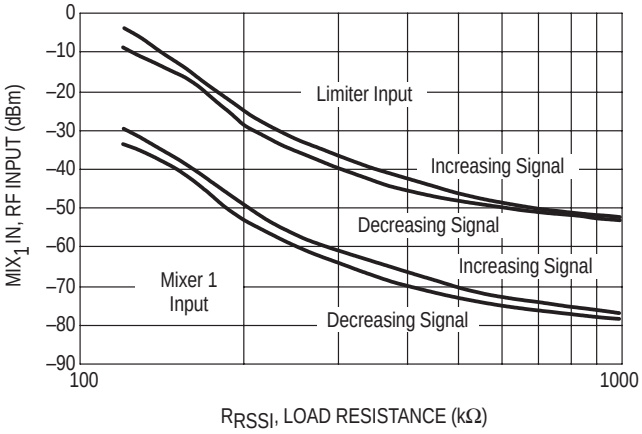


Figure 58. RSSI Ripple versus RF Input Level for Different RSSI Capacitors

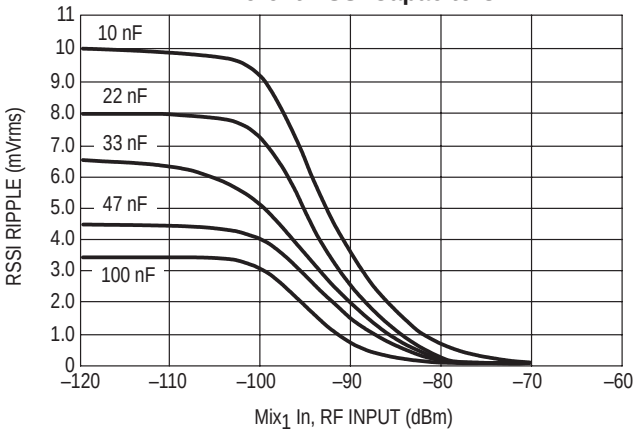
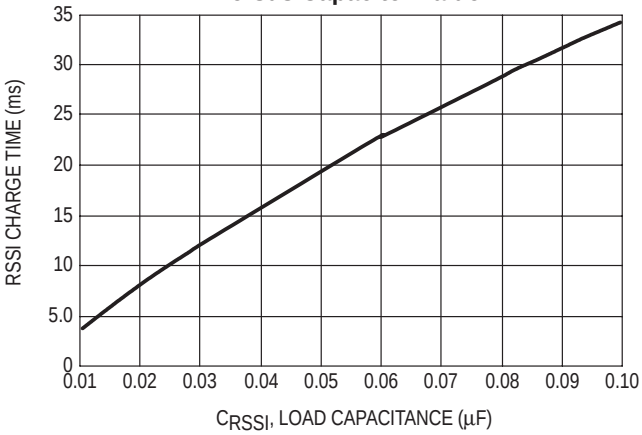


Figure 59. RSSI Charge Time versus Capacitor Value



RF System Performance

The sensitivity of the IC is typically 0.4 μVrms matched (single ended or differential) with no preamp. To achieve suitable system performance, a preamp and passive duplexer may be used. In production final test, each section of the IC is separately tested to guarantee its system performance in the specific application. The preamp and duplexer (differential, matched input) yields typically –115 dBm @ 12 dB SINAD sensitivity performance under full duplex operation. See Figure 45 and 48.

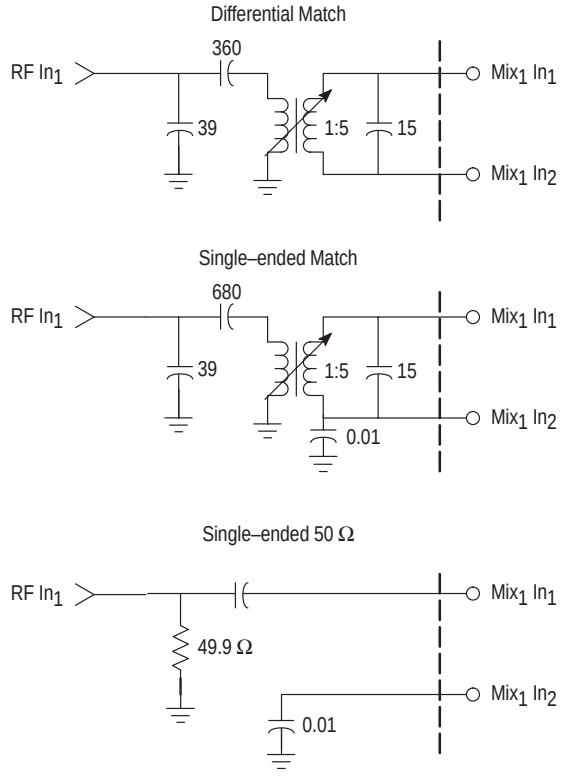
The duplexer is important to achieve full duplex operation without significant “de–sensing” of the receiver by the transmitter. The combination of the duplexer and preamp circuit should attenuate the transmitter power to the receiver by over 60 dB. This will improve the receiver system noise figure without giving up too much IMD performance.

The duplexer may be a two piece unit offered by Shimida, Sansui, or Toko products (designed for 25 channel CT–0 cordless phone). The duplexer frequency response at the receiver port has a notch at the transmitter frequency band of about 35 to 40 dB with a 2.0 to 3.0 dB insertion loss at the receiver frequency band.

The preamp circuit utilizes a tuned transformer at the output side of the amplifier. This transformer is designed to bandpass filter at the receiver input frequency while rejecting the transmitter frequency. The tuned preamp also improves the noise performance by reducing the bandwidth of the pass band and by reducing the second stage contribution of the 1st mixer. The preamp is biased such that it yields suitable noise figure and gain.

The following matching networks have been used to obtain 12 dB SINAD sensitivity numbers:

Figure 60. Matching Input Networks



The exact impedance looking into the RF In1 pin is displayed in the following table along with the sensitivity levels.

Figure 61. 12 dB SINAD Sensitivity Levels, US Handset Application Channel 21

	Sensitivity (dBm)	Input Impedance (dBm)
Differential matched	–115.3	50.2 ± 0.1j
Single–ended match	–114.8	50.2 ± 0.1j
Single–ended 50 Ω	–100.1	50.2 ± 0.1j

The graphs in Figures 64 to 69 are performance results based on Evaluation Board Schematic (Figure 137). This evaluation board did not use a duplexer or preamp stage. Figure 62 is a summary of the RF performance and Figure 63 contains the French RF Performance Summary.

Figure 62. RF Performance Summary for US Applications

MC13110A/MC13111A (fdev = 3.0 kHz, fmod = 1.0 kHz, 50 Ω)			
Parameter	**Handset**	**Baseset**	**Unit**
Sensitivity at 12 dB SINAD	–100.1	–100.1	dBm
Recovered Audio	132	132	mVrms
SINAD @ –30 dBm	41.8	41.4	dB
THD @ –30 dBm	0.8	0.8	%
S/N @ –30 dBm	78.2	78.5	dB
AMRR @ –30 dBm	73.4	72.2	dB
RSSI range	>80	>80	dB

Figure 63. RF Performance Summary for US French Applications

MC13110A/MC13111A (fdev = 1.5 kHz, fmod = 1.0 kHz, 50 Ω)			
Parameter	**Handset**	**Baseset**	**Unit**
Sensitivity at 12 dB SINAD	–91	–90.8	dBm
Recovered Audio	89.8	90	mVrms
SINAD @ –30 dBm	42.1	44.3	dB
THD @ –30 dBm	0.8	0.8	%
S/N @ –30 dBm	75.7	75.1	dB
AMRR @ –30 dBm	56	84.7	dB
RSSI range	>80	>80	dB

RF SYSTEM PERFORMANCE

Figure 64. Typical Receiver Performance Parameters U.S. Handset Application Channel 21

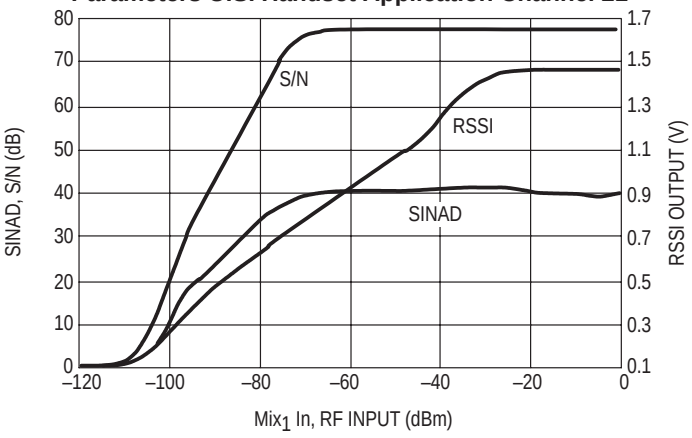


Figure 65. Typical Performance Parameters Over U.S. Handset Channel Frequencies

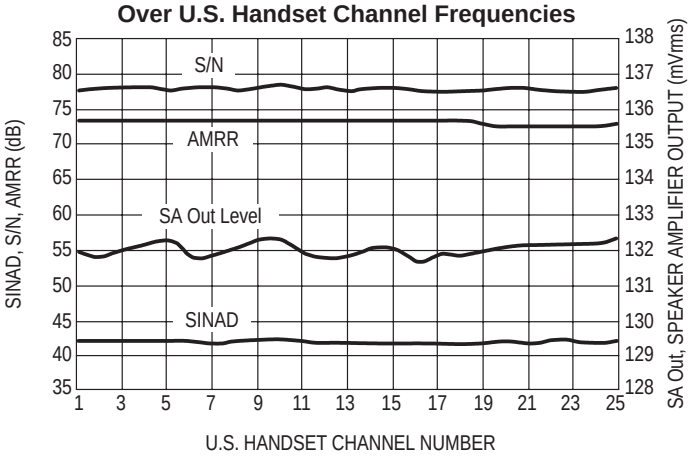


Figure 66. Typical Performance Parameters Over U.S. Baseset Channel Frequencies

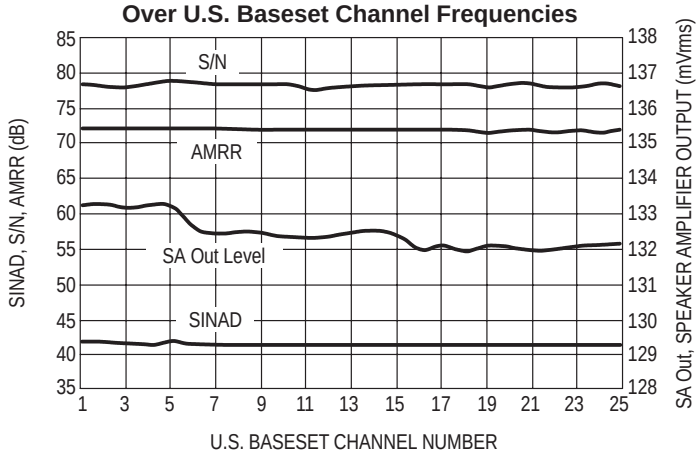


Figure 67. Typical Receiver Performance for US Handset Application Channel 21

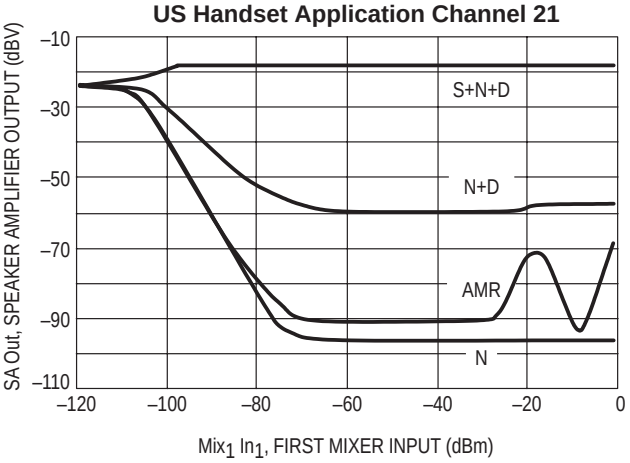


Figure 68. 12 dB SINAD Sensitivity Over US Handset Application Channels

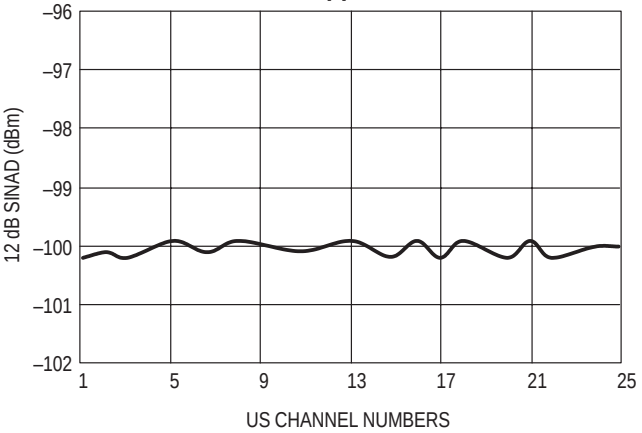
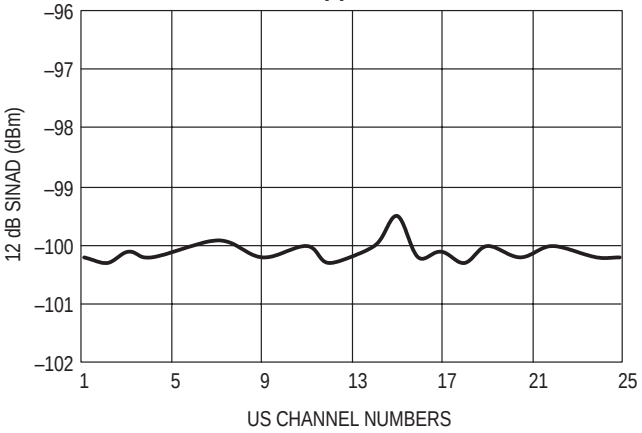


Figure 69. 12 dB SINAD Sensitivity Over US Baseset Application Channels



Receive Audio Path

The R_X Audio signal path begins at “Rx Audio In” and goes through the IC to “E Out”. The “R_X Audio In”, “Scr Out”, and “E In” pins are all ac–coupled. This signal path consists of filters; programmable R_X gain adjust, R_X mute, and volume control, and finally the expander. The typical maximum output voltage at “E Out” should be approximately 0 dBV @ THD = 5.0% .

Figures 71 to 73 represent the receive audio path filter response. The filter response attenuation is very sharp above 3900 Hz, which is the cutoff frequency. Inband (audio), out–of–band, and ripple characteristics are also shown in these graphs.

The group delay (Figure 75) has a peak around 6.5 kHz. This spike is formed by rapid change in the phase at the frequency. In practice this does not cause a problem since the signal is attenuated by at least 50 dB.

The output capability at “Scr Out” and “E Out” are shown in Figures 76, 77, and 78. The results were obtained by increasing the input level for 2.0% distortion at the outputs.

In Figure 70, noise data for the R_X audio path is shown. At Scr Out, the noise level clearly rises when the scrambler is enabled. However, assuming a nominal output level of –20 dBV (100 mVrms) at the 0 dB gain setting, the noise floor is more than 56 dB below the audio signal. However, the noise data at E Out and SA Out is much more improved.

Speaker Amp

The Speaker Amp is an inverting rail–to–rail operational amplifier. The noninverting input is connected to the internal VB reference. External resistors and capacitors are used to set the gain and frequency response. The “SA In” input pin must be ac–coupled. The typical output voltage at “SA Out” is 2.6 V_{pp} with a 130 Ω load. The speaker amp response is shown in Figures 79 and 80.

Data Amp Comparator

The data amp comparator is an inverting hysteresis comparator. Its open collector output has an internal 100 kΩ pull–up resistor. A band pass filter is connected between the “Det Out” pin and the “DA In” pin with component values as shown in the Application Circuit schematic. The “DA In” input signal needs to be ac–coupled, too.

Figure 70. R_X Path Noise Data

Receive Scrambler	Receive Gain (dB)	Volume (dB)	SCR_Out (dBV)	E_Out (dBV)	SA_Out (dBV)
off/on	muted	muted	< –95	< –95	< –95
off	–9.0	–14	–92	< –95	< –95
off	0	0	–85	< –95	< –95
off	1.0	16	–76	< –95	< –95
on (MC13110A)	–9.0	–14	–85	< –95	< –95
on (MC13110A)	0	0	–77	< –95	< –95
on (MC13110A)	10	16	–66	< –95	< –95

R_X AUDIO

Figure 71. R_X Audio Wideband Frequency Response

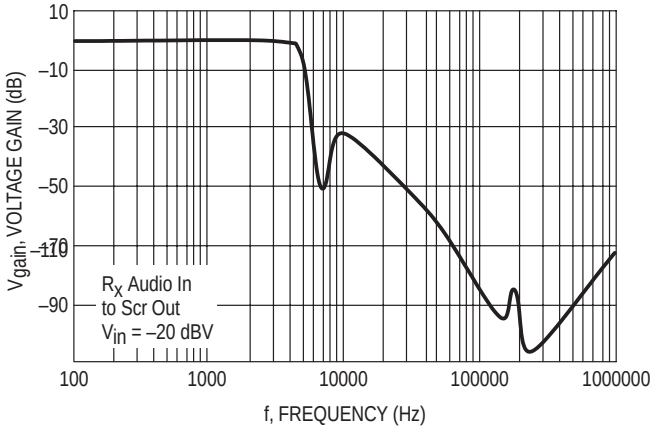


Figure 72. R_X Audio Inband Frequency Response

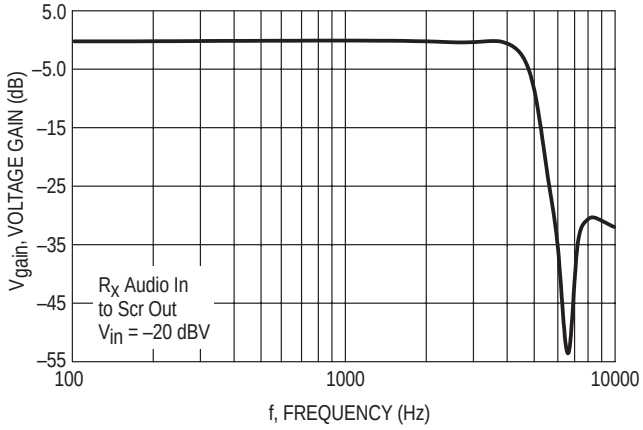


Figure 73. R_X Audio Ripple Response

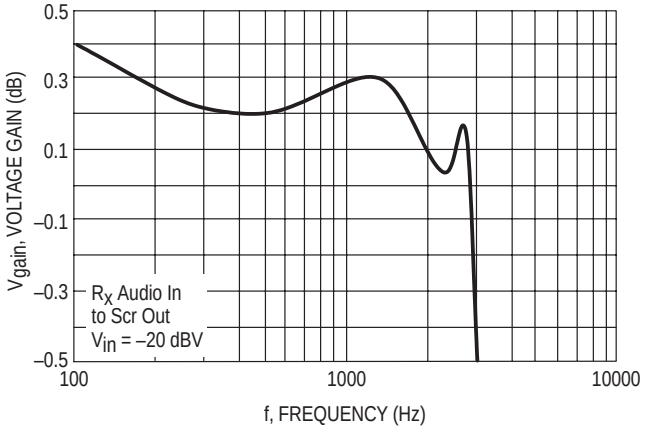


Figure 74. R_X Audio Inband Phase Response

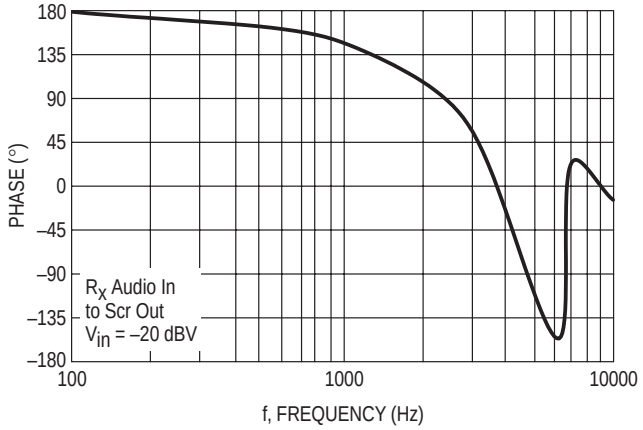


Figure 75. R_X Audio Inband Group Delay

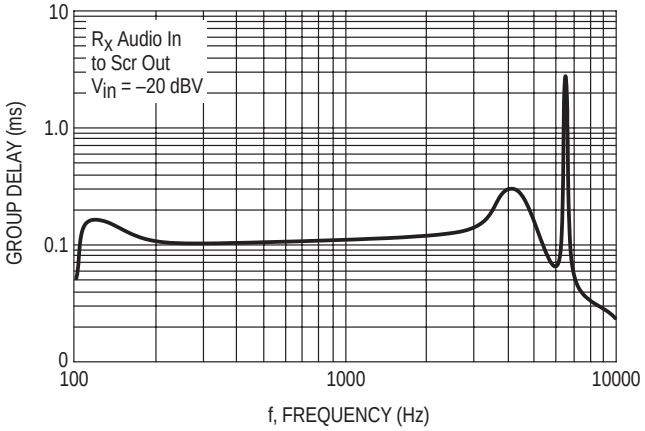
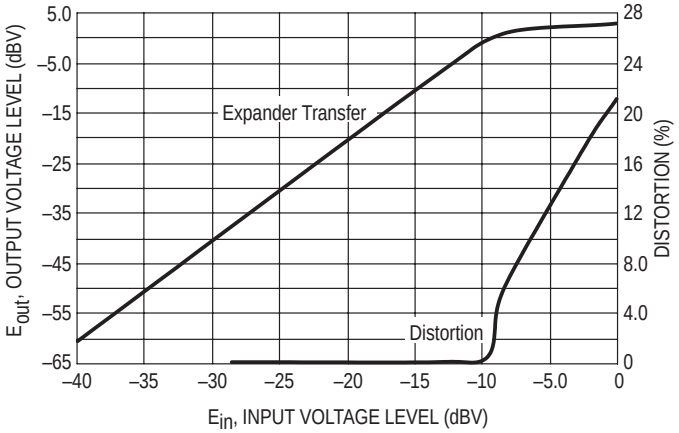


Figure 76. R_X Audio Expander Response



R_X AUDIO

Figure 77. R_X Audio Maximum Output Voltage versus Gain Control Setting

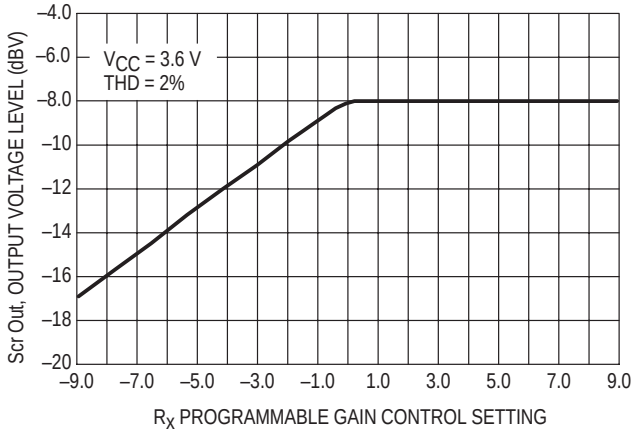


Figure 78. R_X Audio Maximum Output Voltage versus Volume Setting

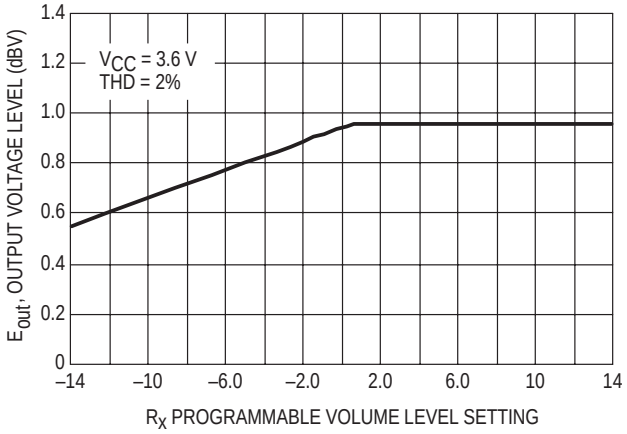


Figure 79. R_X Audio Speaker Amplifier Drive

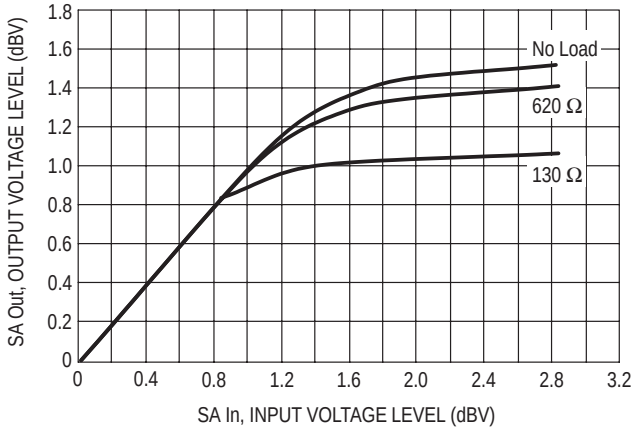
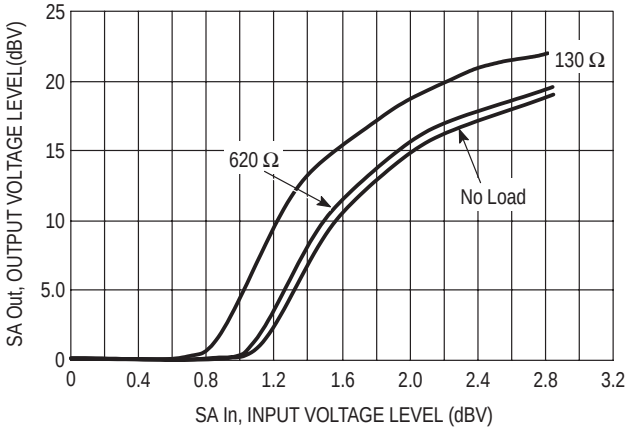


Figure 80. R_X Audio Speaker Amplifier Distortion



Transmit Audio Path

This portion of the audio path goes from “C In” to “T_X Out”. The “C In” pin will be ac–coupled. The audio transmit signal path includes automatic level control (ALC) (also referred to as the Compressor), T_X mute, limiter, filters, and T_X gain adjust. The ALC provides “soft” limiting to the output signal swing as the input voltage slowly increases. With this technique the gain is slightly lowered to help reduce distortion of the audio signal. The limiter section provides hard limiting due to rapidly changing signal levels, or transients. This is accomplished by clipping the signal peaks. The ALC, T_X mute, and limiter functions can be enabled or disabled via the MPU serial interface. The T_X gain adjust can also be remotely controlled to set different desired signal levels. The typical maximum output voltage at “T_X Out” should be approximately 0 dBV @ THD = 5.0%.

Figures 82 to 86 represent the transmit audio path filter response. The filter response attenuation, again, is very definite above 3800 Hz. This is the filter cutoff frequency. Inband (audio), wideband, and ripple characteristics are also shown in these graphs.

The compressor transfer characteristics, shown in Figure 87, has three different slopes. A typical compressor slope can be found between –55 and –15 dBV. Here the slope is 2.0. At an input level above –15 dBV the automatic level control (ALC) function is activated and prevents hard clipping of the output. The slope below –55 dBV input level is one. This is where the compressor curve ends. Above 5.0 dBV the output actually begins to decrease and distort. This is due to supply voltage limitations.

In Figure 88 the ALC function is off. Here the compressor curve continues to increase above –15 dBV up to –4.0 dBV. The limiter begins to clip the output signal at this level and distortion is rapidly rising. Similarly, Figure 68 (ALC and Limiter Off) shows to compressor transfer curve extending all the way up to the maximum output. Finally, Figure 90 through 93 show the T_X Out signal versus several combinations of ALC and Limiter selected.

Figure 81 is the noise data measured for the MC13110A/13111A. This data is for 0 dB gain setting and –20 dBV (100 mVrms) audio levels.

Figure 81. T_X Path Noise Data

Transmit Scrambler	Transmit Gain (dB)	Amp_Out (dBV)	T_X_Out (dBV)
off/on	muted	muted	< –95
off	–9.0	< –95	–83
off	0	< –95	–74
off	10	< –95	–64
on (MC13110A)	–9.0	< –95	–82
on (MC13110A)	0	< –95	–73
on (MC13110A)	10	–< –95	–63

Mic Amp

Like the Speaker Amp the Mic Amp is also an inverting rail–to–rail operational amplifier. The noninverting input terminal is connected to the internal VB reference. External resistors and capacitors are used to set the gain and frequency response. The “T_X In” input is ac–coupled.

T_X AUDIO

Figure 82. T_X Audio Wideband Frequency Response

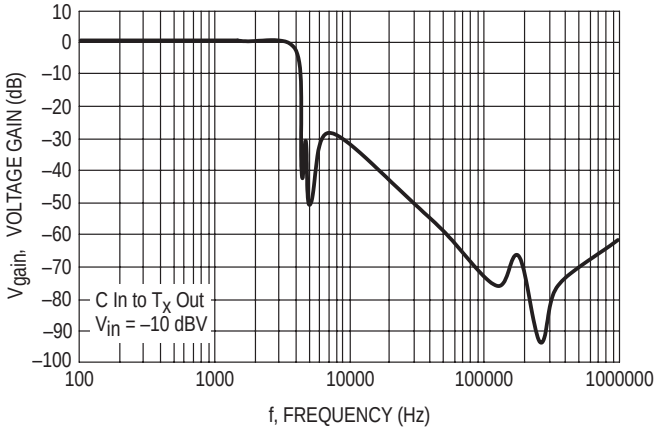


Figure 83. T_X Audio Inband Frequency Response

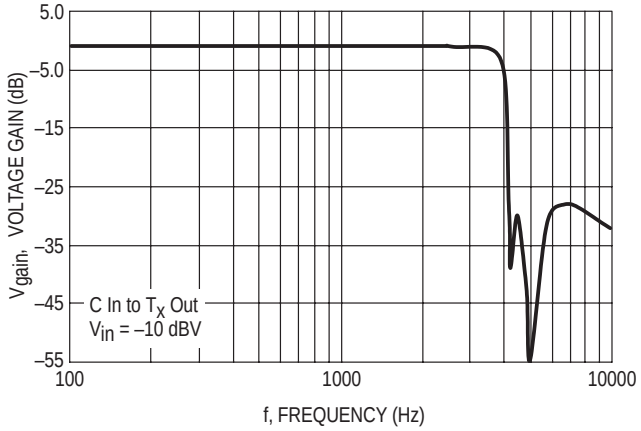


Figure 84. T_X Audio Ripple Response

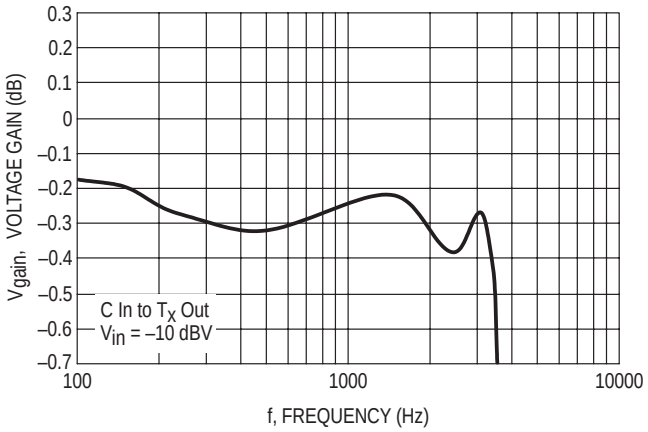


Figure 85. T_X Audio Inband Phase Response

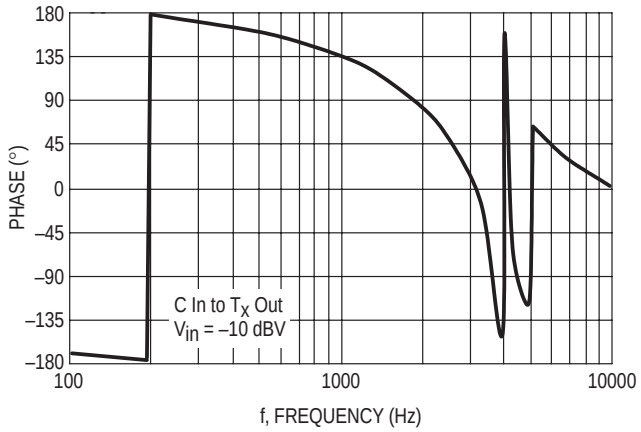


Figure 86. T_X Audio Inband Group Delay

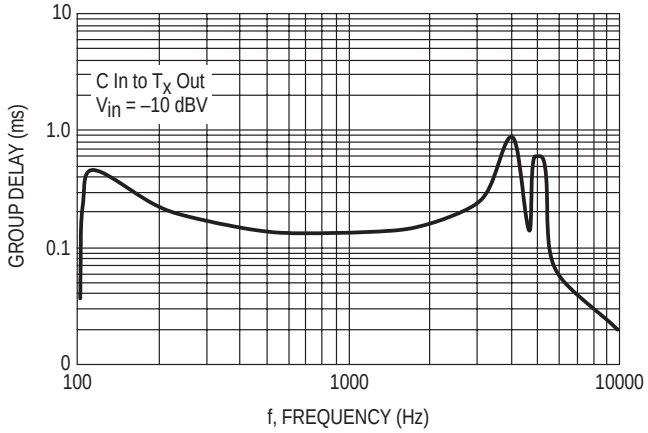
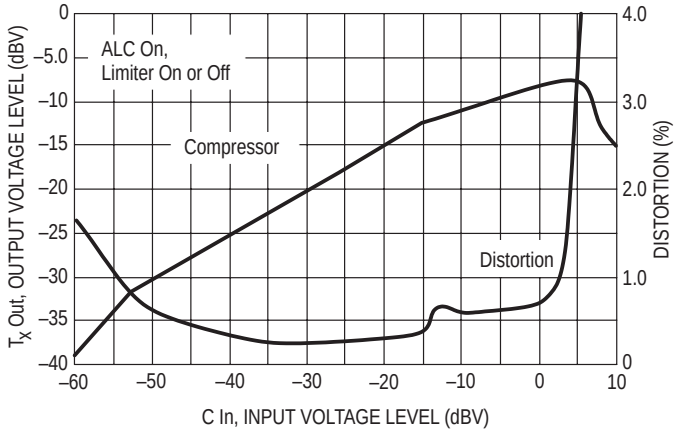


Figure 87. T_X Audio Compressor Response



T_X AUDIO

Figure 88. T_X Audio Compressor Response

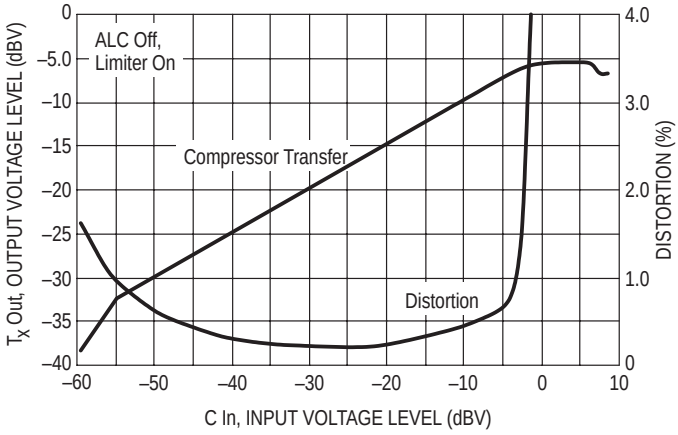


Figure 89. T_X Audio Compressor Response

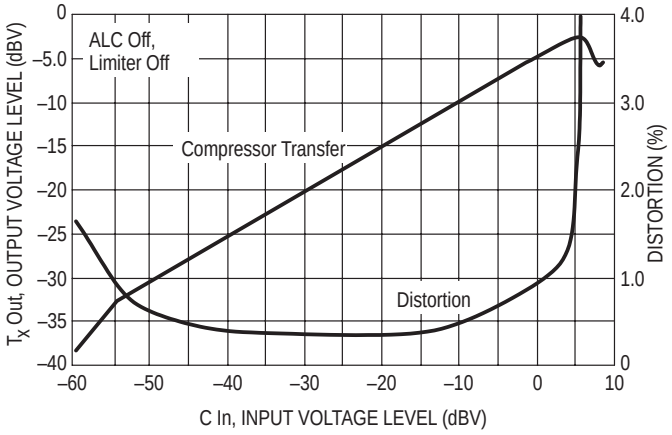


Figure 90. T_X Audio Maximum Output Voltage versus Gain Control Setting

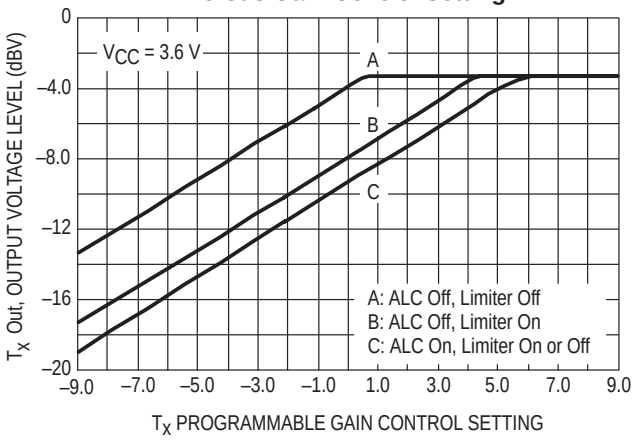


Figure 91. T_X Output Audio Response

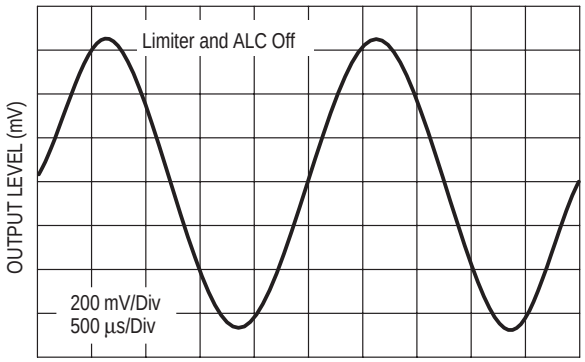


Figure 92. T_X Output Audio Response

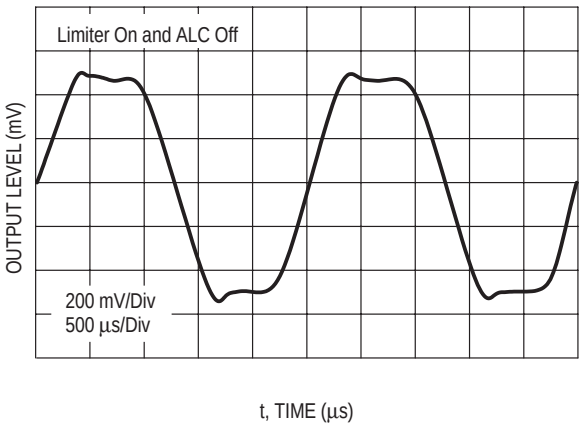
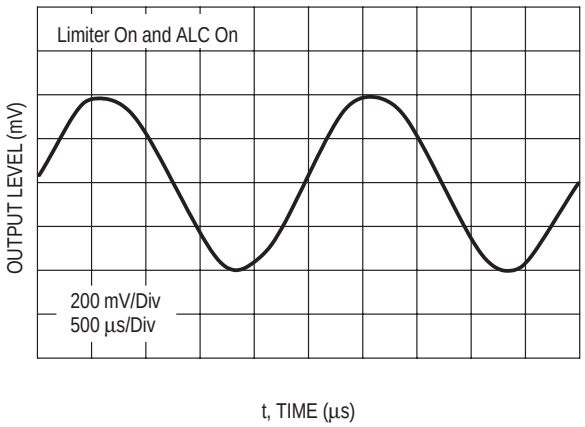


Figure 93. T_X Audio Output Response



PLL SYNTHESIZER SECTION

PLL Frequency Synthesizer General Description

Figure 95 shows a simplified block diagram of the programmable universal dual phase locked loop (PLL) designed into the MC13110A and MC13111A IC. This dual PLL is fully programmable through the MCU serial interface and supports most country channel frequencies including USA (25 ch), Spain, Australia, Korea, New Zealand, U.K., Netherlands, France, and China (see channel frequency tables in AN1575, "Worldwide Cordless Telephone Frequencies").

The 2nd local oscillator and reference divider provide the reference frequency signal for the R_X and T_X PLL loops. The programmed divider value for the reference divider is selected based on the crystal frequency and the desired R_X and T_X reference frequency values. For the U.K., additional divide by 25 and divide by 4 blocks are provided to allow for generation of the 1.0 kHz and 6.2 kHz reference frequencies.

The 14–bit R_X counter is programmed for the desired first local oscillator frequency. The 14–bit T_X counter is programmed for the desired transmit channel frequency. All counters power–up to a set default state for USA channel #21 using a 10.24 MHz reference frequency crystal (see power–up default latch register state in the Serial Programmable Interface section).

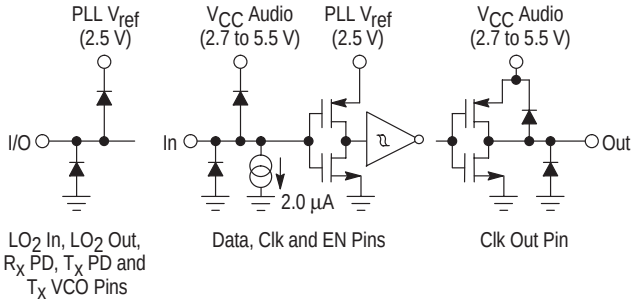
To extend the sensitivity of the 1st LO for U.S. 25 channel operation, internal fixed capacitors can be connected to the tank circuit through microprocessor programmable control. When designing the external PLL loop filters, it is recommended that the T_X and R_X phase detectors be considered as current drive type outputs. The loop filter control voltage must be 0.5 V away from either the positive or negative supply rail.

PLL I/O Pin Configurations

The 2nd LO, R_X and T_X PLL's, and MPU serial interface are powered by the internal voltage regulator at the "PLL V_{ref}" pin. The "PLL V_{ref}" pin is the output of a voltage regulator which is powered from the "V_{CC} Audio" power supply pin. It is regulated by an internal bandgap voltage reference. Therefore, the maximum input and output levels for most of the PLL I/O pins (LO2 In, LO2 Out, R_X PD, T_X PD, T_X VCO) is the regulated voltage at the "PLL V_{ref}" pin. The ESD protection diodes on these pins are also connected to "PLL V_{ref}".

Internal level shift buffers are provided for the pins (Data, Clk, EN, Clk Out) which connect directly to the microprocessor. The maximum input and output levels for these pins is V_{CC}. Figure 94 shows a simplified schematic of the I/O pins.

Figure 94. PLL I/O Pin Simplified Schematics

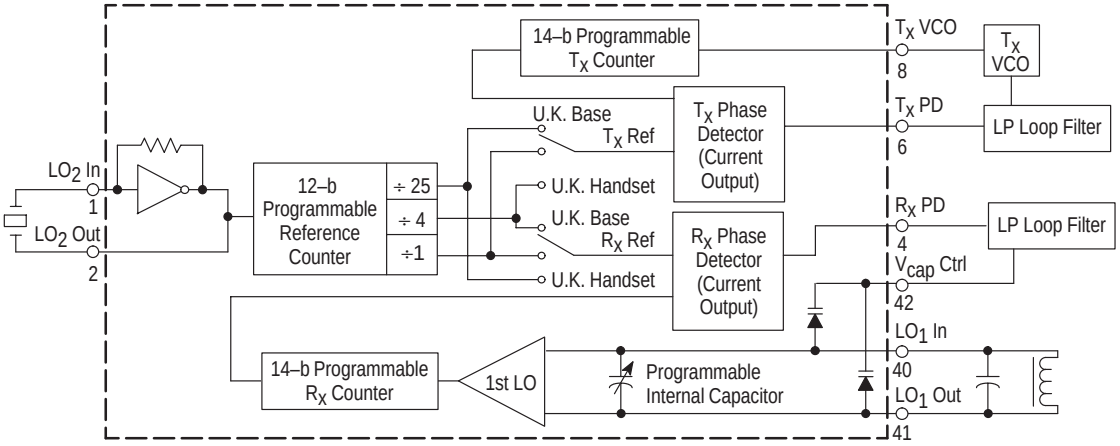


PLL Loop Control Voltage Range

The control voltage for the T_X and R_X loop filters is set by the phase detector outputs which drive the external loop filters. The phase detectors are best considered to have a current mode type output. The output can have three states; ground, high impedance, and positive supply, which in this case is the voltage at "PLL V_{ref}". When the loop is locked the phase detector outputs are at high impedance. An exception of this state is for narrow current pulses, referenced to either the positive or negative supply rails. If the loop voltages get within 0.5 V of either rail the linear current output starts to degrade. The phase detector current source was not designed to operate at the supply rails. VCO tuning range will also be limited by this voltage range

The maximum loop control voltage is the "PLL V_{ref}" voltage which is 2.5 V. If a higher loop control voltage range is desired, the "PLL V_{ref}" pin can be pulled to a higher voltage. It can be tied directly to the V_{CC} voltage (with suitable filter capacitors connected close to each pin). When this is done, the internal voltage regulator is automatically disabled. This is commonly used in the telephone base set where an external 5.0 V regulated voltage is available. It is important to remember, that if "PLL V_{ref}" is tied to V_{CC} and V_{CC} is not a regulated voltage, the PLL loop parameters and lock–up time will vary with supply voltage variation. The phase detector gain constant, K_{pd}, will not be affected if the "PLL V_{ref}" is tied to V_{CC}.

Figure 95. Dual PLL Simplified Block Diagram

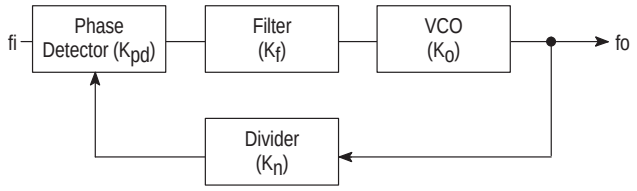


Loop Filter Characteristics

Lets consider the following discussion on loop filters. The fundamental loop characteristics, such as capture range, loop bandwidth, lock–up time, and transient response are controlled externally by loop filtering.

Figure 96 is the general model for a Phase Lock Loop (PLL).

Figure 96. PLL Model



Where:

K_{pd} = Phase Detector Gain Constant
K_f = Loop Filter Transfer Function
K_o = VCO Gain Constant
K_n = Divide Ratio (1/N)
fi = Input frequency
fo = Output frequency
fo/N = Feedback frequency divided by N

From control theory the loop transfer function can be represented as follows:

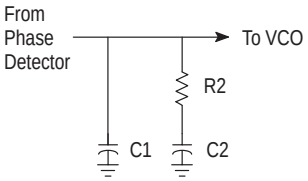
$A = K_{pd}\, K_f\, K_o\, K_n$ Open loop gain

K_{pd} can be either expressed as being 2.5 V/4.0 π or 1.0 mA/2.0 π for the CT–0 circuits. More details about performance of different type PLL loops, refer to Motorola application note AN535.

The loop filter can take the form of a simple low pass filter. A current output, type 2 filter will be used in this discussion since it has the advantage of improved step response, velocity, and acceleration.

The type 2 low pass filter discussed here is represented as follows:

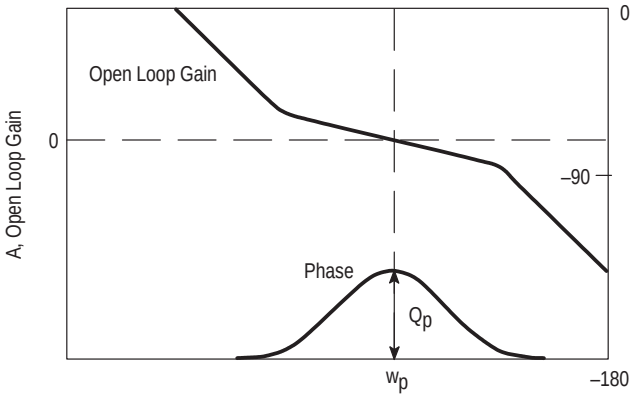
Figure 97. Loop Filter with Additional Integrating Element



From Figure 97, capacitor C1 forms an additional integrator, providing the type 2 response, and filters the discrete current steps from the phase detector output. The function of the additional components R2 and C2 is to create a pole and a zero (together with C1) around the 0 dB point of the open loop gain. This will create sufficient phase margin for stable loop operation.

In Figure 98, the open loop gain and the phase is displayed in the form of a Bode plot. Since there are two integrating functions in the loop, originating from the loopfilter and the VCO gain, the open loop gain response follows a second order slope (–40 dB/dec) creating a phase of –180 degrees at the lower and higher frequencies. The filter characteristic needs to be determined such that it is adding a pole and a zero around the 0 dB point to guarantee sufficient phase margin in this design (Qp in Figure 98).

Figure 98. Bode Plot of Gain and Phase in Open Loop Condition



The open loop gain including the filter response can be expressed as:

$$A_{openloop} = \frac{K_{pd}K_o(1 + jw(R2C2))}{jwK_n\left(jw\left(1 + jw\left(\frac{R2C1C2}{C1+C2}\right)\right)\right)} \quad \textbf{(1)}$$

The two time constants creating the pole and the zero in the Bode plot can now be defined as:

$$T1 = \frac{R2C1C2}{C1 + C2} \qquad T2 = R2C2 \quad \textbf{(2)}$$

By substituting equation (2) into (1), it follows:

$$A_{openloop} = \left(\frac{K_{pd}K_oT1}{w^2C1K_nT2}\right)\left(\frac{1 + jwT2}{1 + jwT1}\right) \quad \textbf{(3)}$$

The phase margin (phase + 180) is thus determined by:

$$Q_p = \arctan(wT2) - \arctan(wT1) \quad \textbf{(4)}$$

At $w=w_p$, the derivative of the phase margin may be set to zero in order to assure maximum phase margin occurs at w_p (see also Figure 98). This provides an expression for w_p:

$$\frac{dQ_p}{dw} = 0 = \frac{T2}{1 + (wT2)^2} - \frac{T1}{1 + (wT1)^2} \quad \textbf{(5)}$$

$$w = w_p = \frac{1}{\sqrt{T2T1}} \quad \textbf{(6)}$$

Or rewritten:

$$T1 = \frac{1}{w_p{}^2T2} \quad \textbf{(7)}$$

By substituting into equation (4), solve for T2:

$$T2 = \frac{\tan\left(\frac{Q_p}{2} + \frac{\pi}{4}\right)}{w_p} \quad \textbf{(8)}$$

By choosing a value for w_p and Q_p, T1 and T2 can be calculated. The choice of Q_p determines the stability of the loop. In general, choosing a phase margin of 45 degrees is a good choice to start calculations. Choosing lower phase margins will provide somewhat faster lock–times, but also generate higher overshoots on the control line to the VCO. This will present a less stable system. Larger values of phase margin provide a more stable system, but also increase lock–times. The practical range for phase margin is 30 degrees up to 70 degrees.

The selection of w_p is strongly related to the desired lock–time. Since it is quite complicated to accurately calculate lock time, a good first order approach is:

$$T\_lock \approx \frac{3}{w_p} \quad \textbf{(9)}$$

Equation (9) only provides an order of magnitude for lock time. It does not clearly define what the exact frequency difference is from the desired frequency and it does not show the effect of phase margin. It assumes, however, that the phase detector steps up to the desired control voltage without hesitation. In practice, such step response approach is not really valid. The two input frequencies are not locked. Their phase maybe momentarily zero and force the phase detector into a high impedance mode. Hence, the lock times may be found to be somewhat higher.

In general, w_p should be chosen far below the reference frequency in order for the filter to provide sufficient attenuation at that frequency. In some applications, the reference frequency might represent the spacing between channels. Any feedthrough to the VCO that shows up as a spur might affect adjacent channel rejection. In theory, with the loop in lock, there is no signal coming from the phase detector. But in practice leakage currents will be supplied to both the VCO and the phase detector. The external capacitors may show some leakage, too. Hence, the lower w_p, the better the reference frequency is filtered, but the longer it takes for the loop to lock.

As shown in Figure 98, the open loop gain at w_p is 1 (or 0 dB), and thus the absolute value of the complex open loop gain as shown in equation (3) solves C1:

$$C1 = \left(\frac{K_{pd}K_oT1}{w^2K_nT2}\right)\sqrt{\frac{\left(1 + w_pT2\right)^2}{\left(1 + w_pT1\right)^2}} \quad \textbf{(10)}$$

With C1 known, and equation (2) solve C2 and R2:

$$C2 = C1\left(\frac{T2}{T1} - 1\right) \quad \textbf{(11)}$$

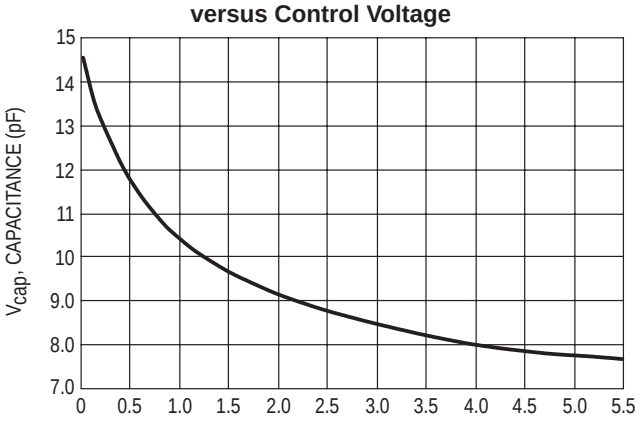
$$R2 = \frac{T2}{C2} \quad \textbf{(12)}$$

The VCO gain is dependent on the selection of the external inductor and the frequency required. The free running frequency of the VCO is determined by:

$$f = \frac{1}{2\pi\sqrt{LC_T}} \quad \textbf{(13)}$$

In which L represents the external inductor value and C_T represents the total capacitance (including internal capacitance) in parallel with the inductor. The VCO gain can be easily calculated via the internal varicap transfer curve shown below.

Figure 99. Varicap Capacitance versus Control Voltage



As can be derived from Figure 99, the varicap capacitance changes 1.3 pF over the voltage range from 1.0 V to 2.0 V:

$$\Delta Cvar = \frac{1.3\ pF}{V} \quad \textbf{(14)}$$

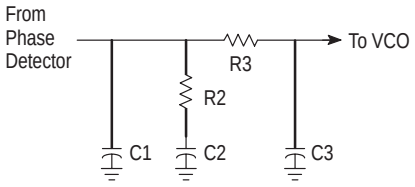
Combining (13) with (14) the VCO gain can be determined by:

$$K_O = \frac{1}{jw}\left\{\frac{1}{2\pi\sqrt{L\left(C_T + \frac{\Delta Cvar}{2}\right)}} - \frac{1}{2\pi\sqrt{L\left(C_T + \frac{\Delta Cvar}{2}\right)}}\right\} \quad \textbf{(15)}$$

Although the basic loopfilter previously described provides adequate performance for most applications, an extra pole may be added for additional reference frequency filtering. Given that the channel spacing in a CT–0 telephone set is based on the reference frequency, and any feedthrough to

the first LO may effect parameters like adjacent channel rejection and intermodulation. Figure 100 shows a loopfilter architecture incorporating an additional pole.

Figure 100. Loop Filter with Additional Integrating Element



For the additional pole formed by R3 and C3 to be efficient, the cut–off frequency must be much lower than the reference frequency. However, it must also be higher than w_p in order not to compromise phase margin too much. The following equations were derived in a similar manner as for the basic filter previously described.

Similarly, it can be shown:

$$A_{openloop} = -\frac{K_{pd}K_o}{K_n w^2\left((C1 + C2 + C3) - w^2 C1C2C3R2R3\right)} + \frac{1 + jwT2}{1 + jwT1} \quad \textbf{(16)}$$

In which:

$$T1 = \frac{(C1 + C2)T2 + (C1C2)T3}{C1 + C2 + C3 - w^2 C1T2T3} \quad \textbf{(17)}$$

$$T2 = R2C2 \quad \textbf{(18)} \qquad T3 = R3C3 \quad \textbf{(19)}$$

From T1 it can be derived that:

$$C2 = \frac{(T1 + T2)C3 - C1\left(T2 + T3 - T1 + w^2 T1T2T3\right)}{T3 - T1} \quad \textbf{(20)}$$

In analogy with (10), by forcing the loopgain to 1 (0 dB) at w_p, we obtain:

$$C1(T1 + T2) + C2T3 + C3T2 = \left(\frac{K_{pd}K_o}{K_n {w_p}^2}\right)\sqrt{\frac{1 + \left(w_pT2\right)^2}{1 + \left(w_pT1\right)^2}} \quad \textbf{(21)}$$

Solving for C1:

$$C1 = \frac{(T2 - T1)T3C3 - (T3 - T1)T2C3 + (T3 - T1)\left(\frac{K_{pd}K_oT1}{{w_p}^2K_n}\right)\sqrt{\frac{1+\left(w_pT2\right)^2}{1+\left(w_pT1\right)^2}}}{(T3 - T1)T2 + (T3 - T1)T3 - \left(T2 + T3 - T1 + {w_p}^2T1T2T3\right)T3} \quad \textbf{(22)}$$

By selecting w_p via (9), the additional time constant expressed as T3, can be set to:

$$T3 = \frac{1}{Kw_p} \quad \textbf{(23)}$$

The K–factor shown determines how far the additional pole frequency will be separated from w_p. Selecting too small of a K–factor, the equations may provide negative capacitance or resistor values. Too large of a K–factor may not provide the maximum attenuation.

By selecting R3 to be 100 kΩ, C3 becomes known and C1 and C2 can be solved from the equations. By using equations (8) and (7), time constants T2 and T1 can be derived by selecting a phase margin. Finally, R2 follows from T2 and C2.

The following pages, the loopfilter components are determined for both handset and baseset the US application based on the equations described. Choose K to be approximately five times w_p ($5w_p$).

In an application, w_p is chosen to be 20 times less than the reference frequency of 5.0 kHz and the phase margin has been set to 45 degrees. This provides a lock time according to (9) of about 2.0 ms (order of magnitude). With the adjacent channels spaced at least 15 kHz away, reference feedthrough at w_p will not be directly disastrous but still, the additional pole may be added in the loopfilter design for added safety.

In an application, w_p is chosen to be 20 times less than the reference frequency of 5.0 kHz and the phase margin has been set to 45 degrees. This provides a lock time according to (9) of about 2.0 ms (order of magnitude). With the adjacent channels spaced at least 15 kHz away, reference feedthrough at w_p will not be directly disastrous but still, the additional pole may be added in the loopfilter design for added safety.

Figure 101. Open Loop Response Handset US with Selected Values

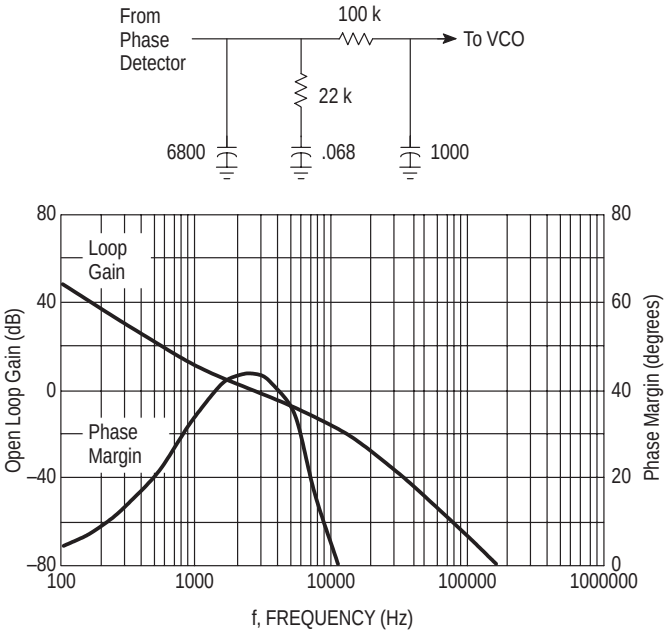


Figure 102. Open Loop Response Baseset US with Selected Values

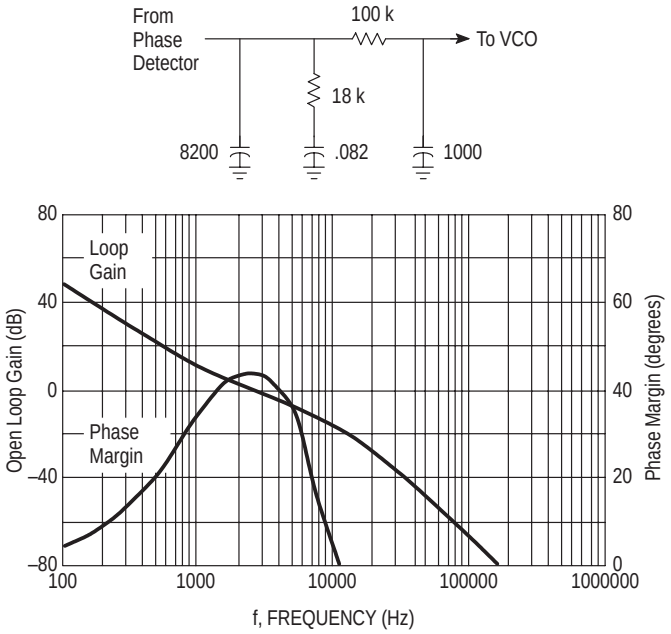


Figure 103. Handset US

Conditions		
L = 470 uH	F_{ref} = 5.0 kHz	
RF = 46.77 MHz	Q_p = 45 degrees	
VCO center = 36.075 MHz	$w_p = w_{ref}$ / 20 radians	
Results	**Equations**	**Select**
K_{pd} = 159.2 uA/rad		
K_{VCO} = 3.56 Mrad/V	(14), (15)	
T2 = 1540 µs	(8)	
T1 = 264 µs	(7)	
T3 = 91 µs	with K = 7	
C1 = 7.6 nF	(21)	C1 = 6.8 nF
C2 = 70.9 nF	(20)	C2 = 68 nF
R2 = 21.7 kΩ	(18)	R2 = 22 kΩ
R3 = 100 kΩ	choose:	R3 = 100 kΩ
C3 = 909.5 pF	(19)	C3 = 1 nf

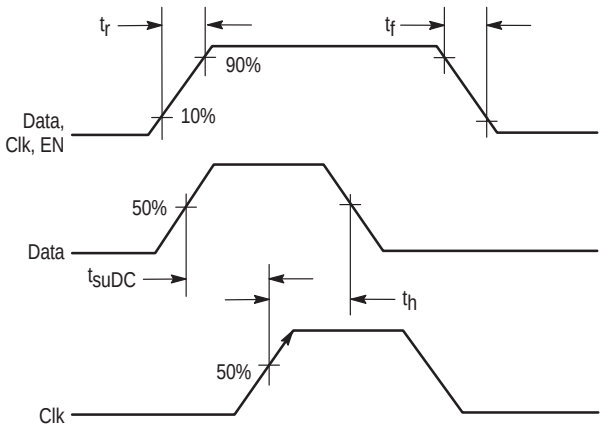
Figure 104. Baseset US

Conditions		
L = 470 uH	F_{ref} = 5.0 kHz	
RF = 49.83 MHz	Q_p = 45 degrees	
VCO center = 39.135 MHz	$w_p = w_{ref}$ / 20 radians	
Results	**Equations**	**Select**
K_{pd} = 159.2 uA/rad		
K_{VCO} = 4.54 Mrad/V	(14), (15)	
T2 = 1540 µs	(8)	
T1 = 264 µs	(7)	
T3 = 91 µs	with K = 7	
C1 = 9.1 nF	(21)	C1 = 8.2 nF
C2 = 83.5 nF	(20)	C2 = 82 nF
R2 = 18.4 kΩ	(18)	R2 = 18 kΩ
R3 = 100 kΩ	choose:	R3 = 100 kΩ
C3 = 909.5 pF	(19)	C3 = 1 nf

Microprocessor Serial Interface

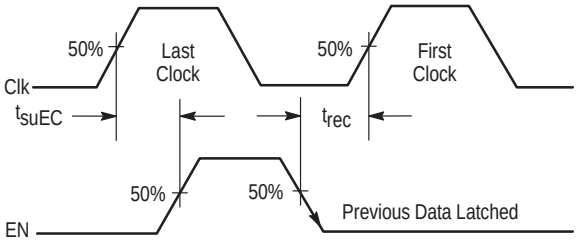
The Data, Clock, and Enable (“Data”, “Clk”, and “EN” respectively) pins provide a MPU serial interface for programming the reference counters, the transmit and receive channel divide counters, the switched capacitor filter clock counter, and various other control functions. The “Data” and “Clk” pins are used to load data into the MC13111A shift register (Figure 109). Figure 105 shows the timing required on the “Data” and “Clk” pins. Data is clocked into the shift register on positive clock transitions.

Figure 105. Data and Clock Timing Requirement



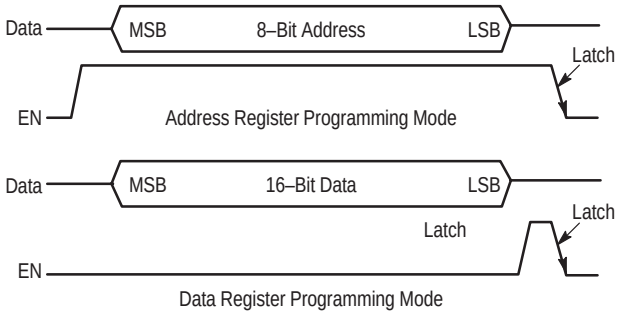
After data is loaded into the shift register, the data is latched into the appropriate latch register using the “EN” pin. This is done in two steps. First, an 8–bit address is loaded into the shift register and latched into the 8–bit address latch register. Then, up to 16–bits of data is loaded into the shift register and latched into the data latch register. It is specified by the address that was previously loaded. Figure 106 shows the timing required on the EN pin. Latching occurs on the negative EN transition.

Figure 106. Enable Timing Requirement



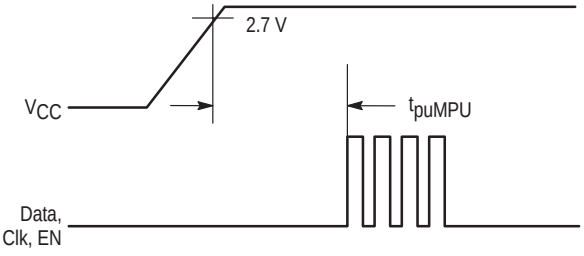
The state of the “EN” pin when clocking data into the shift register determines whether the data is latched into the address register or a data register. Figure 107 shows the address and data programming diagrams. In the data programming mode, there must not be any clock transitions when “EN” is high. The clock can be in a high state (default high) or a low state (default low) but must not have any transitions during the “EN” high state. The convention in these figures is that latch bits to the left are loaded into the shift register first. A minimum of four “Clk” rising edge transition must occur before a negative “EN” transition will latch data or an address into a register.

Figure 107. Microprocessor Interface Programming Mode Diagrams



The MPU serial interface is fully operational within 100 μs after the power supply has reached its minimum level during power–up (see Figure 108). The MPU Interface shift registers and data latches are operational in all four power saving modes; Inactive, Standby, R_X, and Active Modes. Data can be loaded into the shift registers and latched into the latch registers in any of the operating modes.

Figure 108. Microprocessor Serial Interface Power–Up Delay



Data Registers

Figure 109 shows the data latch registers and addresses which are used to select each of each registers. Latch bits to the left (MSB) are loaded into the shift register first. The LSB bit must always be the last bit loaded into the shift register. Bits proceeding the register must be “0’s” as shown.

Power–Up Defaults for Data Registers

When the IC is first powered up, all latch registers are initialized to a defined state. The device is initially placed in the R_X mode with all mutes active. The reference counter is set to generate a 5.0 kHz reference frequency from a 10.24 MHz crystal. The switched capacitor filter clock counter is set properly for operation with a 10.24 MHz crystal. The T_X and R_X counter registers are set for USA handset channel frequency, number 21 (Channel 6 for previous FCC 10 Channel Band). Figure 110 shows the initial power–up states for all latch registers.

Figure 109. Microprocessor Interface Data Latch Registers

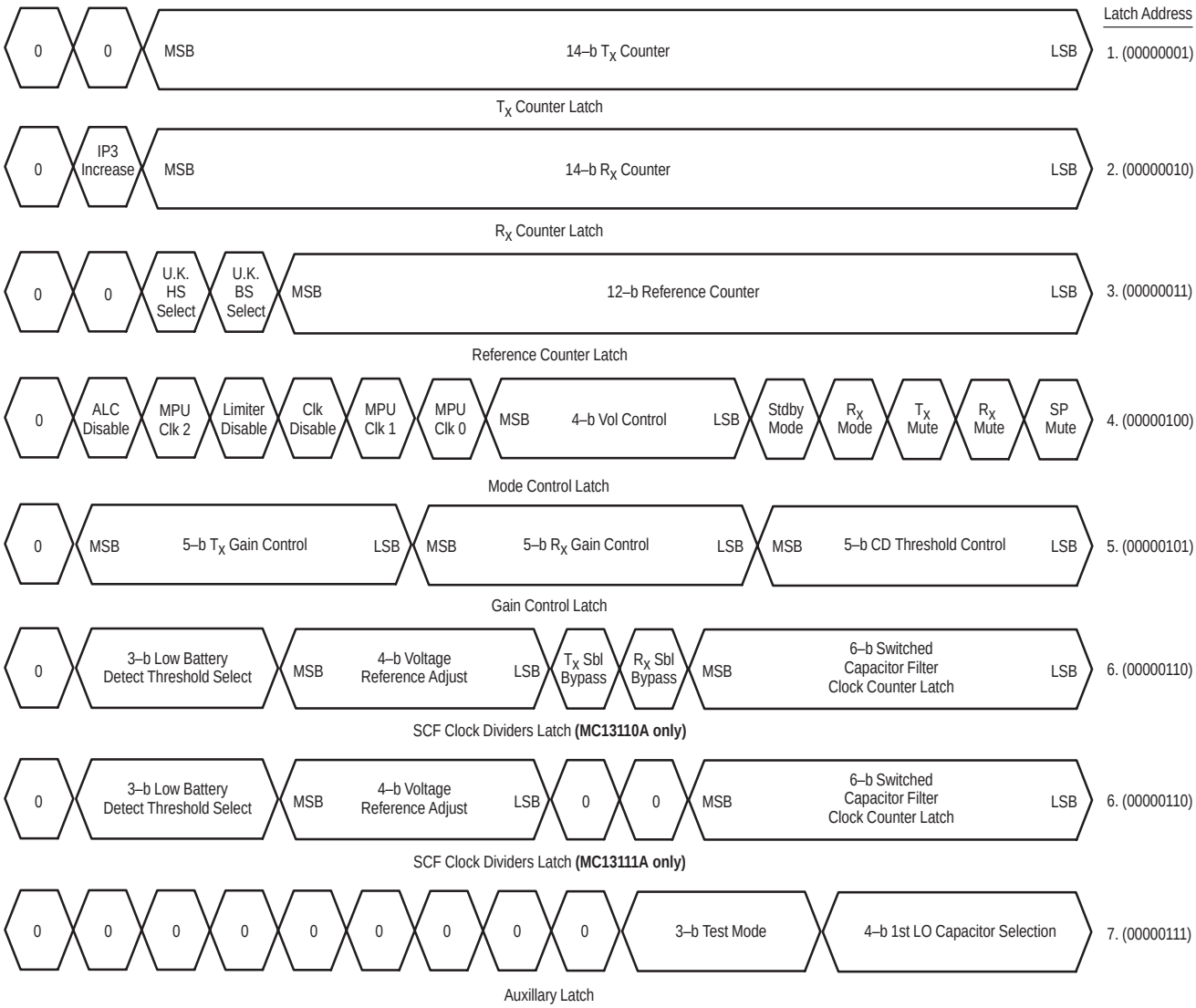


Figure 110. Latch Register Power–Up Defaults

Register	Count	MSB								LSB							
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
T_X	9966	–	–	1	0	0	1	1	0	1	1	1	0	1	1	1	0
R_X	7215	–	–	0	1	1	1	0	0	0	0	1	0	1	1	1	1
Ref	2048	–	–	0	0	1	0	0	0	0	0	0	0	0	0	0	0
Mode	N/A	–	0	0	0	0	1	1	0	1	1	1	0	1	1	1	1
Gain	N/A	–	0	1	1	1	1	0	1	1	1	1	1	0	1	0	0
SCF (MC13110A)	31	–	0	0	0	0	1	1	1	0	0	0	1	1	1	1	1
SCF (MC13111A)	31	–	0	0	0	0	1	1	1	–	–	0	1	1	1	1	1
Aux	N/A	–	–	–	–	–	–	–	–	–	0	0	0	0	0	0	0

NOTE: 12. Bits 6 and 7 in the SCF latch register are ”Don’t Cares” for the MC13111A since this part does not have a scrambler.

T_X and R_X Counter Registers

The 14 bit T_X and R_X counter registers are used to select the transmit and receive channel frequencies. In the R_X counter there is an “IP3 Increase” bit that allows the ability to trade off increased receiver mixer performance versus reduced power consumption. With “IP3 increase” = <1>, there is about a 10 dB improvement in 1 dB compression and 3rd order intercept for both the 1st and 2nd mixers. However, there is also an increase in power supply current of 1.3 mA. The power–up default for the MC13111A is “IP3 Increase” = <0>. The register bits are shown in Figure 111.

Reference Counter Register

Reference Counter

Figure 113 shows how the reference frequencies for the R_X and T_X loops are generated. All countries except the U.K. require that the T_X and R_X reference frequencies be identical. In this case, set “U.K. Base Select” and “U.K. Handset Select” bits to “0”. Then the fixed divider is set to “1” and the T_X and R_X reference frequencies will be equal to the crystal oscillator frequency divided by the programmable reference counter value.

The U.K. is a special case which requires a different reference frequency value for T_X and R_X. For U.K. base operation, set “U.K. Base Select” to “1”. For U.K. handset operation, set “U.K. Handset Select” to “1”. The Netherlands is also a special case. A 2.5 kHz reference frequency is used for both the T_X and R_X reference and the total divider value required is 4096. This is larger than the maximum divide value available from the 12–bit reference divider (4095). In this case, set “U.K. Base Select” to “1” and set “U.K. Handset Select” to “1”. This will give a fixed divide by 4 for both the T_X and R_X reference. Then set the reference divider to 1024 to get a total divider of 4096.

Figure 111. R_X and T_X Counter Register Latch Bits

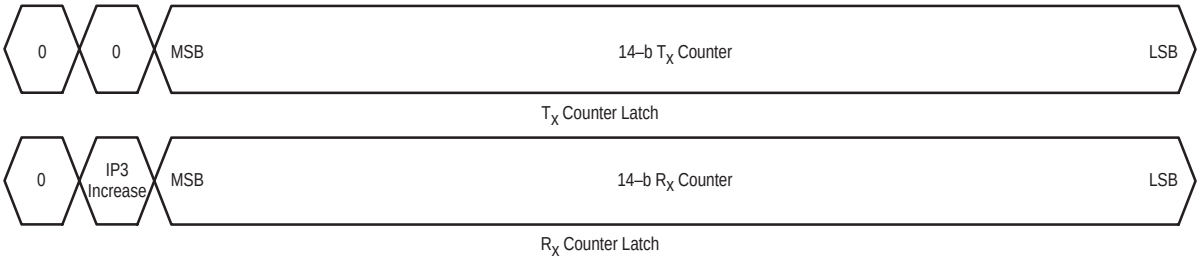
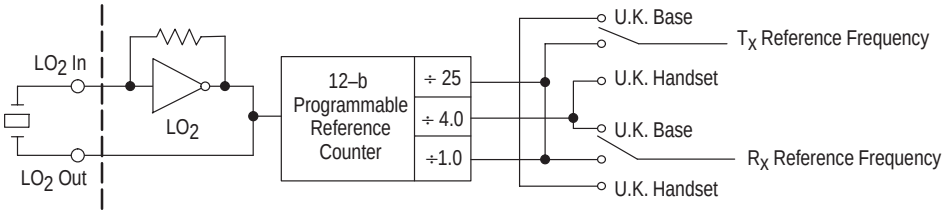


Figure 112. Reference Counter Register

Figure 113. Reference Counter Register Programming Mode

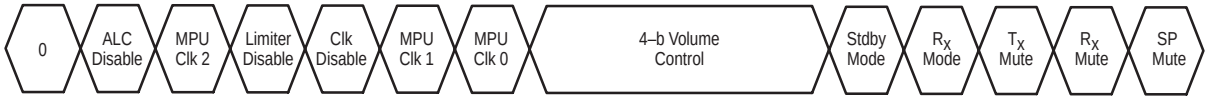


U.K. Handset Select	U.K. Base Select	T_X Divider Value	R_X Divider Value	Application
0	0	1	1	All but U.K. and Netherlands
0	1	25	4	U.K. Base Set
1	0	4	25	U.K. Hand Set
1	1	4	4	Netherlands Base and Hand Set

Figure 114. Reference Frequency and Divider Values

MC13110A / MC13111A							
Crystal Frequency	**Reference Divider Value**	**U.K. Base/ Handset Divider**	**Reference Frequency**	**SC Filter Clock Divider**	**SC Filter Clock Frequency**	**Scrambler Modulation Divider**	**Scrambler Modulation Frequency**
10.24 MHz	2048	1	5.0 kHz	31	165.16 kHz	40	4.129 kHz
10.24 MHz	1024	4	5.0 kHz	31	165.16 kHz	40	4.129 kHz
11.15 MHz	2230	1	5.0 kHz	34	163.97 kHz	40	4.099 kHz
12.00 MHz	2400	1	5.0 kHz	36	166.67 kHz	40	4.167 kHz
11.15 MHz	1784	1	6.25 kHz	34	163.97 kHz	40	4.099 kHz
11.15 MHz	446	4	6.25 kHz	34	163.97 kHz	40	4.099 kHz
11.15 MHz	446	25	1.0 kHz	34	163.97 kHz	40	4.099 kHz

Figure 115. Mode Control Register



Reference Frequency Selection

The "LO_2 In" and "LO_2 Out" pins form a reference oscillator when connected to an external parallel–resonant crystal. The reference oscillator is also the second local oscillator for the RF Receiver. Figure 114 shows the relationship between different crystal frequencies and reference frequencies for cordless phone applications in various countries. "LO_2 In" may also serve as an input for an externally generated reference signal which is ac–coupled. The switched capacitor filter 6–bit programmable counter must be programmed for the crystal frequency that is selected since this clock is derived from the crystal frequency and must be held constant regardless of the crystal that is selected. The actual switched capacitor clock divider ratio is twice the programmed divider ratio due to the a fixed divide by 2.0 after the programmable counter. The scrambler mixer modulation frequency is the switched capacitor clock divided by 40 for the MC13110A.

Mode Control Register

The power saving modes; mutes, disables, volume control, and microprocessor clock output frequency are all set by the Mode Control Register. Operation of the Control Register is explained in Figures 115 through 119.

Figure 116. Mute and Disable Control Bit Descriptions

ALC Disable	1 0	Automatic Level Control Disabled Normal Operation
T_X Limiter Disable	1 0	T_X Limiter Disabled Normal Operation
Clock Disable (MC13110A/111A)	1 0	MPU Clock Output Disabled Normal Operation
T_X Mute	1 0	Transmit Channel Muted Normal Operation
R_X Mute	1 0	Receive Channel Muted Normal Operation
SP Mute	1 0	Speaker Amp Muted Normal Operation

Power Saving Operating Modes

When the MC13110A or MC13111A are used in a handset, it is important to conserve power in order to prolong battery life. There are five modes of operation for the MC13110A/MC13111A; Active, R_X, Standby, Interrupt, and Inactive. They are Active, R_X, and Standby. In the Active mode, all circuit blocks are powered. In the R_X mode, all circuitry is powered down except for those circuit sections needed to receive a transmission from the base. In the Standby and Interrupt Modes, all circuitry is powered down except for the circuitry needed to provide the clock output for the microprocessor. In the Inactive Mode, all circuitry is powered down except the MPU serial interface. Latch memory is maintained in all modes. Figure 118 shows the control register bit values for selection of each power saving mode and Figure 118 shows the circuit blocks which are powered in each of these operating modes.

Figure 117. Power Saving Mode Selection

Stdby Mode Bit	R_X Mode Bit	"CD Out/ Hardware Interrupt" Pin	Power Saving Mode
MC13110A/MC13111A			
0	0	X	Active
0	1	X	R_X
1	0	X	Standby
1	1	1 or High Impedance	Inactive
1	1	0	Interrupt
MC13110B/MC13111B [Note 14]			
0	0	X	Active
0	1	X	R_X
1	X	X	Standby
1	1	0	Interrupt

NOTES: 13. "X" is a don't care
14. MPU Clock Out is "Always On"

Figure 118. Circuit Blocks Powered During Power Saving Modes

Circuit Blocks	MC13110A/MC13111A			
	Active	R_X	Standby	Inactive
"PLL V_{ref}" Regulated Voltage	X	X	X[1]	X[1, 2]
MPU Serial Interface	X	X	X	X[2]
2nd LO Oscillator	X	X	X	
MPU Clock Output	X	X	X	
RF Receiver and 1st LO VCO	X	X		
R_X PLL	X	X		
Carrier Detect	X	X		
Data Amp	X	X		
Low Battery Detect	X	X		
T_X PLL	X			
R_X and T_X Audio Paths	X			

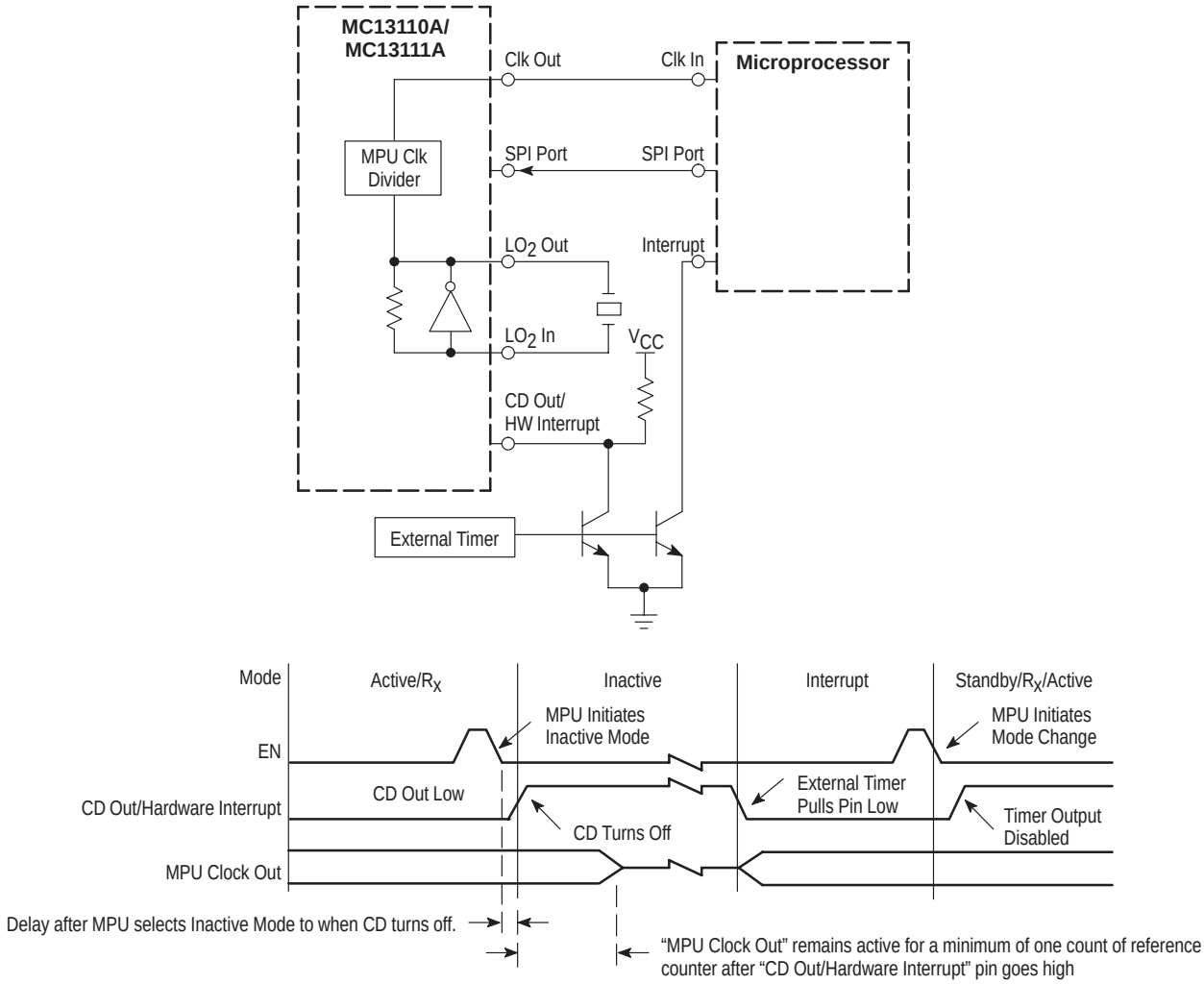
NOTE: 15. In Standby and Inactive Modes, "PLL V_{ref}" remains powered but is not regulated. It will fluctuate with V_{CC}.

Power Saving Application

In some handset applications it may be desirable to power down all circuitry including the microprocessor (MPU). First put the MC13110A/MC13111A into the Inactive mode. This turns off the MPU Clock Output (see Figure 119) and disables the microprocessor. Once a command is given to switch the IC into an "Inactive" mode, the MPU Clock output will remain active for a minimum of one reference counter cycle (about 200 μs) and up to a maximum of two reference counter cycles (about 400 μs). This is performed in order to give the MPU adequate time to power down.

An external timing circuit should be used to initiate the turn–on sequence. The "CD Out" pin has a dual function. In the Active and R_X modes it performs the carrier detect function. In the Standby and Inactive modes the carrier detect circuit is disabled and the "CD Out" pin is in a "High" state, because of an external pull–up resistor. In the Inactive mode, the "CD Out" pin is the input for the hardware interrupt function. When the "CD Out" pin is pulled "low", by the external timing circuit, the IC switches from the Inactive to the Interrupt mode. Thereby turning on the MPU Clock Output. The MPU can then resume control of the IC. The "CD Out" pin must remain low until the MPU changes the operating mode from Interrupt to Standby, Active, or R_X modes.

Figure 119. Power Saving Application



MPU "Clk Out" Divider Programming

The "Clk Out" signal is derived from the second local oscillator. It can be used to drive a microprocessor (MPU) clock input. This will eliminate the need for a separate crystal to drive the MPU, thus reducing system cost. Figure 120 shows the relationship between the second LO crystal frequency and the clock output for each divide value. Figure 121 shows the "Clk Out" register bit values. With a 10.24 MHz crystal, the divide by 312.5 gives the same clock frequency as a clock crystal and allows the MPU to display the time on a LCD display without additional external components.

Figure 120. Clock Output Values

Crystal Frequency	Clock Output Divider							
	2	2.5	3	4	5	20	80	312.5
10.24 MHz	5.120 MHz	4.096 MHz	3.413 MHz	2.560 MHz	2.048 MHz	512 kHz	128 kHz	32.768 kHz
11.15 MHz	5.575 MHz	4.460 MHz	3.717 MHz	2.788 MHz	2.230 MHz	557 kHz	139 kHz	35.680 kHz
12.00 MHz	6.000 MHz	4.800 MHz	4.000 MHz	3.000 MHz	2.400 MHz	600 kHz	150 kHz	38.400 kHz

Figure 121. Clock Output Divider

MPU Clk Bit #2	MPU Clk Bit #1	MPU Clk Bit #0	Clk Out Divider Value
0	0	0	2
0	0	1	3
0	1	0	4
0	1	1	5
1	0	0	2.5
1	0	1	20
1	1	0	80
1	1	1	312.5

MPU "Clk Out" Power–Up Default Divider Value

The power–up default divider value is "divide by 5". This provides a MPU clock of about 2.0 MHz after initial power–up. The reason for choosing a relatively low clock frequency at initial power–up is because some microprocessors operate using a 3.0 V power supply and have a maximum clock frequency of 2.0 MHz. After initial power–up, the MPU can change the clock divider value and set the clock to the desired operating frequency. Special care was taken in the design of the clock divider to insure that the transition between one clock divider value and another is "smooth" (i.e. there will be no narrow clock pulses to disturb the MPU).

MPU "Clk Out" Radiated Noise on Circuit Board

The clock line running between the MC13110A or MC13111A and the microprocessor has the potential to radiate noise. Problems in the system can occur, especially if the clock is a square wave digital signal with large high frequency harmonics. In order to minimize the radiated noise, a 1000 Ω resistor is included on–chip in series with the "Clk Out" output driver. A small capacitor or inductor with a capacitor can be connected to the "Clk Out" line on the PCB to form a one or two pole low pass filter. This filter should significantly reduce noise radiated by attenuating the high frequency harmonics on the signal line. The filter can also be used to attenuate the signal level so that it is only as large as required by the MPU clock input. To further reduce radiated noise, the PCB signal trace length should be kept to a minimum.

Volume Control Programming

The volume control adjustable gain block can be programmed in 2 dB gain steps from –14 dB to +16 dB. The power–up default value for the MC13110A and MC13111A is 0 dB. (see Figure 122)

Figure 122. Volume Control

Volume Control Bit #3	Volume Control Bit #2	Volume Control Bit #1	Volume Control Bit #0	Volume Control #	Gain/Attenuation Amount
0	0	0	0	0	–14 dB
0	0	0	1	1	–12 dB
0	0	1	0	2	–10 dB
0	0	1	1	3	–8 dB
0	1	0	0	4	–6 dB
0	1	0	1	5	–4 dB
0	1	1	0	6	–2 dB
0	1	1	1	7	0 dB
1	0	0	0	8	2 dB
1	0	0	1	9	4 dB
1	0	1	0	10	6 dB
1	0	1	1	11	8 dB
1	1	0	0	12	10 dB
1	1	0	1	13	12 dB
1	1	1	0	14	14 dB
1	1	1	1	15	16 dB

Gain Control Register

The gain control register contains bits which control the T_X Voltage Gain, R_X Voltage Gain, and Carrier Detect threshold. Operation of these latch bits are explained in Figures 123, 124 and 125.

T_X and R_X Gain Programming

The T_X and R_X audio signal paths each have a programmable gain block. If a T_X or R_X voltage gain, other than the nominal power–up default, is desired, it can be programmed through the MPU interface. Alternately, these programmable gain blocks can be used during final test of the telephone to electronically adjust for gain tolerances in the telephone system (see Figure 124). In this case, the T_X and R_X gain register values should be stored in ROM during final test so that they can be reloaded each time the IC is powered up.

Figure 123. Gain Control Latch Bits

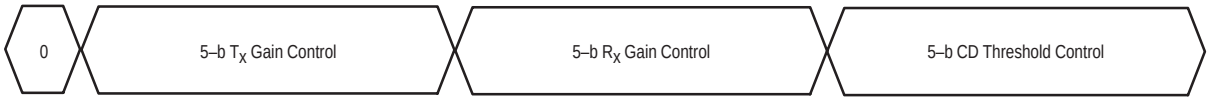


Figure 124. T_X and R_X Gain Control

Gain Control Bit #4	Gain Control Bit #3	Gain Control Bit #2	Gain Control Bit #1	Gain Control Bit #0	Gain Control #	Gain/Attenuation Amount
–	–	–	–	–	<6	–9 dB
0	0	1	1	0	6	–9 dB
0	0	1	1	1	7	–8 dB
0	1	0	0	0	8	–7 dB
0	1	0	0	1	9	–6 dB
0	1	0	1	0	10	–5 dB
0	1	0	1	1	11	–4 dB
0	1	1	0	0	12	–3 dB
0	1	1	0	1	13	–2 dB
0	1	1	1	0	14	–1 dB
0	1	1	1	1	15	0 dB
1	0	0	0	0	16	1 dB
1	0	0	0	1	17	2 dB
1	0	0	1	0	18	3 dB
1	0	0	1	1	19	4 dB
1	0	1	0	0	20	5 dB
1	0	1	0	1	21	6 dB
1	0	1	1	0	22	7 dB
1	0	1	1	1	23	8 dB
1	1	0	0	0	24	9 dB
1	1	0	0	1	25	10 dB
–	–	–	–	–	>25	10 dB

Carrier Detect Threshold Programming

The “CD Out” pin gives an indication to the microprocessor if a carrier signal is present on the selected channel. The nominal value and tolerance of the carrier detect threshold is given in the carrier detect specification section of this document. If a different carrier detect threshold value is desired, it can be programmed through the MPU interface as shown in Figure 125 below. Alternately, the carrier detect threshold can be electronically adjusted during final test of the telephone to reduce the tolerance of the carrier detect threshold. This is done by measuring the threshold and then by adjusting the threshold through the MPU interface. In this case, it is necessary to store the carrier detect register value in ROM so that the CD register can be reloaded each time the combo IC is powered up. If a preamp is used before the first mixer it may be desirable to scale the carrier detect range by connecting an external resistor from the “RSSI” pin to ground. The internal resistor is 187 kΩ.

Figure 125. Carrier Detect Threshold Control

CD Bit #4	CD Bit #3	CD Bit #2	CD Bit #1	CD Bit #0	CD Control #	Carrier Detect Threshold
0	0	0	0	0	0	–20 dB
0	0	0	0	1	1	–19 dB
0	0	0	1	0	2	–18 dB
0	0	0	1	1	3	–17 dB
0	0	1	0	0	4	–16 dB
0	0	1	0	1	5	–15 dB
0	0	1	1	0	6	–14 dB
0	0	1	1	1	7	–13 dB
0	1	0	0	0	8	–12 dB
0	1	0	0	1	9	–11 dB
0	1	0	1	0	10	–10 dB
0	1	0	1	1	11	–9 dB
0	1	1	0	0	12	–8 dB
0	1	1	0	1	13	–7 dB
0	1	1	1	0	14	–6 dB
0	1	1	1	1	15	–5 dB
1	0	0	0	0	16	–4 dB
1	0	0	0	1	17	–3 dB
1	0	0	1	0	18	–2 dB
1	0	0	1	1	19	–1 dB
1	0	1	0	0	20	0 dB
1	0	1	0	1	21	1 dB
1	0	1	1	0	22	2 dB
1	0	1	1	1	23	3 dB
1	1	0	0	0	24	4 dB
1	1	0	0	1	25	5 dB
1	1	0	1	0	26	6 dB
1	1	0	1	1	27	7 dB
1	1	1	0	0	28	8 dB
1	1	1	0	1	29	9 dB
1	1	1	1	0	30	10 dB
1	1	1	1	1	31	11 dB

Clock Divider/Voltage Adjust Register

This register controls the divider value for the programmable switched capacitor filter clock divider, the low battery detect threshold select, the voltage reference adjust, and the scrambler bypass mode (MC13110A only). Operation is explained in Figures 126 through 133. Figure 128 describes the operation of the Tx and Rx Audio bits. Note the power–up default bit is set to <0>, which is the scrambler bypass mode.

Low Battery Detect

The low battery detect circuit can be operated in programmable and non–programmable threshold modes. The non–programmable threshold mode is only available in the 52 QFP package. In this mode, there are two low battery detect comparators and the threshold values are set by external resistor dividers which are connected to the REF1 and REF2 pins. In the programmable threshold mode, several different threshold levels may be selected through the “Low Battery Detect Threshold Register” as shown in Figure 127. The power–on default value for this register is <0,0,0> and is the non–programmable mode. Figure 129 shows equivalent schematics for the programmable and non–programmable operating modes.

Figure 126. Clock Divider/Voltage Adjust Latch Bits

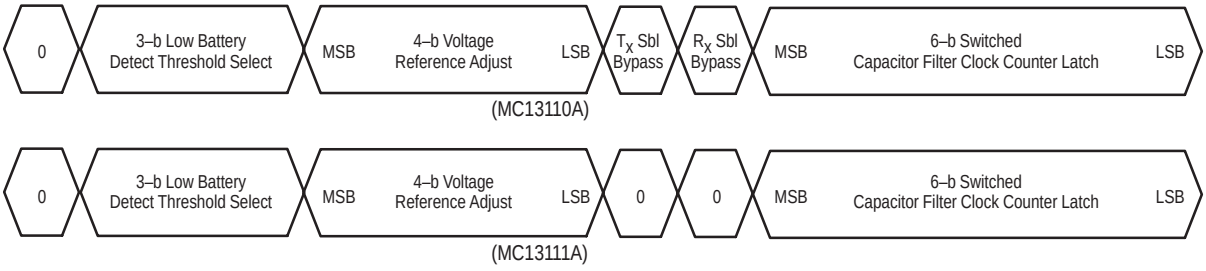


Figure 127. Low Battery Detect Threshold Selection

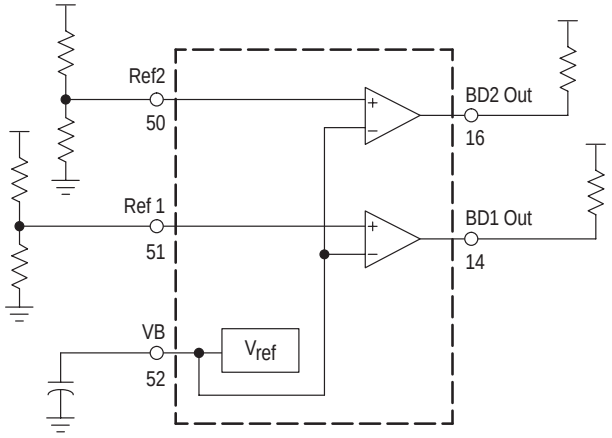
Low Battery Detect Threshold Select Bit #2	Low Battery Detect Threshold Select Bit #1	Low Battery Detect Threshold Select Bit #0	Select #	Operating Mode	Nominal Low Battery Detect Threshold Value (V)
0	0	0	0	Non–Programmable	N/A
0	0	1	1	Programmable	2.850
0	1	0	2	Programmable	2.938
0	1	1	3	Programmable	3.025
1	0	0	4	Programmable	3.200
1	0	1	5	Programmable	3.288
1	1	0	6	Programmable	3.375
1	1	1	7	Programmable	3.463

NOTE: 17. Nominal Threshold Value is before electronic adjustment.

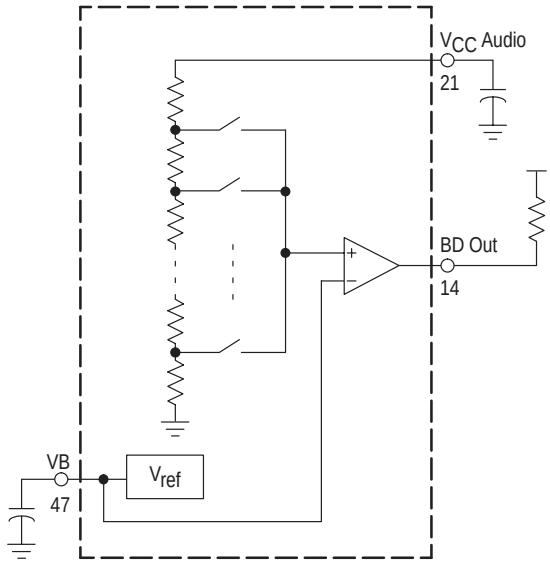
Figure 128. MC13110A Bypass Mode Bit Description (MC13110A Only)

T_X Scrambler Bypass	1	T_X Scrambler Post–Mixer LPF and Mixer Bypassed
	0	Normal Operation with T_X Scrambler
R_X Scrambler Bypass	1	R_X Scrambler Post–Mixer LPF and Mixer Bypassed
	0	Normal Operation R_X Scrambler

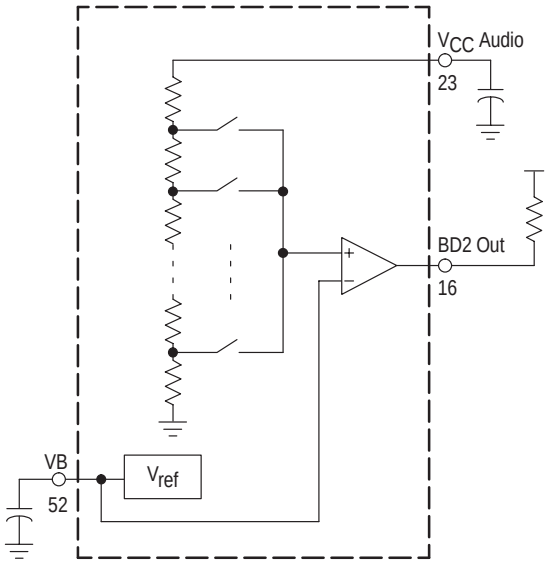
Figure 129. Low Battery Detect Equivalent Schematics



Non–Programmable Threshold Mode: 52–QFP Package



Programmable Threshold Mode: 48–LQFP Package



Programmable Threshold Mode: 52–QFP Package

Voltage Reference Adjustment

An internal 1.5 V bandgap voltage reference provides the voltage reference for the "BD_1 Out" and "BD_2 Out" low battery detect circuits, the "PLL V_{ref}" voltage regulator, the "V_B" reference, and all internal analog ground references. The initial tolerance of the bandgap voltage reference is ±6%. The tolerance of the internal reference voltage can be improved to ±1.5% through MPU serial interface programming. During final test of the telephone, the battery detect threshold is measured. Then, the internal reference voltage value is adjusted electronically through the MPU serial interface to achieve the desired accuracy level. The voltage reference register value should be stored in ROM during final test so that it can be reloaded each time the MC13110A or MC13111A is powered up (see Figure 130).

Figure 130. Bandgap Voltage Reference Adjustment

V_{ref}Adj. Bit #3	V_{ref}Adj. Bit #2	V_{ref}Adj. Bit #1	V_{ref}Adj. Bit #0	V_{ref}Adj. #	V_{ref} Adj. Amount
0	0	0	0	0	–9.0%
0	0	0	1	1	–7.8%
0	0	1	0	2	–6.6%
0	0	1	1	3	–5.4%
0	1	0	0	4	–4.2%
0	1	0	1	5	–3.0%
0	1	1	0	6	–1.8%
0	1	1	1	7	–0.6%
1	0	0	0	8	+0.6 %
1	0	0	1	9	+1.8 %
1	0	1	0	10	+3.0 %
1	0	1	1	11	+4.2 %
1	1	0	0	12	+5.4 %
1	1	0	1	13	+6.6 %
1	1	1	0	14	+7.8 %
1	1	1	1	15	+9.0 %

Switched Capacitor Filter Clock Programming

A block diagram of the switched capacitor filter clock divider is show in Figure 131. There is a fixed divide by 2 after the programmable divider. The switched capacitor filter clock value is given by the following equation;

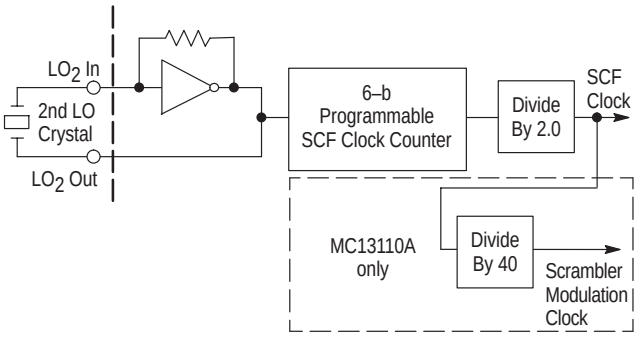
(SCF Clock) = F(2nd LO) / (SCF Divider Value * 2).

The scrambler modulation clock frequency (SMCF) is proportional to the SCF clock. The following equation defines its value:

SMCF = (SCF Clock)/40

The SCF divider should be set to a value which brings the SCF Clock as close to 165.16 kHz as possible. This is based on the 2nd LO frequency which is chosen in Figure 114.

Figure 131. SCF Clock Divider Circuit



Corner Frequency Programming for MC13110A and MC13111A

Four different corner frequencies may be selected by programming the SCF Clock divider as shown in Figures 132 and 133. It is important to note, that all filter corner frequencies will change proportionately with the SCF Clock Frequency and Scrambler Modulation Frequency. The power–up default SCF Clock divider value is 31.

Figure 132. Corner Frequency Programming for 10.240 MHz 2nd LO

MC13110A							
MC13111A							
SCF Clock Divider	Total Divide Value	SCF Clock Freq. (kHz)	R_X Upper Corner Frequency (kHz)	T_X Upper Corner Frequency (kHz)	Scrambler Modulation Frequency (Clk/40) (kHz)	Scrambler Lower Corner Frequency (Hz)	Scrambler Upper Corner Frequency (kHz)
29	58	176.55	4.147	3.955	4.414	267.2	3.902
30	60	170.67	4.008	3.823	4.267	258.3	3.772
31	62	165.16	3.879	3.700	4.129	250.0	3.650
32	64	160.00	3.758	3.584	4.000	242.2	3.536

NOTE: 18. All filter corner frequencies have a tolerance of ±3%.
19. R_X and T_X Upper Corner Frequencies are the same corner frequencies for the MC13110A in scrambler bypass

Figure 133. Corner Frequency Programming for 11.15 MHz 2nd LO

MC13110A / MC13111A							
SCF Clock Divider	Total Divide Value	SCF Clock Freq. (kHz)	R_X Upper Corner Frequency (kHz)	T_X Upper Corner Frequency (kHz)	Scrambler Modulation Frequency (Clk/40) (kHz)	Scrambler Lower Corner Frequency (Hz)	Scrambler Upper Corner Frequency (kHz)
32	64	174.22	4.092	3.903	4.355	263.7	3.850
33	66	168.94	3.968	3.785	4.223	255.7	3.733
34	68	163.97	3.851	3.673	4.099	248.2	3.624
35	70	159.29	3.741	3.568	3.982	241.1	3.520

NOTES: 20. All filter corner frequencies have a tolerance of ±3%.
21. R_X and T_X Upper Corner Frequencies are the same corner frequencies for the MC13110A in scrambler bypass

Figure 134. Auxiliary Register Latch Bits

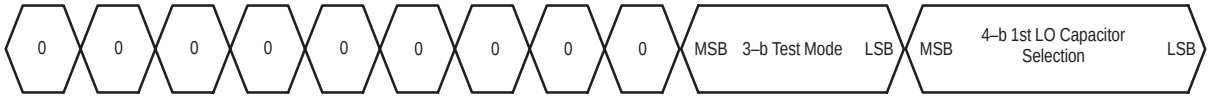


Figure 135. Digital Test Mode Description

TM #	TM 2	TM 1	TM 0	Counter Under Test or Test Mode Option	"T_X V_{CO}" Input Signal	"Clk Out" Output Expected
0	0	0	0	Normal Operation	>200 mVpp	–
1	0	0	1	R_X Counter	0 to 2.5 V	Input Frequency/R_X Counter Value
2	0	1	0	T_X Counter	0 to 2.5 V	Input Frequency/T_X Counter Value
3	0	1	1	Reference Counter + Divide by 4/25	0 to 2.5 V	Input Frequency/Reference Counter Value * 100
4	1	0	0	SC Counter	0 to 2.5 V	Input Frequency/SC Counter Value * 2
5	1	0	1	ALC Gain = 10 Option	N/A	N/A
6	1	1	0	ALC Gain = 25 Option	N/A	N/A

Auxiliary Register

The auxiliary register contains a 4–bit First LO Capacitor Selection latch and a 3–bit Test Mode latch. Operation of these latch bits are explained in Figures 134, 135 and 136.

Test Modes

Test modes are be selected through the 3–bit Test Mode Register. In test mode, the "T_X VCO" input pin is multiplexed to the input of the counter under test. The output of the counter under test is multiplexed to the "Clk Out" output pin so that each counter can be individually tested. **Make sure test mode bits are set to "0's" for normal operation.** Test mode operation is described in Figure 135. During normal operation, the "T_X VCO" input can be a minimum of 200 mVpp at 80 MHz and should be AC coupled. Input signals should be standard logic levels of 0 to 2.5 V and a maximum frequency of 16 MHz.

First Local Oscillator Programmable Capacitor Selection

There is a very large frequency difference between the minimum and maximum channel frequencies in the 25 Channel U.S. standard. The internal varactor adjustment range is not large enough to accommodate this large frequency span. An internal capacitor with 15 programmable capacitor values can be used to cover the 25 channel frequency span without the need to add external capacitors and switches. The programmable internal capacitor can also be used to eliminate the need to use an external variable capacitor to adjust the 1st LO center frequency during telephone assembly. Figure 32 shows the schematic of the 1st LO tank circuit. Figure 136 shows the register control bit values.

The internal programmable capacitor is composed of a matrix bank of capacitors that are switched in as desired. Programmable capacitor values between about 0 and 16 pF can be selected in steps of approximately 1.1 pF. The internal parallel resistance values in the table can be used to calculate the quality factor (Q) of the oscillator if the Q of the external inductor is known. The temperature coefficient of the varactor is 0.08%/°C. The temperature coefficient of the internal programmable capacitor is negligible. Tolerance on the varactor and programmable capacitor values is ±15%.

Figure 136. First Local Oscillator Internal Capacitor Selection

1st LO Cap. Bit 3	1st LO Cap. Bit 2	1st LO Cap. Bit 1	1st LO Cap. Bit 0	1st LO Cap. Select	Internal Programmable Capacitor Value (pF)	Varactor Value over 0.3 to 2.5 V (pF)	Equivalent Internal Parallel Resistance at 40 MHz (kΩ)	Equivalent Internal Parallel Resistance at 51 MHz (kΩ)
0	0	0	0	0	0.0	9.7 to 5.8	1200	736
0	0	1	0	2	0.6	9.7 to 5.8	79.3	48.8
0	0	0	1	1	1.7	9.7 to 5.8	131	80.8
0	1	0	1	5	2.8	9.7 to 5.8	31.4	19.3
0	1	1	0	6	3.9	9.7 to 5.8	33.8	20.8
0	1	1	1	7	4.9	9.7 to 5.8	66.6	41
0	1	0	0	4	6.0	9.7 to 5.8	49.9	30.7
0	0	1	1	3	7.1	9.7 to 5.8	40.7	25.1
1	0	0	0	8	8.2	9.7 to 5.8	27.1	16.7
1	0	0	1	9	9.4	9.7 to 5.8	21.6	13.3
1	0	1	0	10	10.5	9.7 to 5.8	20.5	12.6
1	0	1	1	11	11.6	9.7 to 5.8	18.6	11.5
1	1	0	0	12	12.7	9.7 to 5.8	17.2	10.6
1	1	0	1	13	13.8	9.7 to 5.8	15.8	9.7
1	1	1	0	14	14.9	9.7 to 5.8	15.3	9.4
1	1	1	1	15	16.0	9.7 to 5.8	14.2	8.7

OTHER APPLICATIONS INFORMATION

PCB Board Lay–Out Considerations

The ideal printed circuit board (PCB) lay out would be double–sided with a full ground plane on one side. The ground plane would be divided into separate sections to prevent any audio signal from feeding into the first local oscillator via the ground plane. Leaded components, can likewise, be inserted on the ground plane side to improve shielding and isolation from the circuit side of the PCB. The opposite side of the PCB is typically the circuit side. It has the interconnect traces and surface mount components. In cases where cost allows, it may be beneficial to use multi–layer boards to further improve isolation of components and sensitive sections (i.e. RF and audio). For the CT–0 band, it is also permissible to use single–sided PC layouts, but with continuous full ground fill in and around the components.

The proper placement of certain components specified in the application circuit may be very critical. In a lay–out design, these components should be placed before the other less critical components are inserted. It is also imperative that all RF paths be kept as short as possible. Finally, the MC13110A and MC13111A ground pins should be tied to ground at the pins and V_{CC} pins should have adequate decoupling to ground as close to the IC as possible. In mixed mode systems where digital and RF/Analog circuitry are present, the V_{CC} and V_{EE} buses need to be ac–decoupled and isolated from each other. The design must also take great caution to avoid interference with low level analog circuits. The receiver can be particularly susceptible to interference as they respond to signals of only a few microvolts. Again, be sure to keep the dc supply lines for the digital and analog portions separate. Avoid ground paths carrying common digital and analog currents, as well.

Component Selection

The evaluation circuit schematics specify particular components that were used to achieve the results shown in the typical curves and tables, but alternate components should give similar results. The MC13110A and MC13111A IC are capable of matching the sensitivity, IMD, adjacent channel rejection, and other performance criteria of a multi–chip analog cordless telephone system. For the most part, the same external components are used as in the multi–chip solution.

VB and PLL V_{ref}

VB is an internally generated bandgap voltage. It functions as an ac reference point for the operational amplifiers in the audio section as well as for the battery detect circuitry. This pin needs to be sufficiently filtered to reduce noise and prevent crosstalk between R_X audio to T_X audio signal paths. A practical capacitor range to choose that will minimize crosstalk and noise relative to start up time is 0.5 μf to 10 μf. The start time for a 0.5 μf capacitor is approximately 5.0 ms, while a 10μf capacitor is about 10 ms.

The “PLL V_{ref}” pin is the internal supply voltage for the R_X and T_X PLL’s. It is regulated to a nominal 2.5 V. The “V_{CC} Audio” pin is the supply voltage for the internal voltage regulator. Two capacitors with 10 μF and 0.01 μF values must be connected to the “PLL V_{ref}” pin to filter and stabilize this regulated voltage. The “PLL V_{ref}” pin may be used to power other IC’s as long as the total external load current does not exceed 1.0 mA. The tolerance of the regulated voltage is initially ±8.0%, but is improved to ±4.0% after the internal Bandgap voltage reference is adjusted electronically through the MPU serial interface. The voltage regulator is turned off in the Standby and Inactive modes to reduce current drain. In these modes, the “PLL V_{ref}” pin is internally connected to the “V_{CC} Audio” pin (i.e., the power supply voltage is maintained but is now unregulated).

It is important to note that the momentary drop in voltage below 2.5 V during this transition may affect initial PLL lock times and also may trigger the reset. To prevent this, the PLL V_{ref} capacitor described above should be kept the same or larger than the VB capacitor, say 10 μf as shown in the evaluation and application diagrams.

DC Coupling

Choosing the right coupling capacitors for the compander is also critical. The coupling capacitors will have an affect on the audio distortion, especially at lower audio frequencies. A useful capacitor range for the compander timing capacitors is 0.1 μf to 1.0 μf. It is advised to keep the compander capacitors the same value in both the handset and baseset applications.

All other dc coupling capacitors in the audio section will form high pass filters. The designer should choose the overall cut off frequency (–3.0 dB) to be around 200 Hz. Designing for lower cut off frequencies may add unnecessary cost and capacitor size to the design, while selecting too high of a cut off frequency may affect audio quality. It is not necessary or advised to design each audio coupling capacitors for the same cut off frequency. Design for the overall system cut off frequency. (Note: Do not expect the application, evaluation, nor production test schematics to necessarily be the correct capacitor selections.) The goals of these boards may be different than the systems approach a designer must consider.

For the supply pins (V_{CC} Audio and V_{CC} RF) choose a 10 μf in parallel with a high quality 0.01 μf capacitor. Separation of the these two supply planes is essential, too. This is to prevent interference between the RF and audio sections. It is always a good design practice to add additional coupling on each supply plane to ground as well.

The IF limiter capacitors are recommended to be 0.1 μf. Smaller values lower the gain of the limiter stage. The –3.0 dB limiting sensitivity and SINAD may be adversely affected.

Figure 138. Evaluation Board Schematic

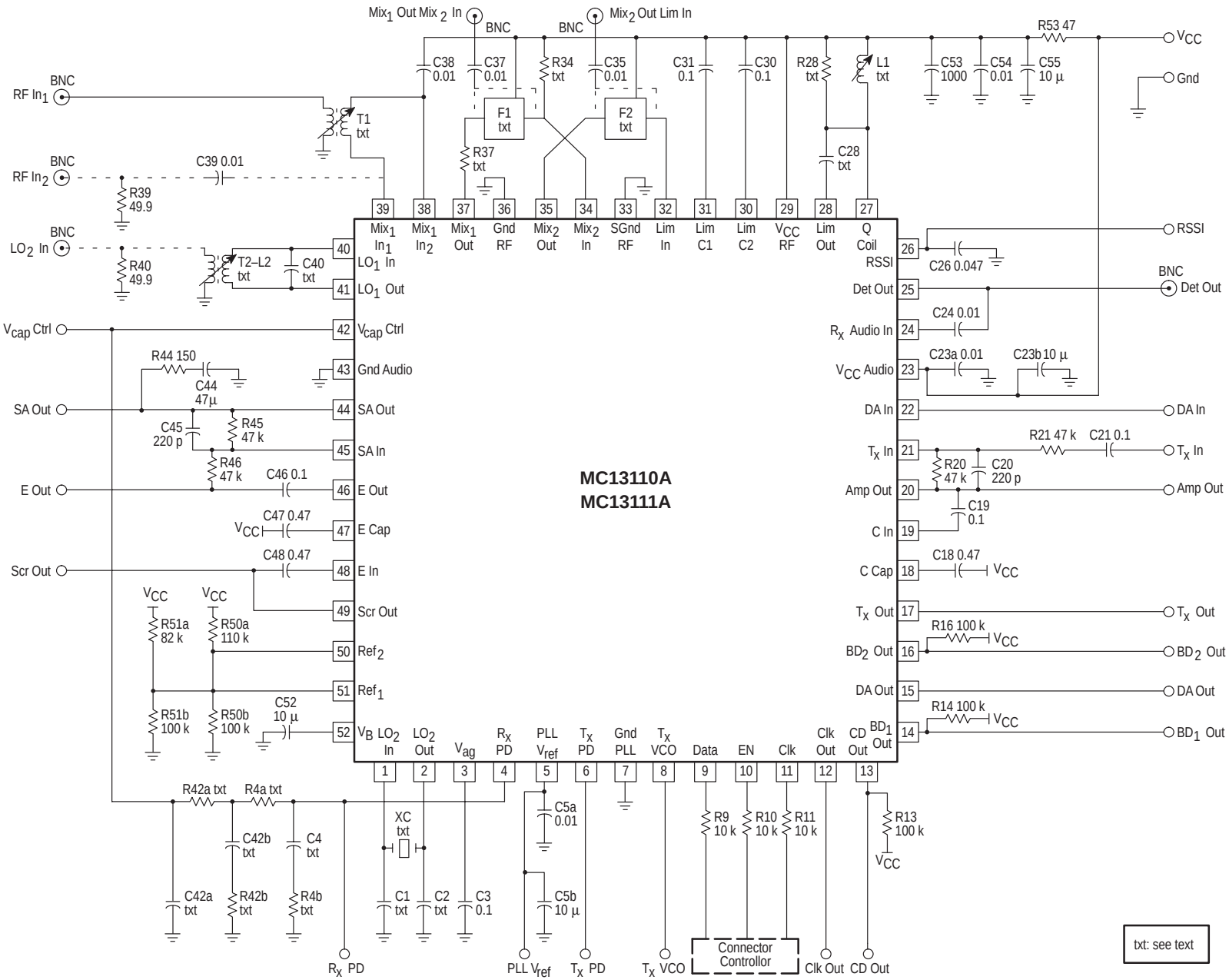


Figure 138. Evaluation Board Bill of Materials for U.S. and French Application

Comp. Number	USA Application Handset		French Application Base		
	RF (50 Ω)	RF Matched	RF Crystal (50 Ω)	RF Ceramic (50 Ω)	RF Matched
INPUT MATCHING					
T1	n.m.	Toko 1:5 292GNS–765A0	n.m.	n.m.	Toko 1:5 292GNS–765A0
C38	0.01	n.m.	0.01	0.01	n.m.
C39	0.01	n.m.	0.01	0.01	n.m.
10.7 MHz FILTER					
F1	Ceramic	Ceramic	Crystal	Ceramic	Ceramic
R37	0	0	1.2 k	0	0
R34	360	360	3.01 k	360	360
450 kHz FILTER					
F2	4 Element Murata E	4 Element Murata E	4 Element Murata G	4 Element Murata G	4 Element Murata G
DEMODULATOR					
L1	Q Coil Toko 7MCS–8128Z	Q Coil Toko 7MCS–8128Z	Ceramic Murata CDBM 450C34	Ceramic Murata CDBM 450C34	Ceramic Murata CDBM 450C34
R28	22.1 k	22.1 k	2.7 k	2.7 k	2.7 k
C28	10 p	10 p	390 p	390 p	390 p
OSCILLATOR					
Xtal	10.24 C1 = 10 p	10.24 C1 = 10 p	11.15 C1 = 18 p	11.15 C1 = 18 p	11.15 C1 = 18 p
C2	18 p	18 p	33 p	33 p	33 p
C1	5–25 p	5–25 p	15 p + 5–25 p	15 p + 5–25 p	15 p + 5–25 p
FIRST LO					
L2	0.47 Toko T1370	0.47 Toko T1370	0.22 Toko T1368	0.22 Toko T1368	0.22 Toko T1368
C40 HS/BS	HS: 27 pF BS: 22 pF	HS: 27 pF BS: 22 pF	BS: 100 p HS: 68 pF	BS: 100 p HS: 68 pF	BS: 100 p HS: 68 pF
LOOP FILTER HANDSET/BASESET					
R4a	HS: 0 BS: 0	HS: 0 BS: 0	HS: 0 BS: 0	HS: 0 BS: 0	HS: 0 BS: 0
R4b	HS: 0 BS: 0	HS: 0 BS: 0	HS: 0 BS: 0	HS: 0 BS: 0	HS: 0 BS: 0
C4	HS: 6800 BS: 8200	HS: 6800 BS: 8200	HS: 8600 BS: 6800	HS: 8600 BS: 6800	HS: 8600 BS: 6800
R42a	HS: 100 k BS: 100 k	HS: 100 k BS: 100 k	HS: 100 k BS: 100 k	HS: 100 k BS: 100 k	HS: 100 k BS: 100 k
R42b	HS: 22 k BS: 18 k	HS: 22 k BS: 18 k	HS: 18 k BS: 22 k	HS: 18 k BS: 22 k	HS: 18 k BS: 22 k
C42a	HS: 1000 BS: 1000	HS: 1000 BS: 1000	HS: 1000 BS: 1000	HS: 1000 BS: 1000	HS: 1000 BS: 1000
C42b	HS: 0.068 BS: 0.082	HS: 0.068 BS: 0.082	HS: 0.082 BS: 0.068	HS: 0.082 BS: 0.068	HS: 0.082 BS: 0.068

APPENDIX B
APPLICATIONS CIRCUIT

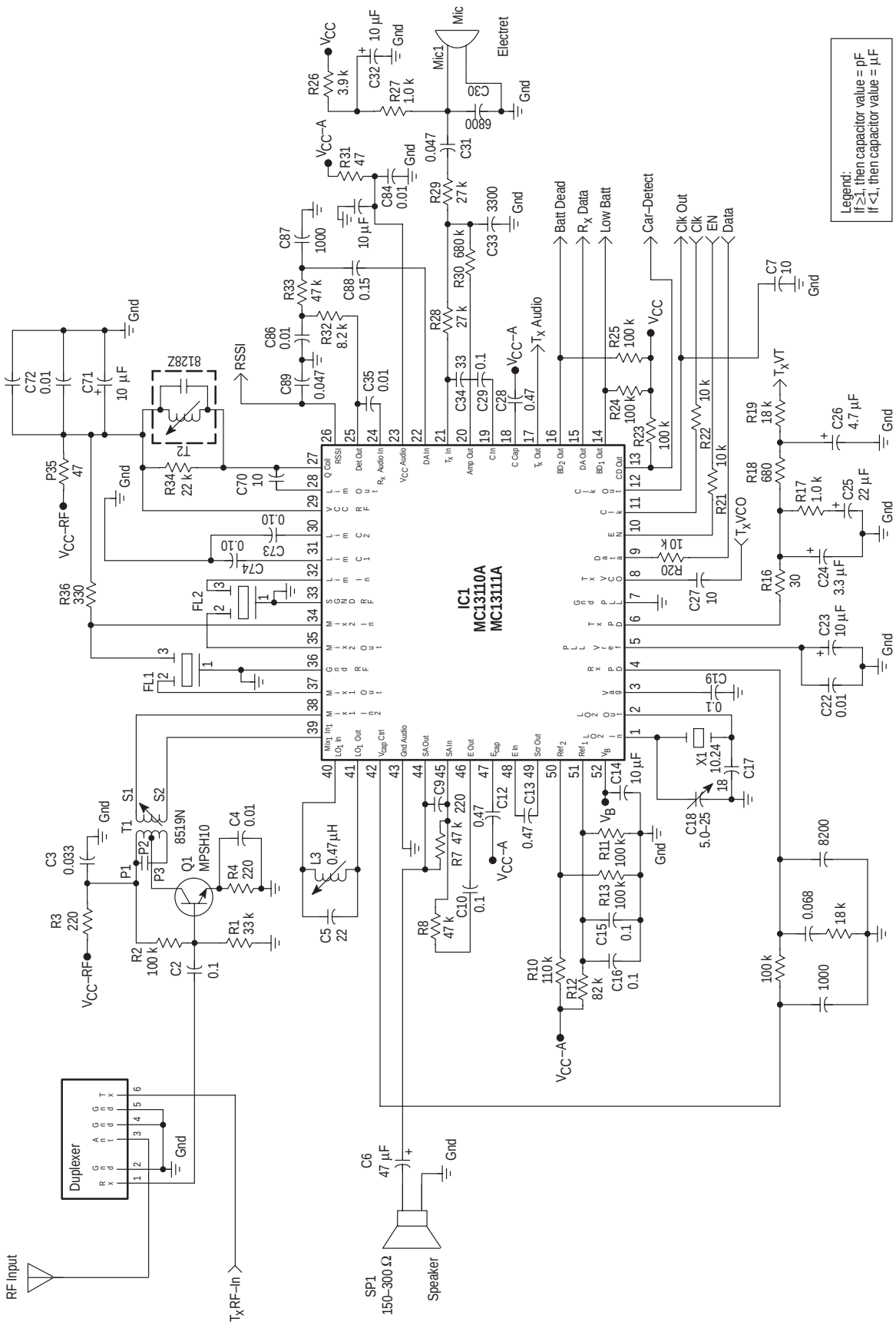
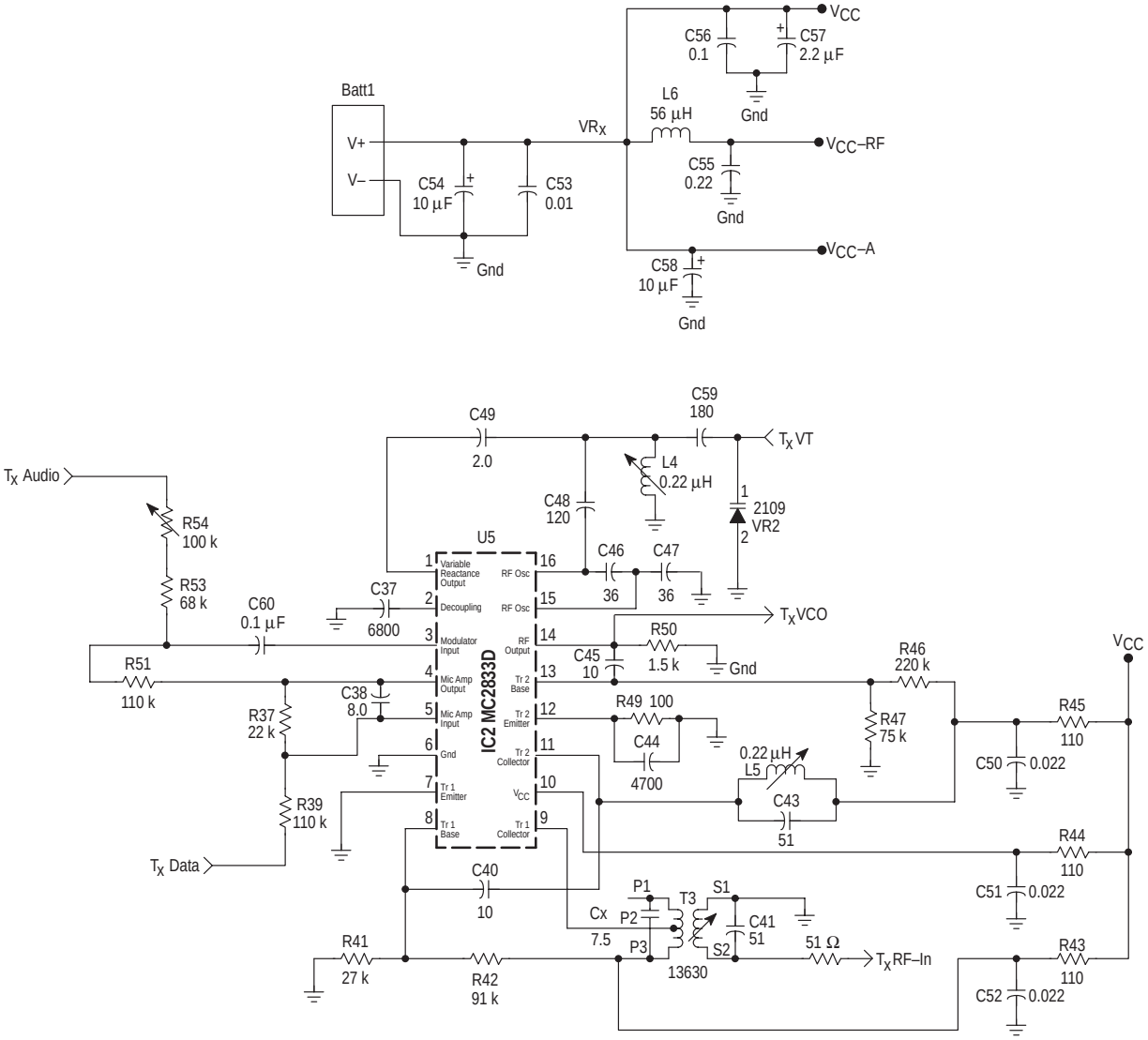


Figure 140. Basic Cordless Telephone Transceiver Application Circuit

Figure 140. Basic Cordless Telephone Transceiver Application Circuit (continued)



APPENDIX C – MEASUREMENT OF COMPANDER ATTACK/DECAY TIME

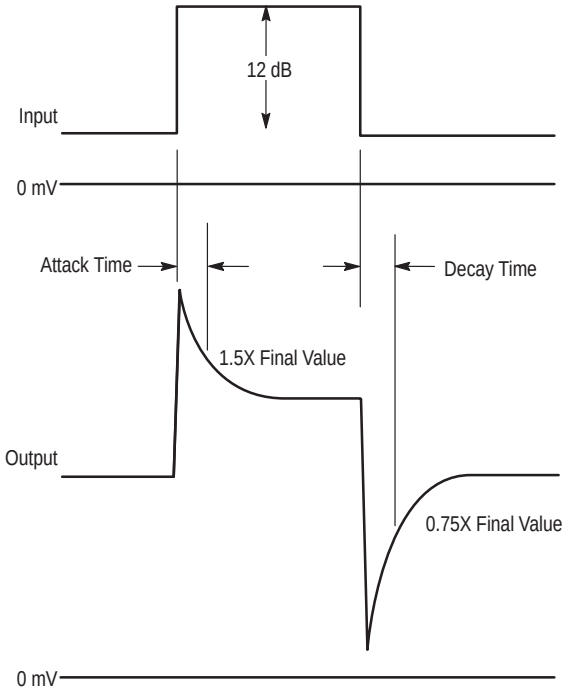
This measurement definition is based on EIA/CCITT recommendations.

Compressor Attack Time

For a 12 dB step up at the input, attack time is defined as the time for the output to settle to 1.5X of the final steady state value.

Compressor Decay Time

For a 12 dB step down at the input, decay time is defined as the time for the input to settle to 0.75X of the final steady state value.

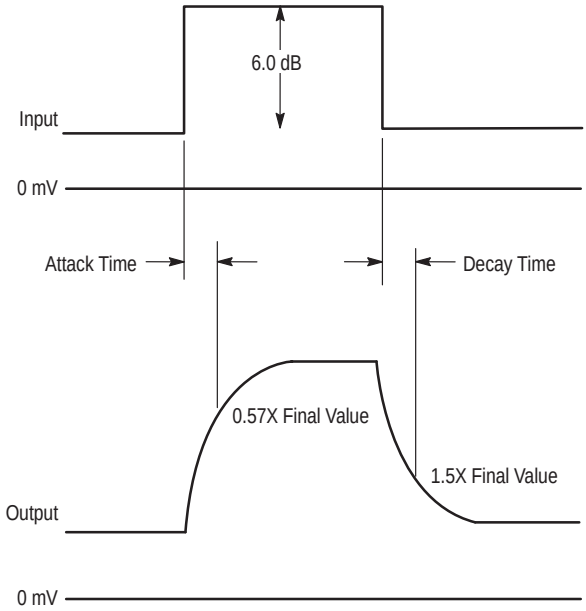


Expander Attack

For a 6.0 dB step up at the input, attack time is defined as the time for the output to settle to 0.57X of the final steady state value.

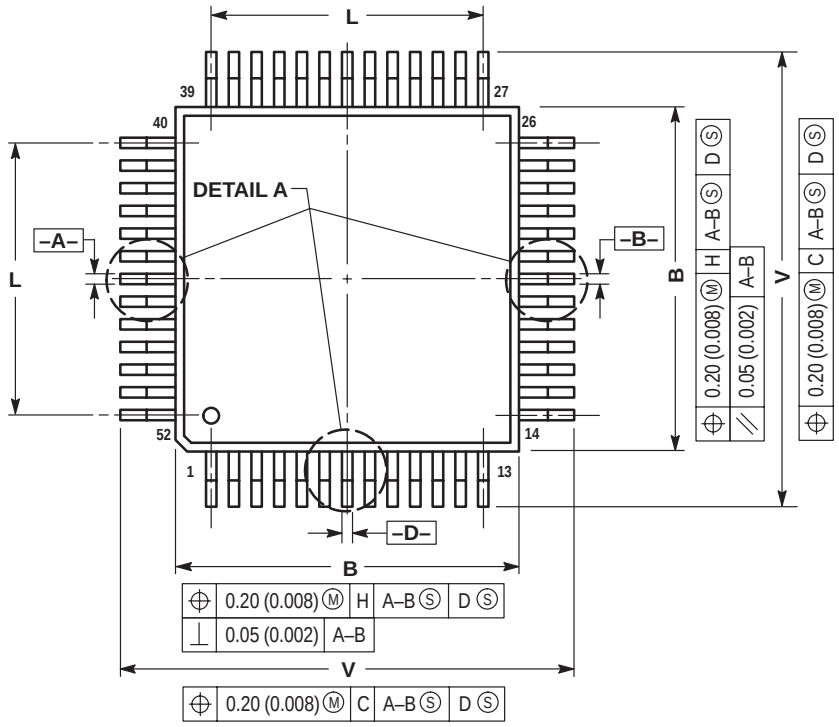
Expander Decay

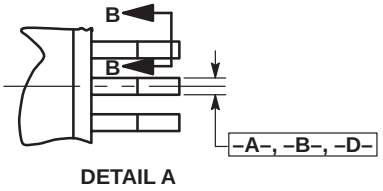
For a 6.0 dB step down at the input, decay time is defined as the time for the output to settle to 1.5X of the final steady state value.



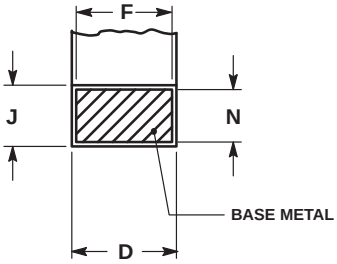
OUTLINE DIMENSIONS

FB SUFFIX
PLASTIC PACKAGE
CASE 848B–04
(QFP–52)
ISSUE C



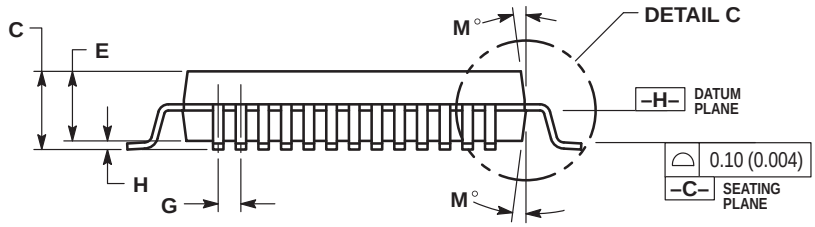


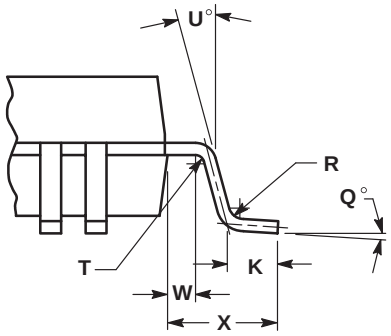
DETAIL A



0.02 (0.008) M C A–B S D S

SECTION B–B





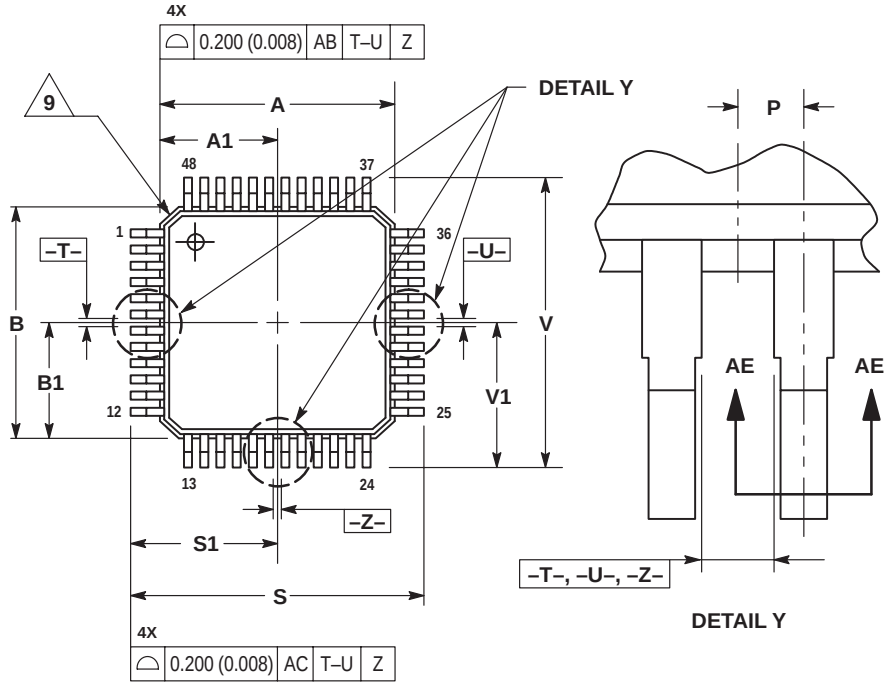
DETAIL C

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –A–, –B– AND –D– TO BE DETERMINED AT DATUM PLANE –H–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –C–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.90	10.10	0.390	0.398
B	9.90	10.10	0.390	0.398
C	2.10	2.45	0.083	0.096
D	0.22	0.38	0.009	0.015
E	2.00	2.10	0.079	0.083
F	0.22	0.33	0.009	0.013
G	0.65 BSC		0.026 BSC	
H	—	0.25	—	0.010
J	0.13	0.23	0.005	0.009
K	0.65	0.95	0.026	0.037
L	7.80 REF		0.307 REF	
M	5 °	10 °	5 °	10 °
N	0.13	0.17	0.005	0.007
Q	0 °	7 °	0 °	7 °
R	0.13	0.30	0.005	0.012
S	12.95	13.45	0.510	0.530
T	0.13	—	0.005	—
U	0 °	—	0 °	—
V	12.95	13.45	0.510	0.530
W	0.35	0.45	0.014	0.018
X	1.6 REF		0.063 REF	

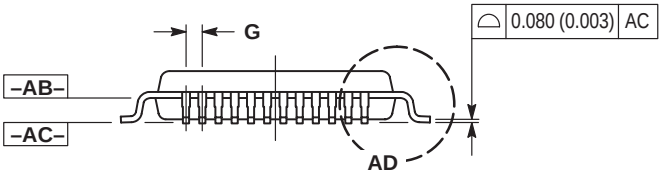
OUTLINE DIMENSIONS

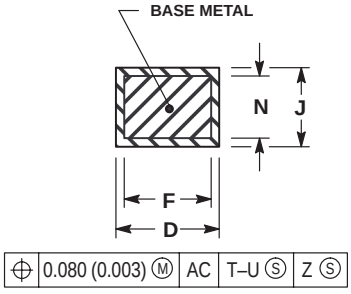
FTA SUFFIX
PLASTIC PACKAGE
CASE 932–02
(LQFP–48)
ISSUE D



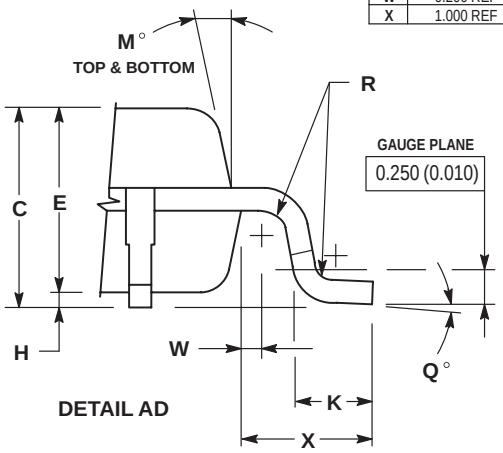
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –AB– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –T–, –U–, AND –Z– TO BE DETERMINED AT DATUM PLANE –AB–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –AC–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –AB–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.350 (0.014).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.000 BSC		0.276 BSC	
A1	3.500 BSC		0.138 BSC	
B	7.000 BSC		0.276 BSC	
B1	3.500 BSC		0.138 BSC	
C	1.400	1.600	0.055	0.063
D	0.170	0.270	0.007	0.011
E	1.350	1.450	0.053	0.057
F	0.170	0.230	0.007	0.009
G	0.500 BASIC		0.020 BASIC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.500	0.700	0.020	0.028
M	12 °REF		12 °REF	
N	0.090	0.160	0.004	0.006
P	0.250 BASIC		0.010 BASIC	
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	9.000 BSC		0.354 BSC	
S1	4.500 BSC		0.177 BSC	
V	9.000 BSC		0.354 BSC	
V1	4.500 BSC		0.177 BSC	
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	





SECTION AE–AE



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