# ANSWERS TO SELECTED PROBLEMS

## CHAPTER 1

1.1 (a) Analog (b) Digital (c) Analog (d) Digital
(e) Analog (f) Digital (g) Digital

1.2 (c) (i) AND (ii) OR (iii) NOT (iv) EX-OR

1.4 (a)

| Inputs | | Output |
|---|---|---|
| *A* | *B* | *Y* |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |
| NOR | | |

(b)

| Inputs | | Output |
|---|---|---|
| *A* | *B* | *Y* |
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |
| NAND | | |

(c)

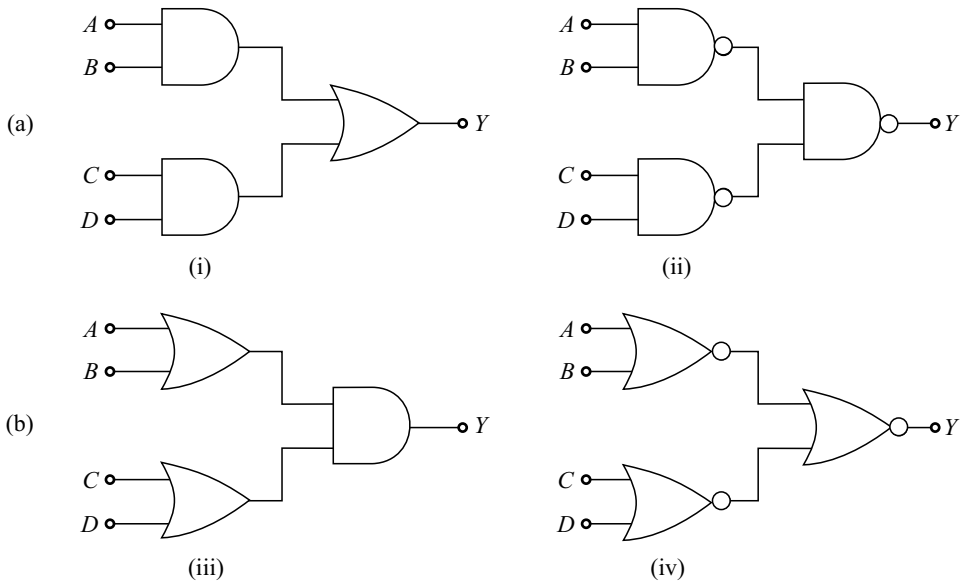
| Inputs | | Output |
|---|---|---|
| *A* | *B* | *Y* |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |
| AND | | |

(d)

| Inputs | | Output |
|---|---|---|
| *A* | *B* | *Y* |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |
| OR | | |

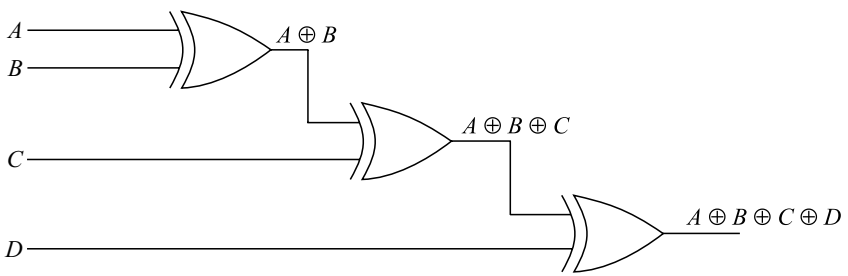
1.6 (a) NAND, NOR (b) AND (c) NAND (d) OR

1.13




1.14 (a) $A \cdot B = B \cdot A$ Commutative
$(A \cdot B) \cdot C = A \cdot (B \cdot C)$ Associative
(b) $A + B = B + A$ Commutative
$(A + B) + C = A + (B + C)$ Associative
(c) $A \oplus B = B \oplus A$ Commutative
$(A \oplus B) \oplus C = A \oplus (B \oplus C)$ Associative

1.16




1.18 $2^N$

1.19 (a) – (i) 14

1.20 (a) (i) 7408, 7432 (ii) 7400
(b) (i) 7432, 7408 (ii) 7402

1.21 *Logic Circuit A*

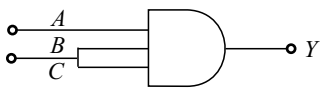
0.4 V = 0
2 V = 1

*Logic Circuit B*

–0.75 V = 1
–1.55 V = 0

1.22

| Inputs | | | Output | | | |
|---|---|---|---|---|---|---|
| *A* | *B* | *C* | *AND* (*a*) | *OR* (*b*) | *NAND* (*c*) | *NOR* (*d*) |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 |

1.23 (a) 

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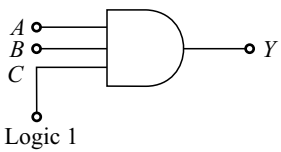
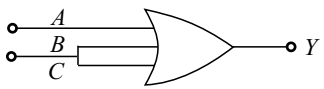



(b) 

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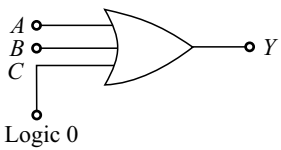
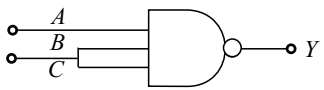
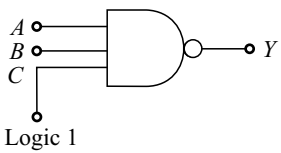
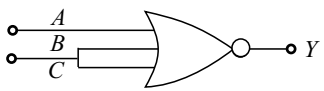



(c) 

or



(d) 

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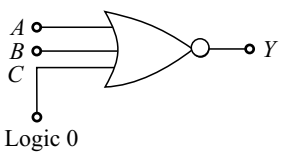
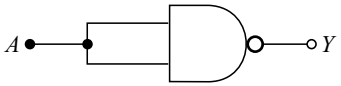


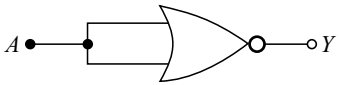

1.25 (a) Active-high
(b) Active-low
(c) Active-high
(d) Active-low

1.26 (a) Active-low
(b) Active-high
(c) Active-low
(d) Active-high

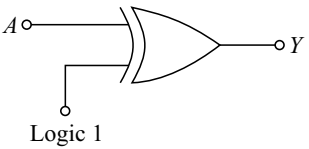
1.29 (a) Yes



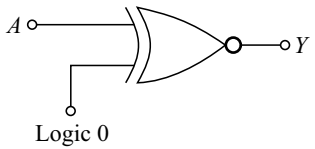

(b) Yes




(c) Yes




(d) Yes




(e) No

(f) No

## CHAPTER 2

2.1 (a) 57 (b) 41 (c) 254 (d) 100
(e) 13.1875 (f) 10.625 (g) 0.875

2.2 (a) 100101 (b) 11111111 (c) 1111
(d) 11010.01 (e) 1011.11 (f) 0.00011001

2.3 (a) 11000 (b) 10000.0001

2.5 (a) $(567)_8 = (101110111)_2$
(b) $(371)_8 = (011111001)_2$
(c) $(33.1)_8 = (011011.001)_2$

2.6 (a) $(334.52)_8 = (220.65625)_{10}$
(b) $(123.25)_8 = (83.328125)_{10}$
(c) $(263)_8 = (179)_{10}$

2.7 (a) $(177)_{16} = (000101110111)_2$
(b) $(F9)_{16} = (11111001)_2$
(c) $(1B.2)_{16} = (00011011.0010)_2$

2.9 (a) 01000110
(b) 001100100111.10001001
(c) 00100000.001100000101

2.10 (a) 01111001
(b) 011001011010.10111100
(c) 01010011.011000111000

2.11 111001

2.12 10011100101100001110110010100 0

2.16 (a) 6 (b) 8

2.19 $100 \times 20 \times 8$ bits

2.20 924 bits

2.21 Code *A* has a minimum distance of 2 and its parity is odd. The words to be added are 0111, 1011, 1101, and 1110.

2.22 4; 1, 2, 4, and 8

2.23

| **Decimal digit** | **Position →** | **1** $p_1$ | **2** $p_2$ | **3** $n_1$ | **4** $p_3$ | **5** $n_2$ | **6** $n_3$ | **7** $n_4$ |
|---|---|---|---|---|---|---|---|---|
| 0 | | 1 | 1 | 0 | 1 | 0 | 0 | 0 |
| 1 | | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 2 | | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| 3 | | 0 | 1 | 0 | 1 | 0 | 1 | 1 |
| 4 | | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 5 | | 1 | 0 | 0 | 1 | 1 | 0 | 1 |
| 6 | | 0 | 0 | 0 | 1 | 1 | 1 | 0 |
| 7 | | 1 | 1 | 0 | 0 | 1 | 1 | 1 |
| 8 | | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| 9 | | 1 | 1 | 1 | 0 | 0 | 0 | 1 |

2.24 (a) 1

2.25 (a) 111101001010
(b) 000000000000
(c) 111011101111

2.26 (a) 01011010
(b) 10000110
(c) 11110100

## CHAPTER 3

3.2 (a) 36 mV (b) 5.14%

3.3 (a) 5.232 mA (b) 161.6%

3.4 119.73 mV

3.5 (a) $10^{-9}$ C (b) 1.099 μs

3.6 (a)

| *A* | *B* | *Y* |
|---|---|---|
| LOW | LOW | LOW |
| LOW | HIGH | HIGH |
| LOW | LOW | HIGH |
| HIGH | HIGH | HIGH |

(b) OR operation

3.7 (a) Active region; Saturation region
(b) 4.7 kΩ
(c) 127.27 kΩ

3.8 (a) $V_{BB} \leq 0.5$ V
(b) 0.5 V < $V_{BB}$ < 3.25 V
(c) $V_{BB} \geq 3.25$ V

3.9 233.3

3.10 Active region
$I_C = 8.43 \times 10^{-2}$ mA, $I_E \approx -8.43 \times 10^{-2}$ mA
$I_B = 8.43 \times 10^{-4}$ mA

3.12 (a) 1.05 V (b) 3.8 V (c) 0.3 mA

3.13 (a) 5 V (b) 0 V (c) 0 V (d) NOR

3.14 (a) Saturation region (b) Saturation region

(c) Active region

3.15 NO

3.17 $\frac{R_C}{2} C_O$

## CHAPTER 4

4.1 16.48 mW

4.2 (a)

(b)

| | $h_{FE} = 10$ | | $h_{FE} = 20$ | |
|---|---|---|---|---|
| | | **Noise margin** | | **Noise margin** |
| $N$ | $V_O$ | $\|\Delta 1\|$ | $V_O$ | $\|\Delta 1\|$ |
| 5 | 1.14 | 0.1 | 1.14 | 0.22 |
| 6 | 1.09 | 0.05 | 1.09 | 0.17 |
| 7 | 1.055 | 0.015 | 1.055 | 0.135 |
| 8 | < 1.04 | Load gate | 1.026 | 0.106 |
| 9 | < 1.04 | transistors | 0.997 | 0.077 |
| 10 | < 1.04 | not in saturation | 0.984 | 0.064 |

(c) fan-out and noise margin increases with $h_{FE}$.

(d) Noise margin decreases with N.

4.3 (a) 10

4.4 (c) 32 mA

4.6 26

4.9 (a) 35

(b) $\Delta 1 = 0.7$ V, $\Delta 0 = -3.4$ V

(c) 12.045 mW

4.10 (a) $\Delta 1 = 7$ V, $\Delta 0 = -7.2$ V

(b) 76

(c) 29.48 mW

4.13 (a) 3.532 mA (b) 1.025 mA (c) 42.385 mA

4.18 0.72 kΩ ≤ $R_C$ ≤ 1.74 kΩ

4.33 Yes

4.34 Yes

## CHAPTER 5

5.1 (a)

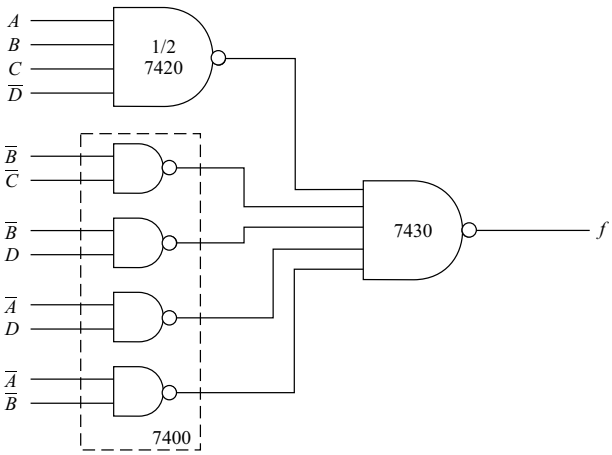
| **Switch** | | **Light** |
|---|---|---|
| $S_1$ | $S_2$ | $L$ |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

5.2 (b) $f = BC + BD$

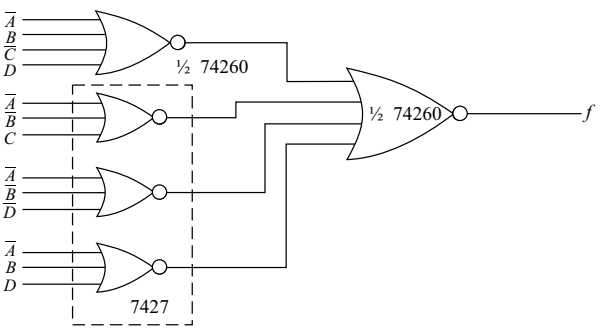
5.3 (b) $f_1 = (\overline{B} + C + D)(\overline{A} + \overline{B} + C)(\overline{A} + B + D)$
$(A + B + \overline{D})(A + \overline{B} + \overline{C})$

$f_2 = (A + \overline{C})(A + B)(\overline{A} + C + \overline{D})(B + \overline{D})$

5.4 (a)




(b)




5.5 (a) one – 7410

(b) $1\frac{1}{3}$ – 7427

5.6 One – 7427

5.7 (c) $f = A + C$

5.8 (a) $f_1 = (A \oplus B) \odot (C \oplus D)$

(b) $f_2 = \overline{A}\,\overline{B} + AB\overline{D} + ACD$

5.9 $E_0 = \overline{A}$

$E_1 = BA + \overline{B}\,\overline{A}$

$E_2 = C\,\overline{B}\,\overline{A} + \overline{C}A + \overline{C}B$

$E_3 = D + CA + CB$

5.10 $A = \overline{E}_0$

$B = \overline{E}_1 E_0 + E_1 \overline{E}_0$

$C = \overline{E}_2 \overline{E}_1 + E_2 E_1 E_0 + E_3 E_1 \overline{E}_0$

$D = E_3 E_2 + E_3 E_1 E_0$

5.11 (a) $f_1 = \overline{C + D}$

(b) $f_2 = (A + \overline{B} + D)\,(B + C + \overline{D})\,(\overline{A} + \overline{C})$

(c) $f_3 = (A + \overline{B} + \overline{C} + \overline{D})\,(B + \overline{C} + D)\,(\overline{A} + B + C)\,(\overline{A} + C + D)$

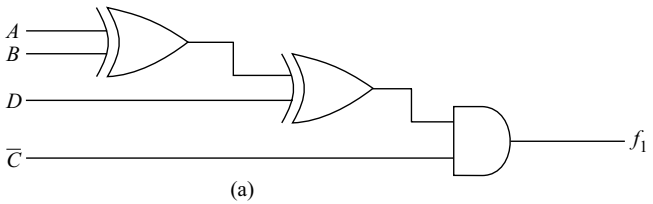
5.12 $f_1 = \overline{A}BE + A\overline{C}\,\overline{E} + ABD + B\overline{C} + A\,\overline{B}C\overline{D}E$

$f_2 = \overline{C}\,\overline{E} + A\,\overline{B}D + \overline{A}\,\overline{D}\,\overline{E} + ADE + \overline{B}CE + CDE + \overline{A}\,\overline{B}E$

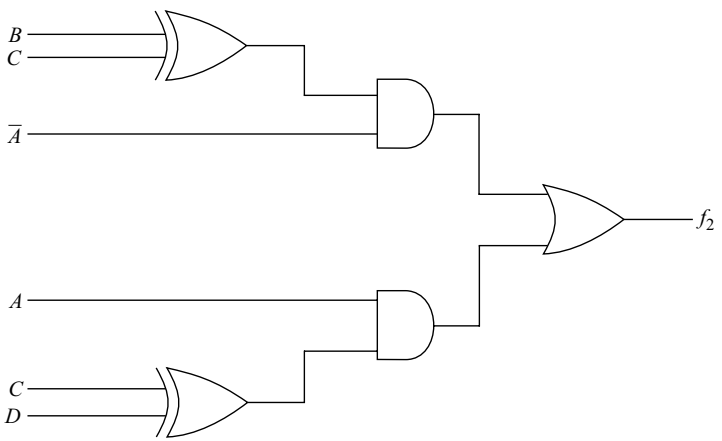
5.14 (a) $f_1 = A\overline{B}\,\overline{C} + \overline{C}D + \overline{B}D + AD$

(b) $f_2 = \overline{A}\,\overline{C}\,\overline{D} + B\overline{C} + \overline{A}B$

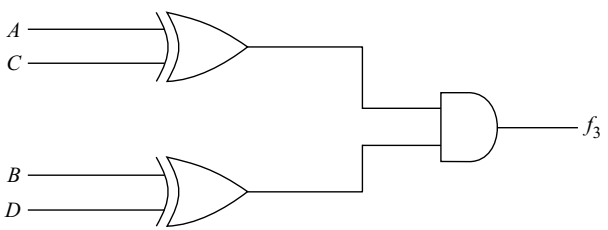
5.15




(a)

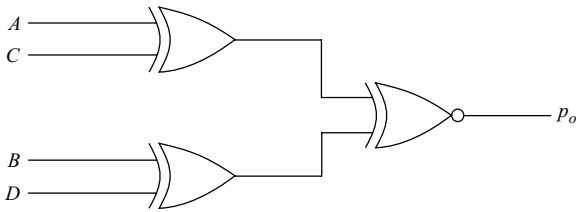



(b)

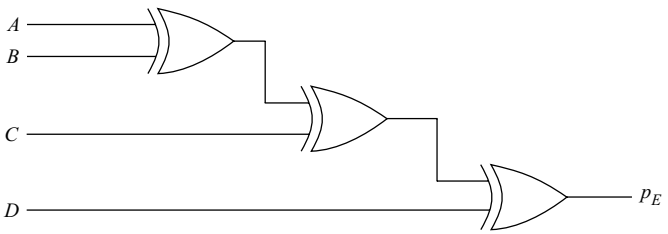



(c)

5.16



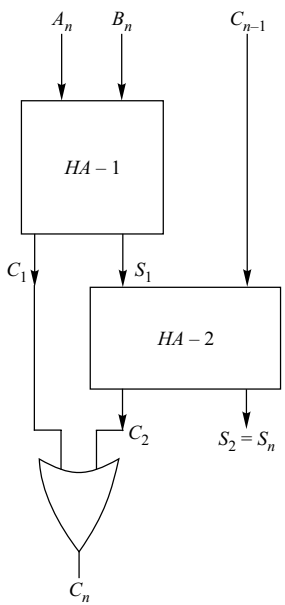

5.17



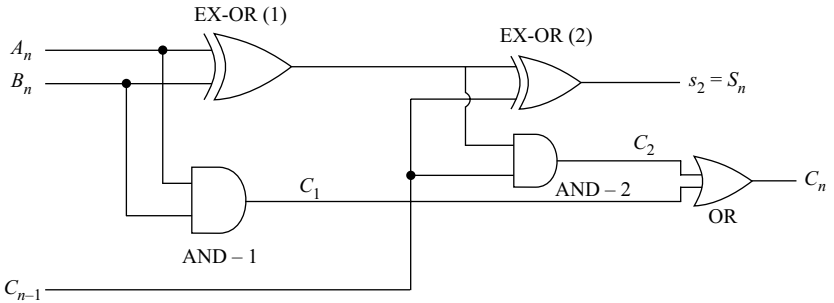

5.18 (a) $f_1 = \overline{A}B\overline{C}\,\overline{D}E + \overline{A}BC\overline{D}F + \overline{A}\,\overline{B}\,\overline{C}DE\overline{F}$

(b) $f_2 = (A + \overline{B} + \overline{C} + D + E + \overline{F})\,(\overline{A} + B + D + E + F)$
$(\overline{A} + B + C + \overline{E} + \overline{F})\,(A + \overline{C} + \overline{D} + E + F)\,(A + B + \overline{C} + E + F)$
$(A + \overline{B} + C + E + F)\,(A + \overline{B} + C + \overline{E} + F)\,(A + B + C + \overline{D})$
$(A + B + \overline{D} + E)\,(B + C + \overline{D} + E)\,(B + C + \overline{D} + F)$
$(A + \overline{B} + C + D)$

5.19 (a)



(b)




5.20 $t_{pd}(S_n) = 40\ ns$
$t_{pd}(C_n) = 40\ ns$

5.21 $f(A, B, C, D) = \overline{A}\,\overline{C} + \overline{A}\,\overline{B}D + \overline{A}B\,\overline{D} + \overline{B}CD + B\,\overline{C}D + BC\,\overline{D} + ACD$

5.22 $f(A, B, C, D) = \overline{B}D + \overline{C}D + AD + A\,\overline{B}\,\overline{C}$

5.23 $f(A, B, C, D, E) = A\,\overline{B}C\,\overline{D}E + A\,\overline{C}\,\overline{E} + \overline{A}BE + ABD + B\,\overline{C}$

5.24 No

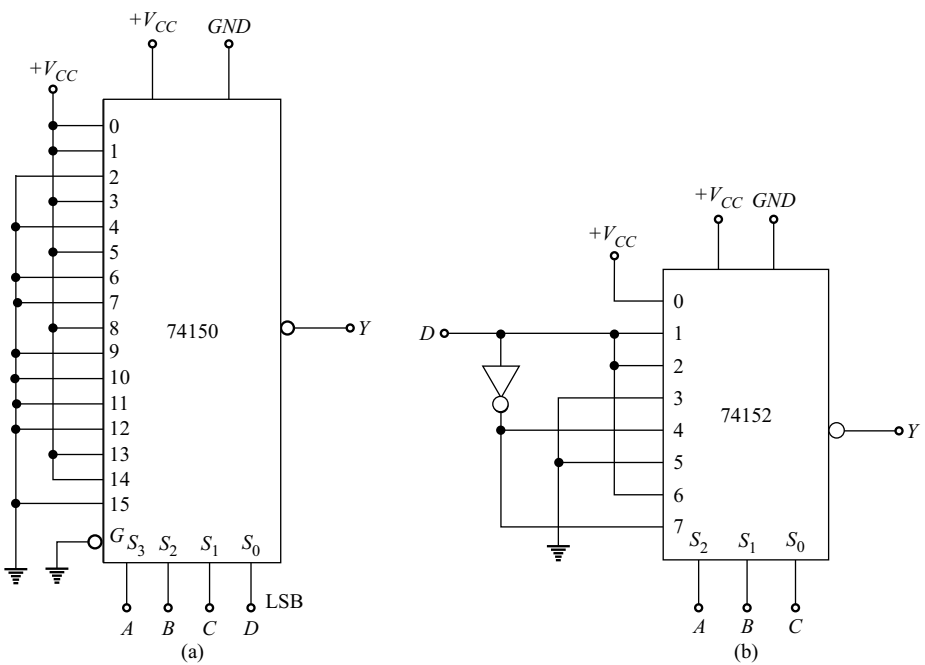
5.25 (a) Yes. Add one more term $\overline{B}C$ in the expression (5.38).

5.26 (b) Yes. Static-0.

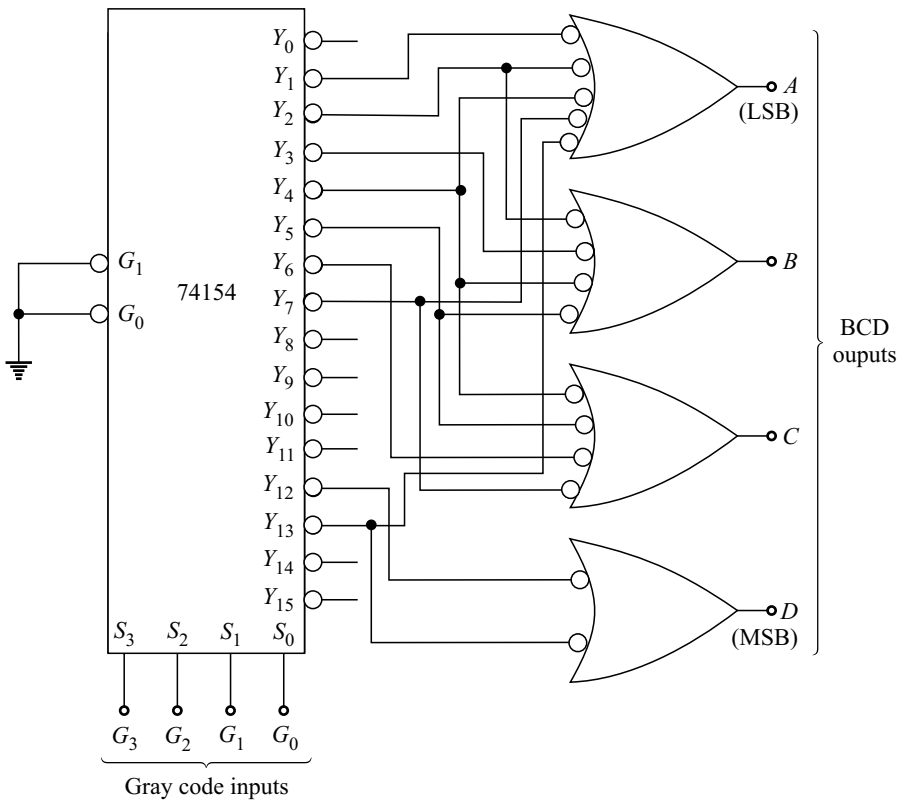
5.27 (b) Yes. Static-1.

# CHAPTER 6

6.1

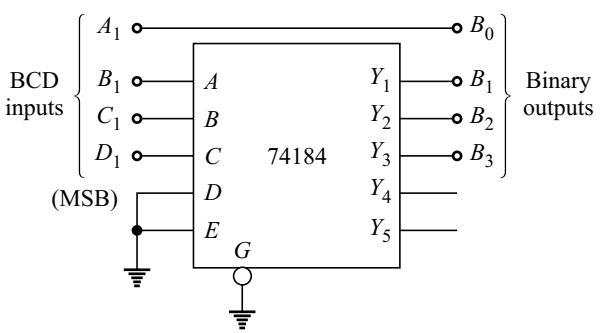


6.5 (b)

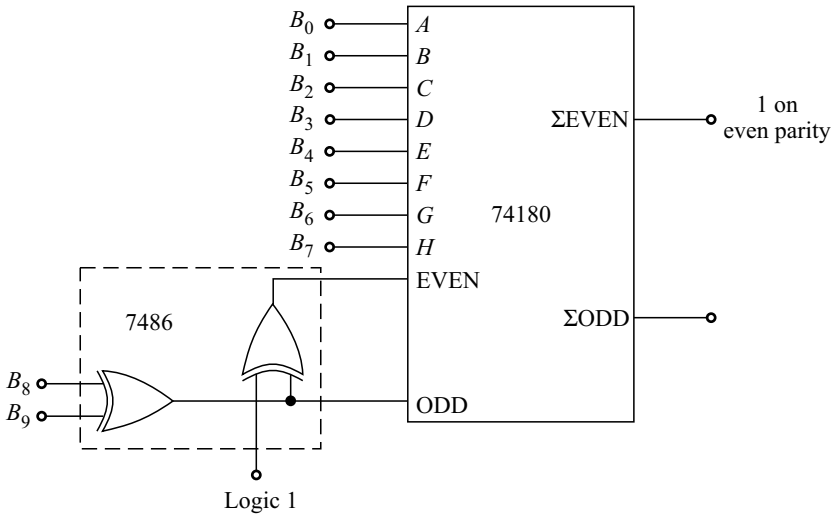



6.11 $t_{pd} = 40\,n$ ns

6.16



6.21




## CHAPTER 7

7.14 (a) $Y_1 = \overline{\overline{Q} \cdot J \cdot CK}$

$Y_2 = \overline{Q \cdot K \cdot CK}$

(b) $Y_1 = \overline{CK \cdot D}$

$Y_2 = \overline{CK \cdot \overline{D}}$

(c) $Y_1 = \overline{CK \cdot T \cdot \overline{Q}}$

$Y_2 = \overline{CK \cdot T \cdot Q}$

7.15 (a) $S = D, R = \overline{D}$

(b) $J = D, K = \overline{D}$

(c) $D = J \cdot \overline{Q} + \overline{K} \cdot Q$

(d) $S = T \cdot \overline{Q}, R = T \cdot Q$

(e) $J = K = T$

(f) $T = J \cdot \overline{Q} + K \cdot Q$

(g) $T = D \oplus Q$

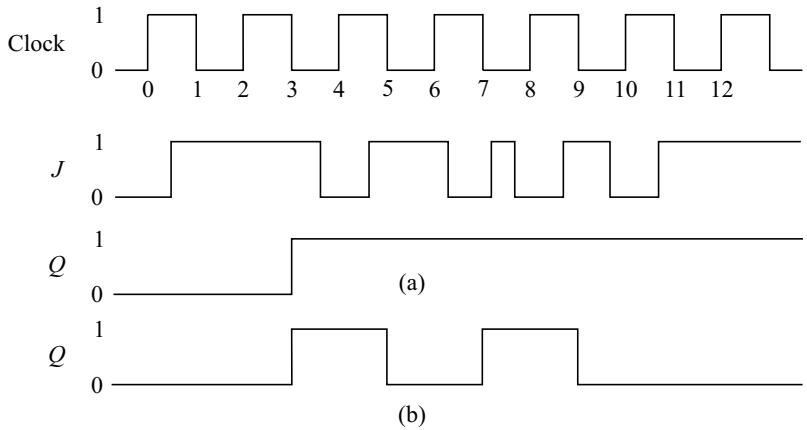
(h) $D = S + \overline{R} \times Q$

(i) $D = T \oplus Q$

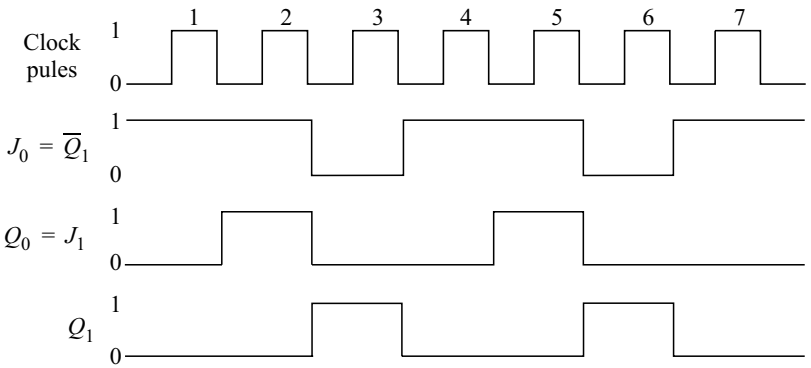
(j) $T = S\overline{Q} + RQ$

(k) $J = S, K = R$

7.17



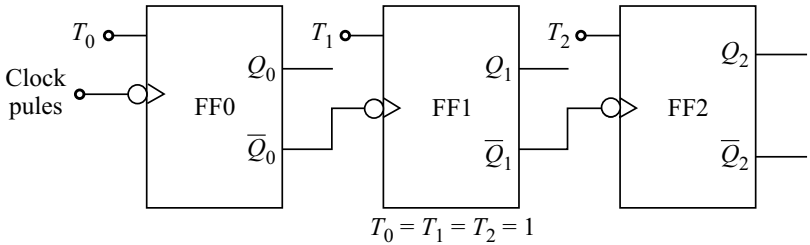

7.20



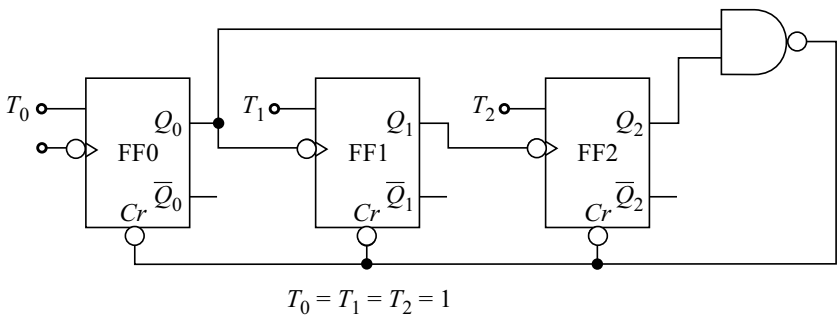

## CHAPTER 8

8.5 Count sequence:

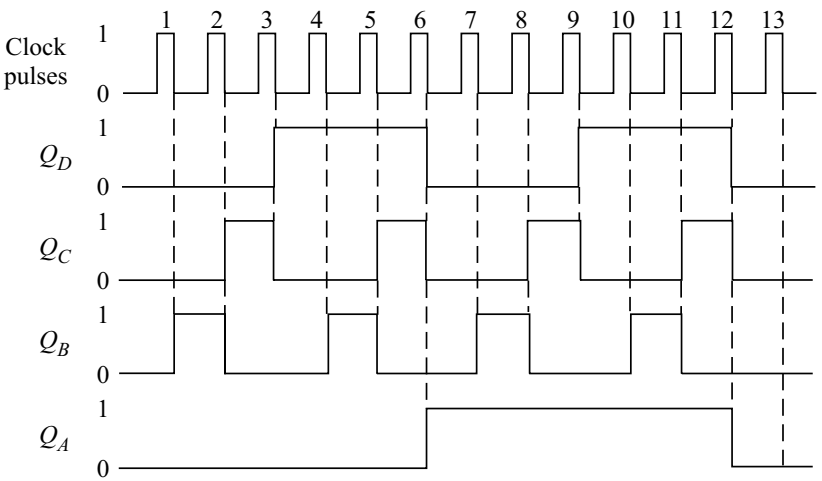
| $Q_2$ | $Q_1$ | $Q_0$ |
|---|---|---|
| 0 | 0 | 0 |
| 1 | 1 | 1 |
| 1 | 1 | 0 |
| 1 | 0 | 1 |
| 1 | 0 | 0 |
| 0 | 1 | 1 |
| 0 | 1 | 0 |
| 0 | 0 | 1 |


$T_0$
Clock pules
FF0
$Q_0$
$\overline{Q}_0$
$T_1$
FF1
$Q_1$
$\overline{Q}_1$
$T_2$
FF2
$Q_2$
$\overline{Q}_2$
$T_0 = T_1 = T_2 = 1$

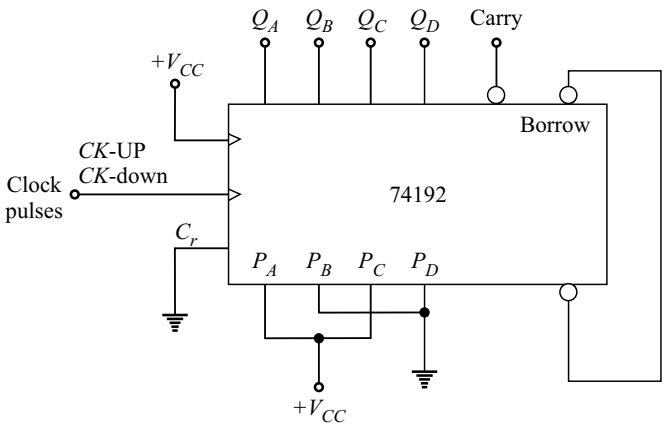
8.9 (a)

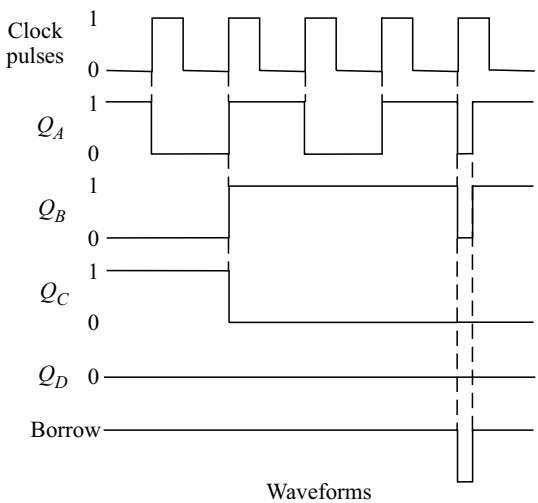

$T_0$
FF0
$Q_0$
$Cr$
$\overline{Q}_0$
$T_1$
FF1
$Q_1$
$Cr$
$\overline{Q}_1$
$T_2$
FF2
$Q_2$
$Cr$
$\overline{Q}_2$
$T_0 = T_1 = T_2 = 1$

8.10


Clock pulses
1 2 3 4 5 6 7 8 9 10 11 12 13
1
0
$Q_D$
$Q_C$
$Q_B$
$Q_A$

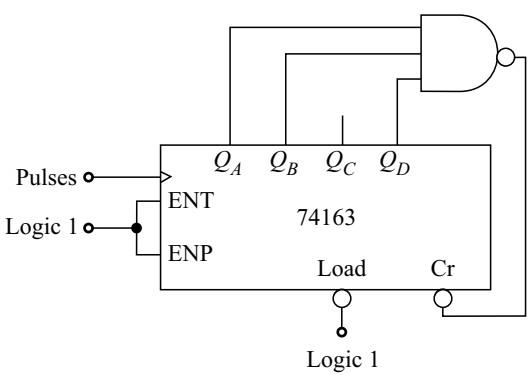
8.21



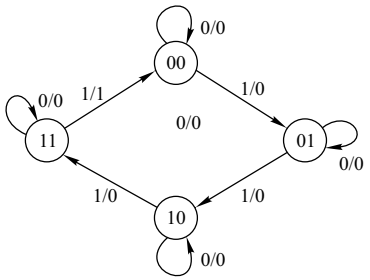




Waveforms

8.25



8.26 (b)



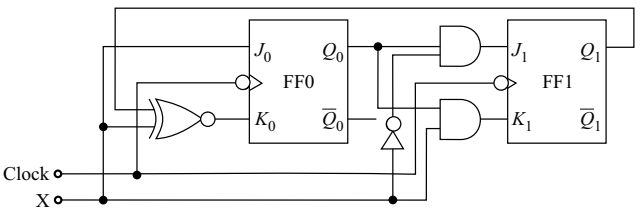

8.27 (a) $D_1 = Q_1 \oplus X$

$D_0 = Q_0 \oplus Q_1$

$Z = \overline{Q}_1 \cdot \overline{X}_1 + Q_0$

(b) 001110

8.28




8.33 01000111010

8.34 (b) (a)-(i) yes, critical

(a)-(ii) yes, non-critical

## CHAPTER 9

9.4 $V_{UT} \approx 1.0042$ V

$V_{LT} \approx 0.9938$ V

9.10 (a) R = 1.5 kΩ, $C$ = 200 pF

(b) R = 10 kΩ, $C$ = 35 pF

9.11 (a) 134 Hz

(b) 180 Hz

9.12 $R_A$ = 1 kΩ

$R_B$ = 2 kΩ

$C$ = 4.67 nF

9.13 (b) $T = 0.7\, R_A C + \dfrac{R_A R_B}{R_A + R_B} C \ln\left(\dfrac{2R_A - R_B}{R_A - 2R_B}\right)$

(d) 48 kΩ

(e) $R_B < R_A/2$

## CHAPTER 10

10.1 5/255 V

10.2

| Digital input | | | Analog output |
|---|---|---|---|
| $S_2$ | $S_1$ | $S_0$ | $V$ |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 2 |
| 0 | 1 | 1 | 3 |
| 1 | 0 | 0 | – 3 |
| 1 | 0 | 1 | – 2 |
| 1 | 1 | 0 | – 1 |
| 1 | 1 | 1 | 0 |

10.8 Less than 12/s
10.9 10/63 V

## CHAPTER 11

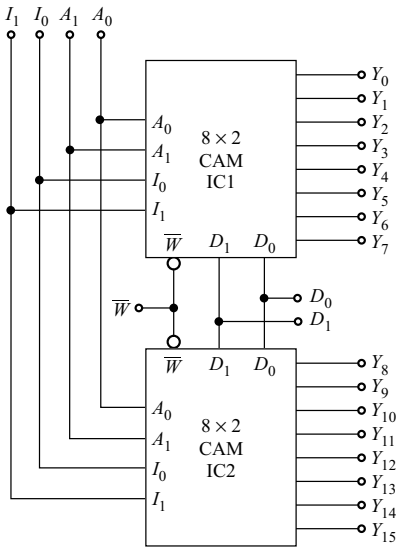
11.1 (a) 2 (b) 4 (c) 6 (d) 8
(e) 10 (f) 11 (g) 16 (h) 20

11.2 (a) (i) 0 – 3 (ii) 0 – *F* (iii) 00 – 3*F* (iv) 00 – *FF*
(v) 000 – 3*FF* (vi) 000 – 7*FF* (vii) 0000 – *FFFF* (viii) 00000 – *FFFFF*
(b) (i) 0 – 3 (ii) 00 – 17 (iii) 00 – 77 (iv) 000 – 377
(v) 0000 – 1777 (vi) 0000 – 3777 (vii) 000000 – 177777 (viii) 0000000 – 3777777

11.4 (a) 4 RAM chips and one 2-line-to-4-line decoder IC
(b) 2 RAM chips
(c) 32 RAM chips and one 4-line-to-16-line decoder IC

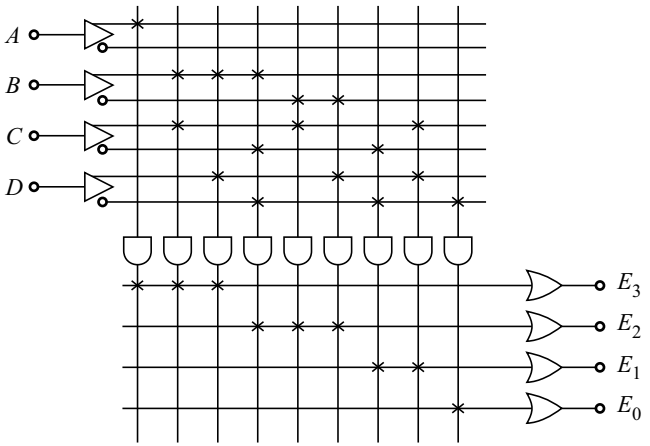
11.6 (a) 2 (b) 2 (c) 4

11.13

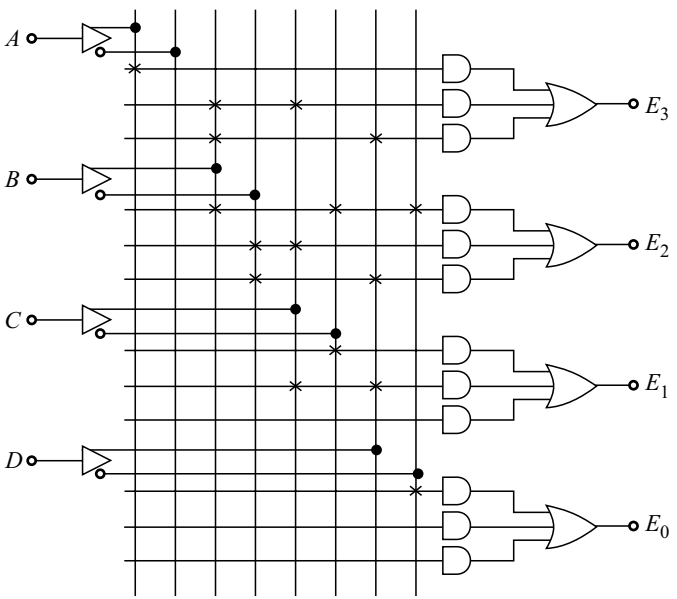


# CHAPTER 12

12.1 (b)




(c)




12.4 The inputs of two 82S100 devices are to be connected in parallel to get 16 outputs.

12.11

| $x_1$ | $x_2$ | $f$ |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

12.12

| |
|---|
| 0 |
| 1 |
| 1 |
| 0 |
| 1 |
| 0 |
| 0 |
| 1 |

## CHAPTER 13

13.1

| *Microprocessor* | *Address space* |
|---|---|
| 8080A | 64 K bytes |
| 6800 | 64 K bytes |
| 8086 | 1 M bytes |
| 9900 | 64 K bytes |
| Z8000 | 8 M bytes |

13.2 256

13.3 (a) 8 RAMs and 1 EPROM

13.4 MVI A, 00H; SUB A; ANI 00H; XRA A

13.6

```
        LXI H,   0A02H
        LDA      0A00H
        MOV      B, A
        LDA      0A01H
        CMP      B
        JZ       FINIS
        JC       GREAT
        MOV      M, A
        JMP      FINIS
GREAT:  M0V      M, B
FINIS:
```

13.7

```
LXI     H,01A0H
MVI     M,00H
```

13.9

```
ANI     0FH
```

13.11 12 bytes

13.14

```
POP     PSW
P0P     H
P0P     D
P0P     B
EI
RET
```

## CHAPTER 14

14.1 (a) Yes. It contains all the allowed characters.
(b) No. Character '•' is not permitted.

(c) No. Starting character can not be a numeral.
(d) Yes. Upper and lower case characters can be mixed.
(e) No. Hyphen (–) is not allowed.
(f) No. Two consecutive underscores are not allowed.

14.2 (a)
```
ENTITY NAND2 IS
PORT (X, Y: IN BIT; Z: OUT BIT);
END NAND2;
```

(b)
```
ENTITY NAND3 IS
PORT (A, B, C: IN BIT; Y: OUT BIT);
END NAND3;
```

14.3 A 4:1 multiplexer is shown in Fig. below. It has four data inputs $I_0$, $I_1$, $I_2$, and $I_3$ and two select inputs $A$ and $B$. There is one output $Y$.

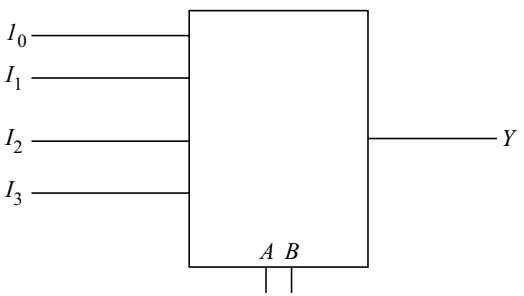



Fig. Prob. 14.3

The entity declaration is

```
LIBRARY IEEE;
USE IEEE STD_LOGIC_1164.ALL;
ENTITY MULTI_4 IS
PORT (I0, I1, I2, I3, A, B: IN STD_LOGIC; Y: OUT STD_LOGIC);
END MULTI_4;
```

14.4 (a) For 2-input NAND gate

```
ARCHITECTURE df_nand2 OF NAND2 IS
BEGIN
Z <= NOT (X AND Y) AFTER 10 ns;
END df_nand2;
```

(b) For 3-input NAND gate

```
ARCHITECTURE df_nand3 OF NAND3 IS
BEGIN
Y <= NOT (A AND B AND C) AFTER 10 ns;
END df_nand3;
```

14.5 Figure 5.21 is redrawn below with the signals marked, and NAND gates numbered.

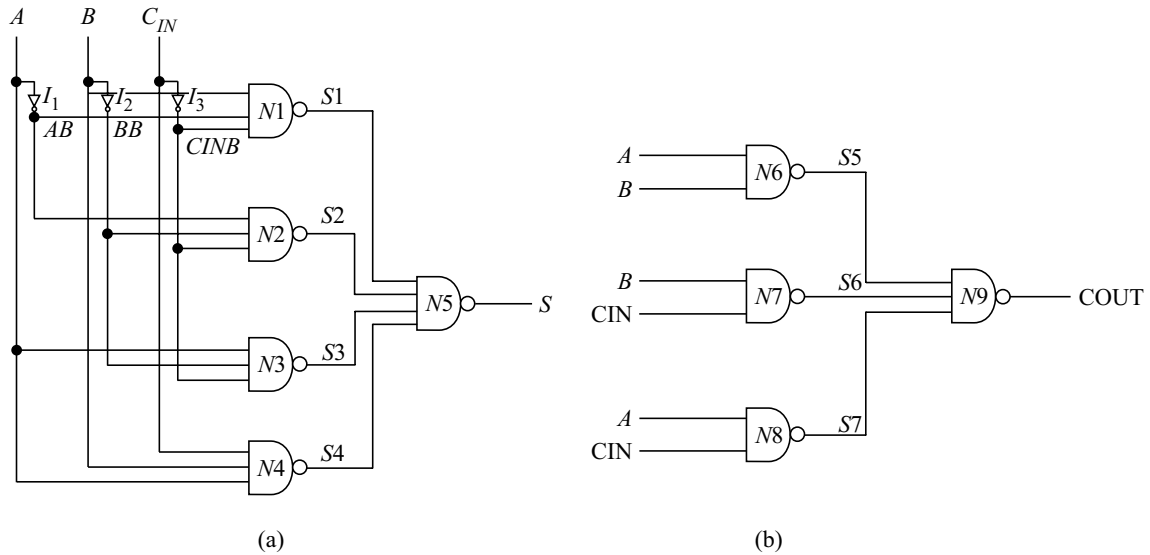



Fig. Prob. 14.5

```
LIBRARY IEEE;
USE IEEE. STD_LOGIC_1164.ALL;
– – Name of entity chosen is F_A
ENTITY F_A IS
PORT  (A, B, CIN: IN STD_LOGIC; S, COUT : OUT STD_LOGIC);
END F_A;
ARCHITECTURE FA_STR OF F_A IS
COMPONENT NAND3
PORT (X1, X2, X3 : IN STD_LOGIC; Y : OUT STD_LOGIC);
END COMPONENT;
COMPONENT  NAND4
PORT (X4, X5, X6, X7 : IN STD_LOGIC; Z OUT STD_LOGIC);
END  COMPONENT;
COMPONENT INV
PORT (P : IN STD_LOGIC; Q : OUT STD_LOGIC);
END  COMPONENT;
COMPONENT  NAND2
PORT (X8, X9 : IN STD_LOGIC; R : OUT STD_LOGIC);
END COMPONENT;
SIGNAL AB, BB, CINB, S1, S2, S3, S4, S5, S6, S7: STD_LOGIC;
BEGIN
I1 : INV PORT MAP (A, AB);
I2 : INV PORT MAP (B, BB);
I3 : INV PORT MAP (CIN, CINB);
N1 : NAND3 PORT MAP (AB, B, CINB, S1);
N2 : NAND3 PORT MAP (AB, BB, CIN, S2);
```

```
    N3 : NAND3 PORT MAP (A, BB, CINB, S3);
    N4 : NAND3 PORT MAP (A, B, CIN, S4);
    N5 : NAND4 PORT MAP (S1, S2, S3, S4, S);
    N6 : NAND2 PORT MAP (A, B, S5);
    N7 : NAND2 PORT MAP (B, CIN, S6);
    N8 : NAND2 PORT MAP (A, CIN, S7);
    N9 : NAND3 PORT MAP (S5, S6, S7, COUT);
    END FA_STR;
```

14.6

```
    LIBRARY IEEE;
    USE IEEE.STD_LOGIC_1164.ALL;
    ENTITY F_A IS
    PORT (A, B, CIN: IN  STD_LOGIC; S, COUT : OUT STD_LOGIC);
    END F_A;
    ARCHITECTURE  FULL_ADDER OF F_A IS
    BEGIN
    S <= ((NOT A) AND B AND (NOT CIN)) OR
         ((NOT A) AND (NOT B) AND CIN) OR
         (A AND (NOT B) AND (NOT CIN)) OR
         (A AND B AND CIN) AFTER 15 ns;
    COUT <= (A AND B) OR (B AND CIN) OR
              (A AND CIN) AFTER 10 ns;
    END FULL_ADDER;
```